PHX23NQ11T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 14 May 2004 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a fully isolated encapsulated plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Isolated package.

1.3 Applications

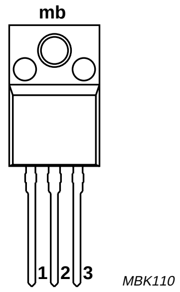
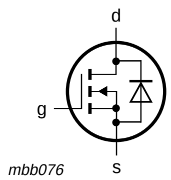
- DC-to-DC converters
- Switched-mode power supplies.

1.4 Quick reference data

- $V_{DS} \leq 110$ V
- $P_{tot} \leq 41.6$ W
- $I_D \leq 16$ A
- $R_{DSon} \leq 70$ mΩ.

2. Pinning information

Table 1: Pinning - SOT186A (TO-220F) simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base; isolated		

SOT186A (TO-220F)

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHX23NQ11T	TO-220F	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 'full pack'	SOT186A

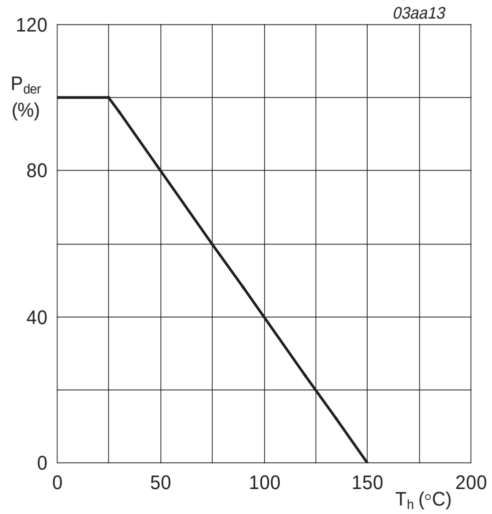
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

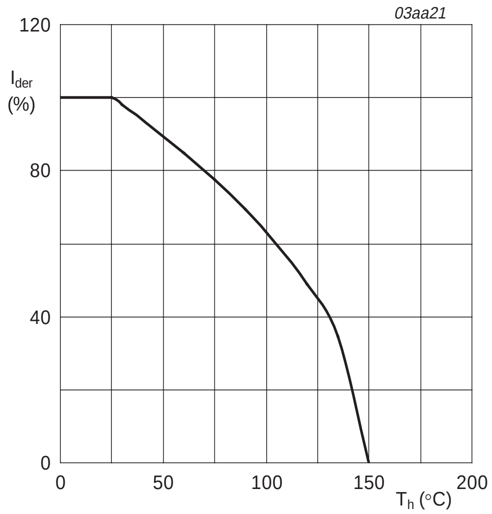
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\ °C \leq T_j \leq 150\ °C$		-	110	V
V_{DGR}	drain-gate voltage (DC)	$25\ °C \leq T_j \leq 150\ °C$; $R_{GS} = 20\ k\Omega$		-	110	V
V_{GS}	gate-source voltage (DC)			-	±20	V
I_D	drain current (DC)	$T_h = 25\ °C$; $V_{GS} = 10\ V$; Figure 2 and 3	[1]	-	16	A
		$T_h = 100\ °C$; $V_{GS} = 10\ V$; Figure 2	[1]	-	10.1	A
I_{DM}	peak drain current	$T_h = 25\ °C$; pulsed; $t_p \leq 10\ \mu s$; Figure 3	[1]	-	64.3	A
P_{tot}	total power dissipation	$T_h = 25\ °C$; Figure 1	[1]	-	41.6	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_S	source (diode forward) current (DC)	$T_h = 25\ °C$	[1]	-	16	A
I_{SM}	peak source (diode forward) current	$T_h = 25\ °C$; pulsed; $t_p \leq 10\ \mu s$	[1]	-	64.3	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 14\ A$; $t_p = 0.1\ ms$; $V_{DD} \leq 100\ V$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\ V$; starting at $T_j = 25\ °C$		-	93	mJ

[1] External heatsink, connected to mounting base.



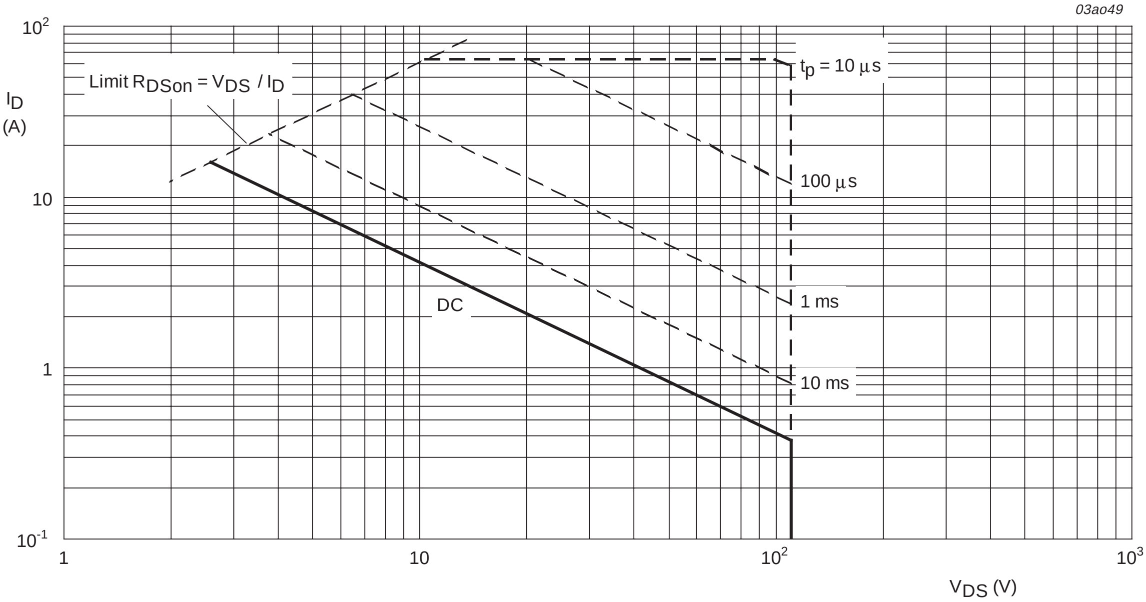
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of heatsink temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of heatsink temperature.



T_h = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	Figure 4	[1]	-	-	3	K/W

[1] External heatsink, connected to mounting base.

5.1 Transient thermal impedance

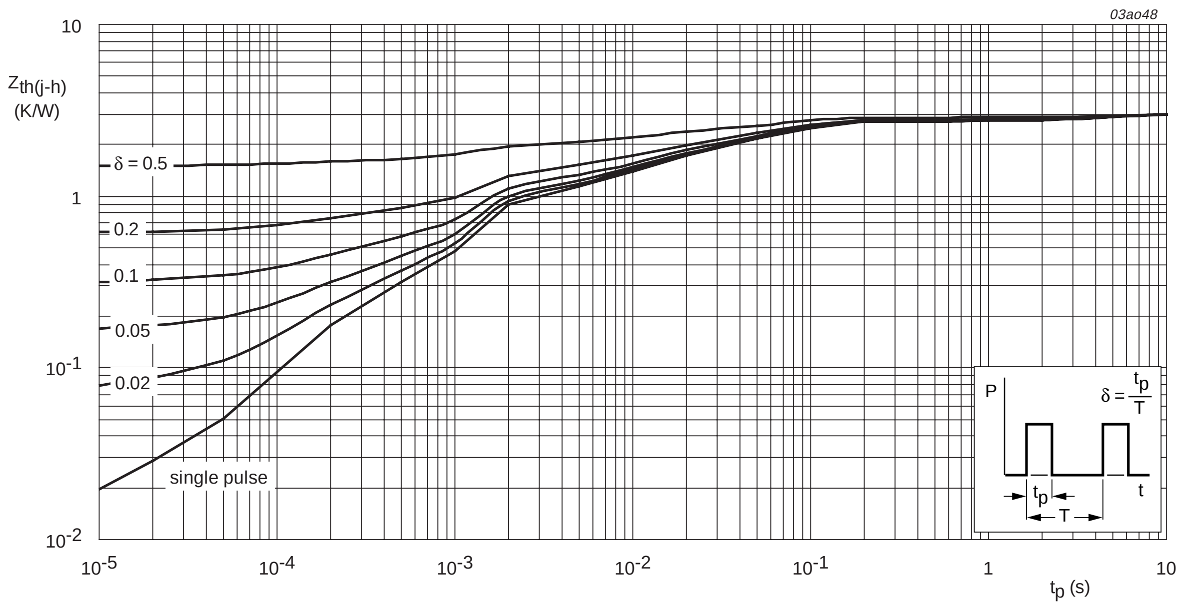


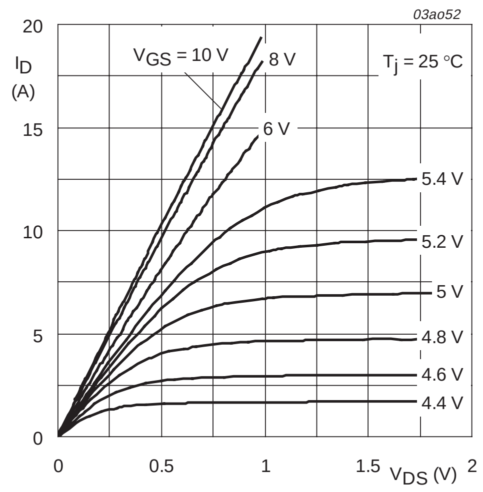
Fig 4. Transient thermal impedance from junction to heatsink as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

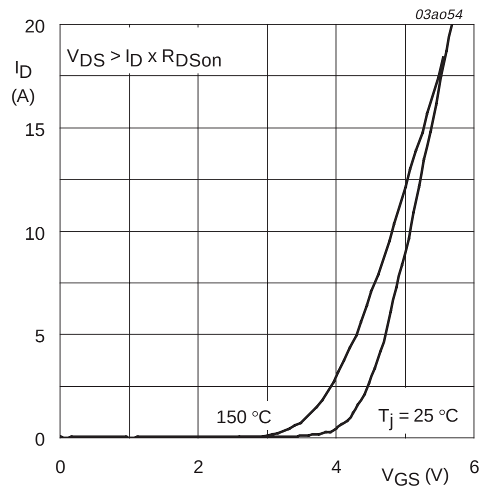
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	110	-	-	V
		T_j = –55 °C	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	2	3	4	V
		T_j = 150 °C	1	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	10	µA
		T_j = 150 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 13 A; Figure 7 and 8				
		T_j = 25 °C	-	49	70	mΩ
		T_j = 150 °C	-	132	189	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 23 A; V_{DD} = 80 V; V_{GS} = 10 V; Figure 13	-	22	-	nC
Q_{gs}	gate-source charge		-	5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	10	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	830	-	pF
C_{oss}	output capacitance		-	140	-	pF
C_{rss}	reverse transfer capacitance		-	85	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 50 V; R_L = 2.2 Ω; V_{GS} = 10 V; R_G = 5.6 Ω	-	8	-	ns
t_r	rise time		-	39	-	ns
$t_{d(off)}$	turn-off delay time		-	26	-	ns
t_f	fall time		-	24	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 11 A; V_{GS} = 0 V; Figure 12	-	0.9	1.5	V
t_{rr}	reverse recovery time	I_S = 11 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	64	-	ns
Q_r	recovered charge		-	120	-	nC



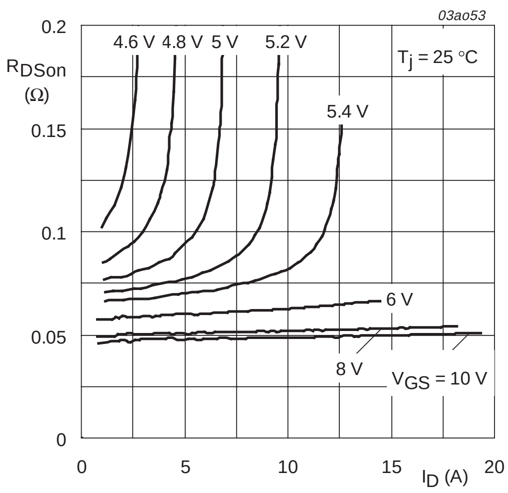
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



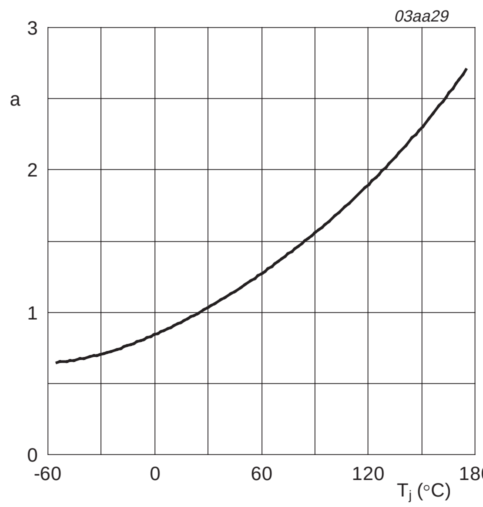
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



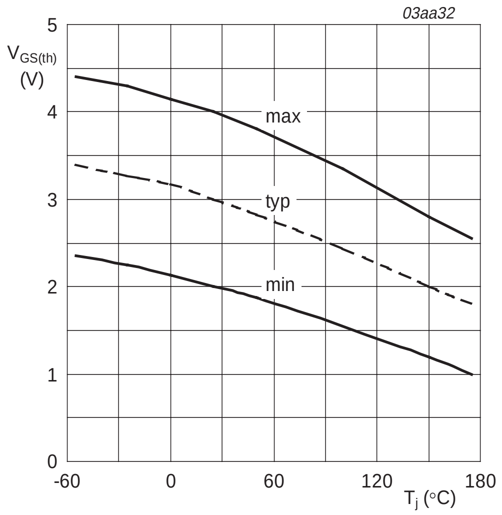
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



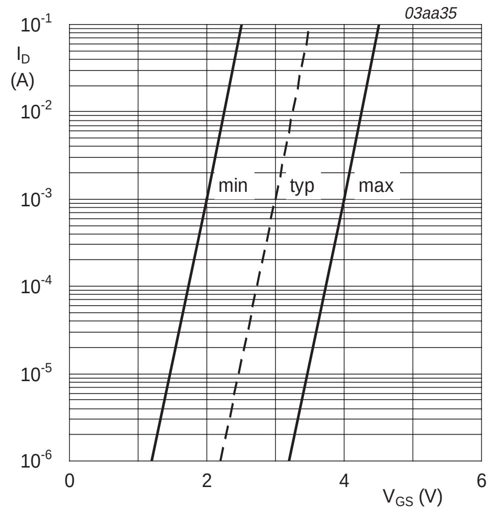
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



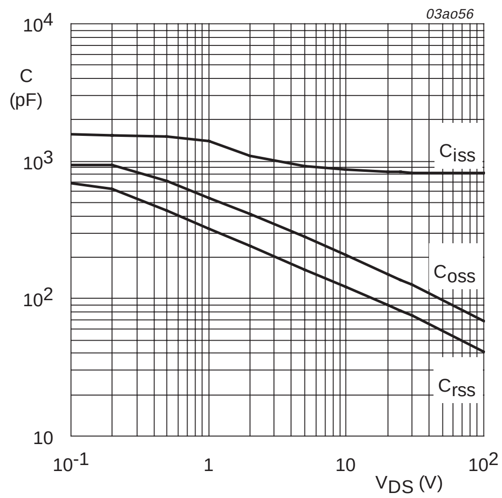
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



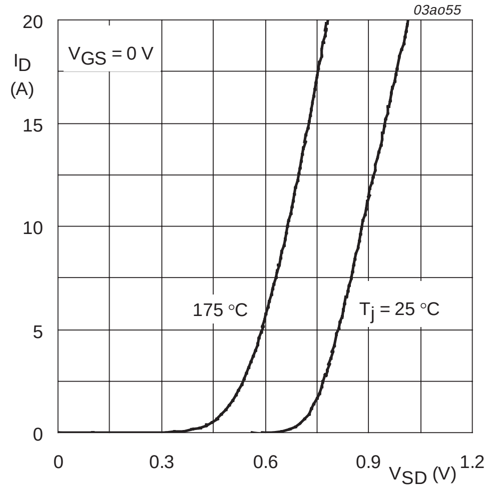
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



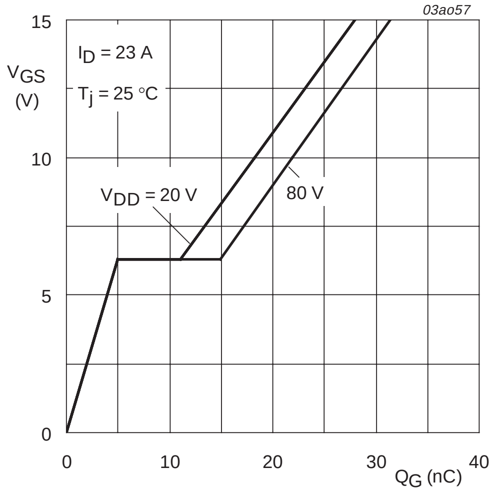
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



I_D = 23 A; V_{DD} = 20 V and 80 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

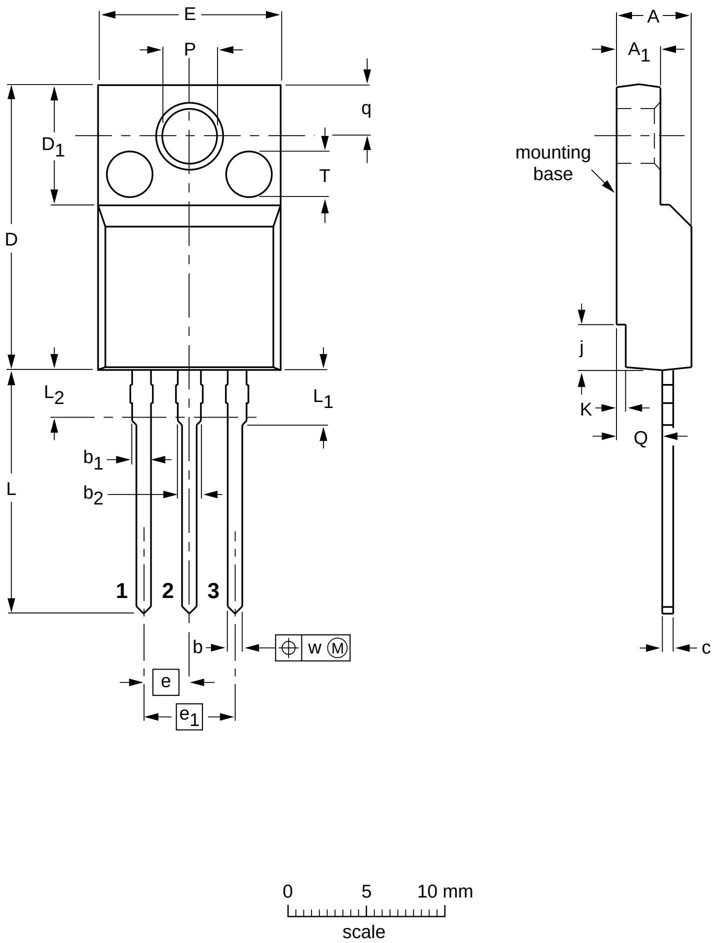
7. Isolation characteristics

Table 6: Isolation characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{isol}	RMS isolation voltage from all three terminals to external heatsink.	f = 50-60 Hz; sinusoidal waveform; RH ≤ 65%; clean and dust-free.	-	-	2500	V
C_{isol}	Capacitance from pin 2 (drain) to external heatsink.	f = 1 MHz	-	10	-	pF

8. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 'full pack' **SOT186A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2[(1)] max.	P	Q	q	T[(2)]	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-03-12~~ 02-04-09

Fig 14. SOT186A (TO-220F).

9. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
01	20040514	-	Product data (9397 750 13177)

10. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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