



**THE DATASHEET OF  
74LVC2G02DP,125**



# 74LVC2G02

Dual 2-input NOR gate

Rev. 13 — 20 April 2018

Product data sheet

## 1 General description

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The 74LVC2G02 provides a 2-input NOR gate function.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

## 2 Features and benefits

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- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G02DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G02DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G02GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74LVC2G02GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089
74LVC2G02GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2
74LVC2G02GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116
74LVC2G02GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm	SOT1203

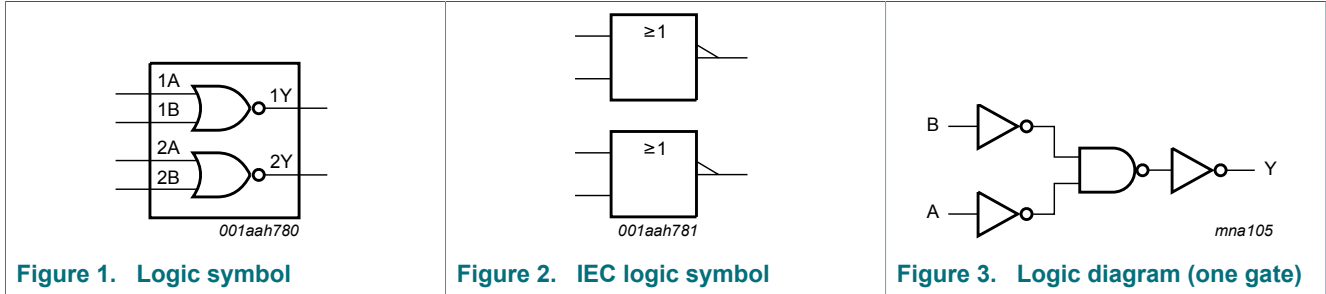
### 4 Marking

Table 2. Marking codes

Type number	Marking code <sup>[1]</sup>
74LVC2G02DP	V02
74LVC2G02DC	V02
74LVC2G02GT	V02
74LVC2G02GF	VB
74LVC2G02GM	V02
74LVC2G02GN	VB
74LVC2G02GS	VB

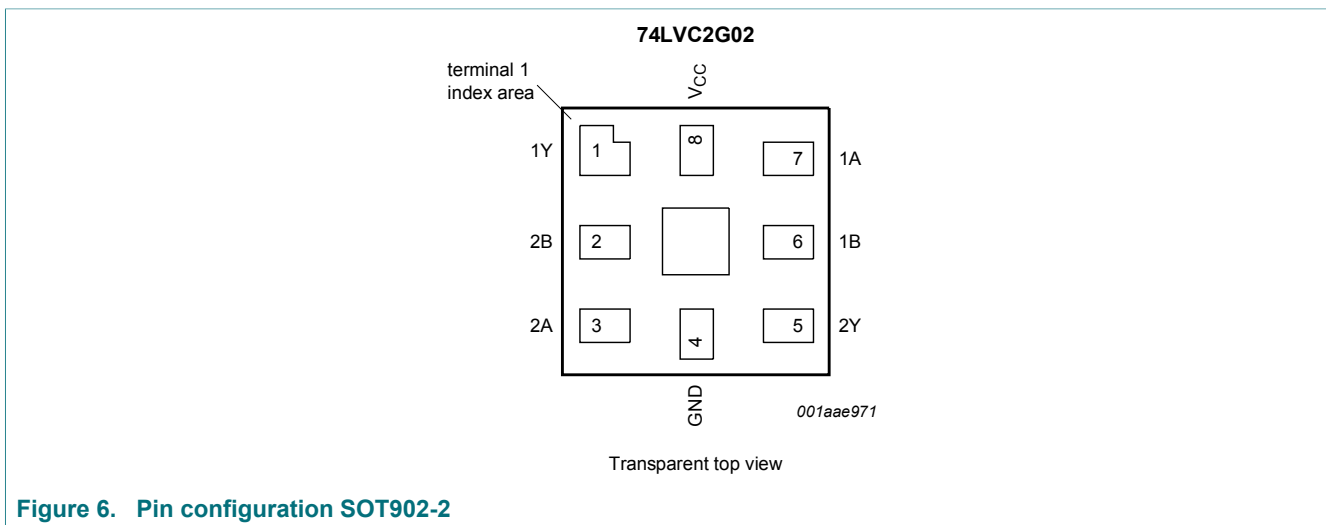
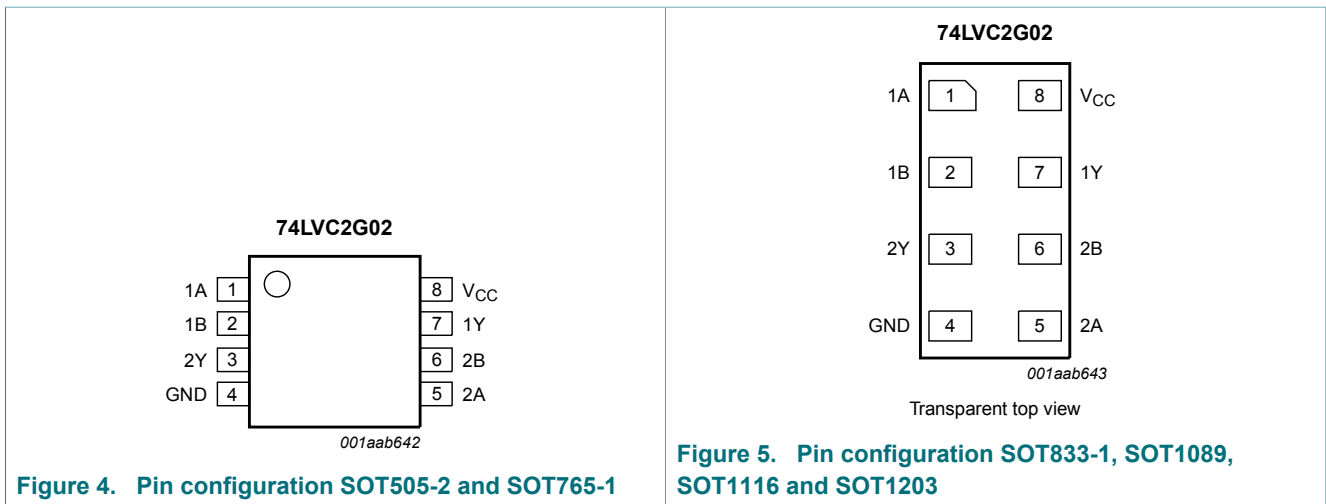
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

**5 Functional diagram**



**6 Pinning information**

**6.1 Pinning**



## 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT1116 and SOT1203	SOT902-2	
1A, 2A	1, 5	7, 3	data input
1B, 2B	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Y, 2Y	7, 3	1, 5	data output
V <sub>CC</sub>	8	8	supply voltage

## 7 Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care.*

Input		Output
nA	nB	nY
L	L	H
X	H	L
H	X	L

## 8 Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$V_I$	input voltage	[1]	-0.5	+6.5	V
$V_O$	output voltage	Active mode [1]	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; $V_{CC} = 0$ V [1]	-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$	-	$\pm 50$	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of  $P_{tot}$  derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

For XSON8 and XQFN8 packages: above 118 °C the value of  $P_{tot}$  derates linearly with 7.8 mW/K.

## 9 Recommended operating conditions

**Table 6. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

## 10 Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	1.53	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.9	2.13	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	2.50	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.3	2.60	-	V
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.8	4.10	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	0.08	0.45	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	0.14	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.19	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.37	0.55	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	0.43	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	±0.1	±1	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	±0.1	±2	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	0.1	4	μA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 5.5 V	-	5	500	μA
C <sub>I</sub>	input capacitance		-	2.5	-	pF

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	0.95	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	1.9	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.0	-	-	V
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.4	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±1	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	-	±2	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	-	4	µA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 5.5 V	-	-	500	µA

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 11 Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	3.8	8.9	1.2	11.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.8	2.4	5.4	0.8	6.8	ns
		V <sub>CC</sub> = 2.7 V	0.8	3.2	6.0	0.8	7.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.6	2.4	4.9	0.6	6.2	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.6	1.8	4.3	0.6	5.5	ns
C <sub>PD</sub>	power dissipation capacitance	per gate; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>	-	14	-	-	-	pF

[1] Typical values are measured at nominal V<sub>CC</sub> and at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

### 11.1 Waveforms and test circuit

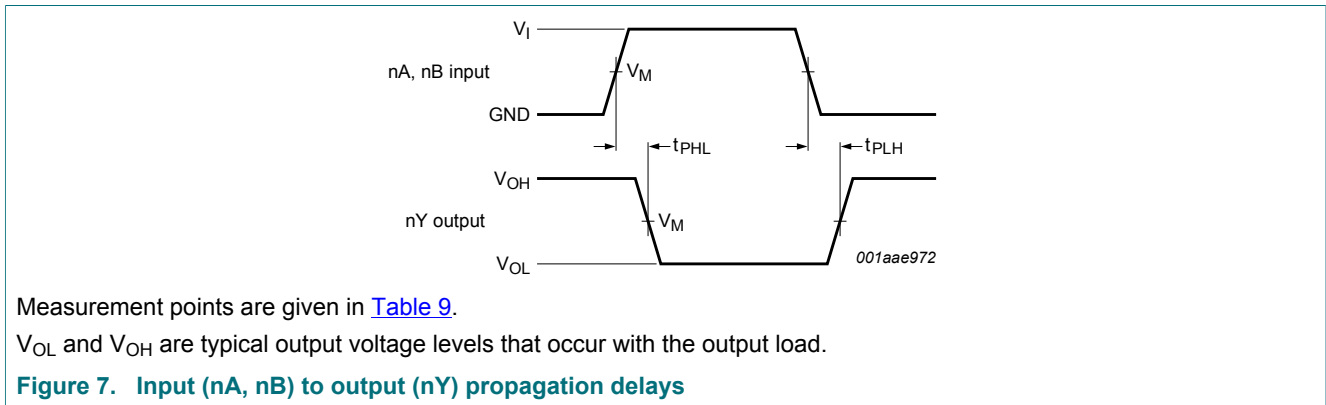
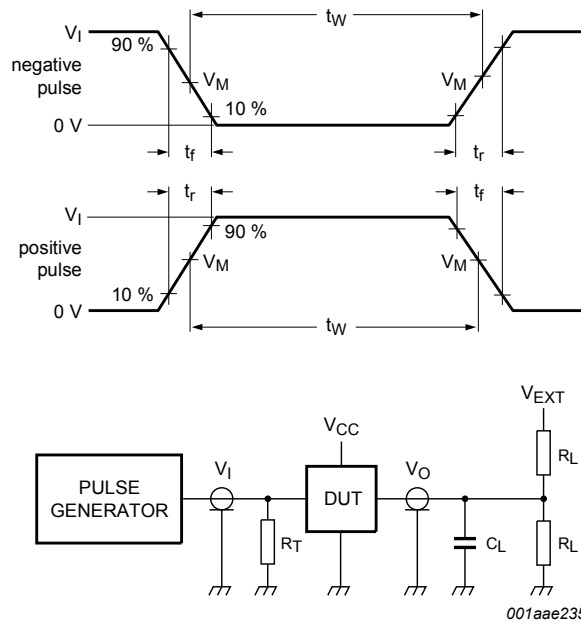


Table 9. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = Test voltage for switching times.

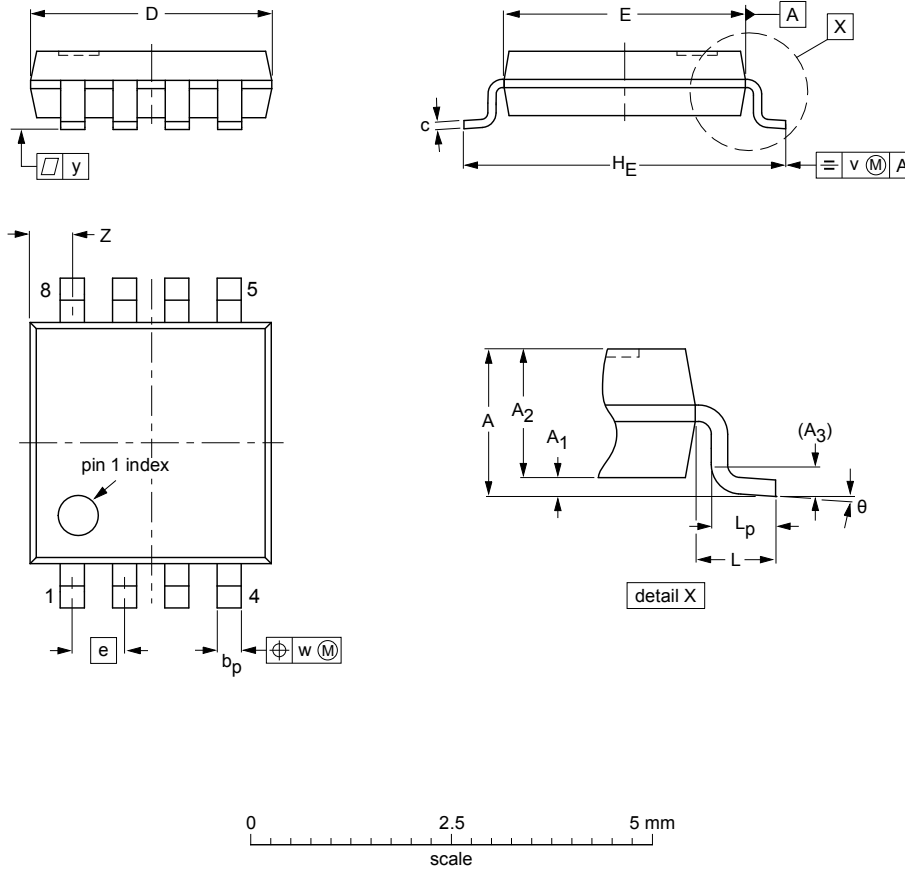
Figure 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load	$V_{EXT}$
$V_{CC}$	$V_I$	$C_L$	$t_{PLH}, t_{PHL}$
	$t_r, t_f$	$R_L$	
1.65 V to 1.95 V	$V_{CC}$	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	30 pF	500 $\Omega$
2.7 V	2.7 V	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	50 pF	500 $\Omega$
4.5 V to 5.5 V	$V_{CC}$	50 pF	500 $\Omega$

12 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

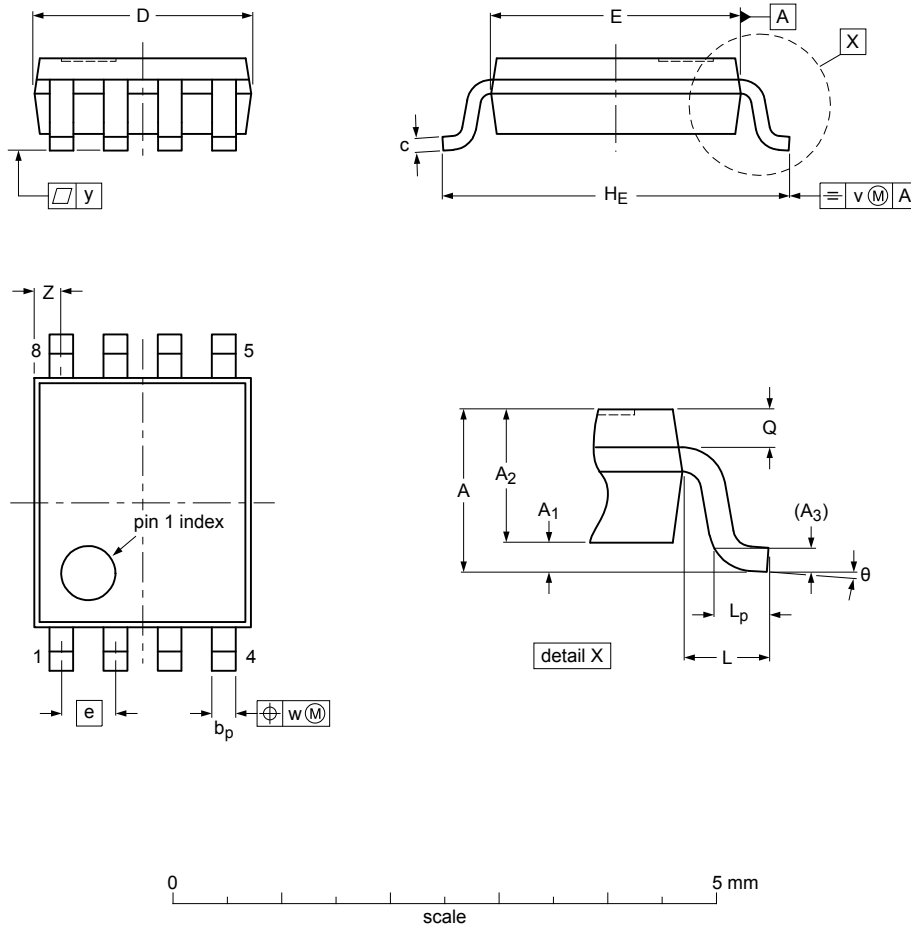
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT505-2		---			02-01-16

Figure 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
	max.																	
mm	max	0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1		0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60		0.17	0.08	1.9	2.2	3.0		0.15	0.19				0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

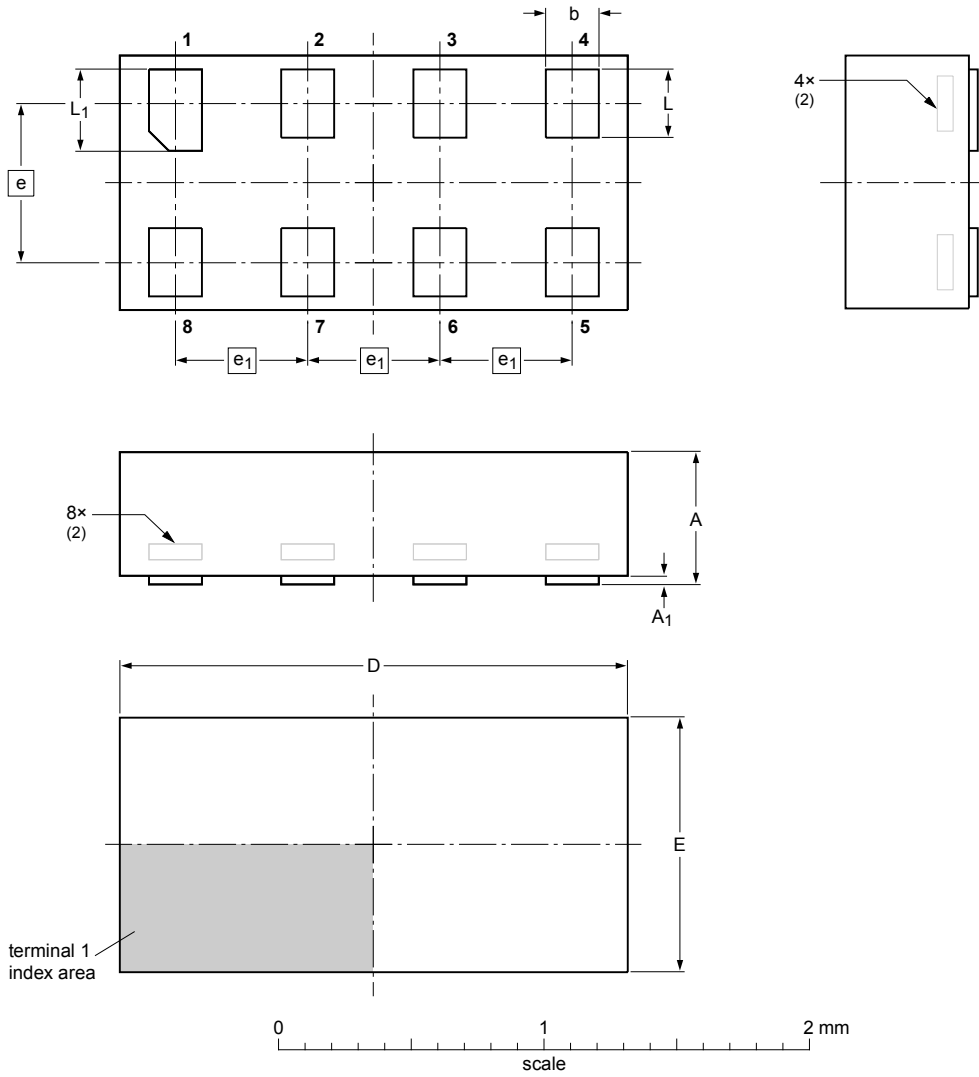
sot765-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				07-06-02 16-05-31

Figure 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max	A <sub>1</sub> max	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

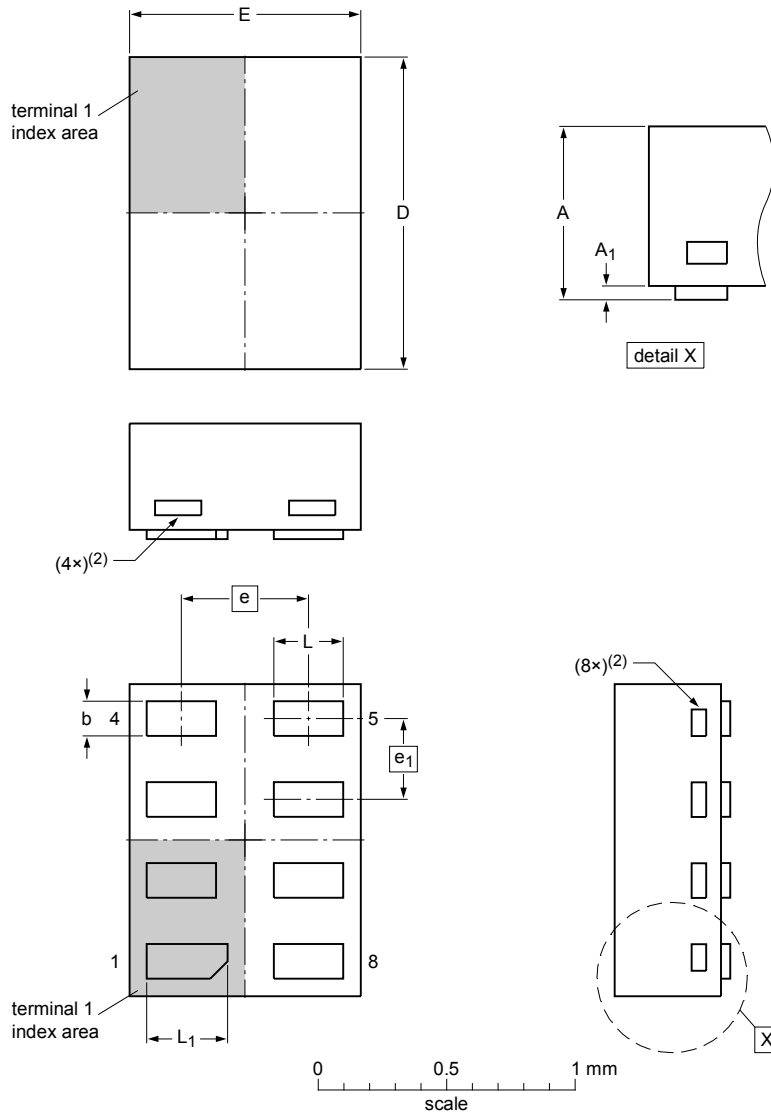
- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		07-11-14 07-12-07

Figure 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089



Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
min			0.12	1.30	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1089\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				10-04-09 10-04-12

Figure 12. Package outline SOT1089 (XSON8)

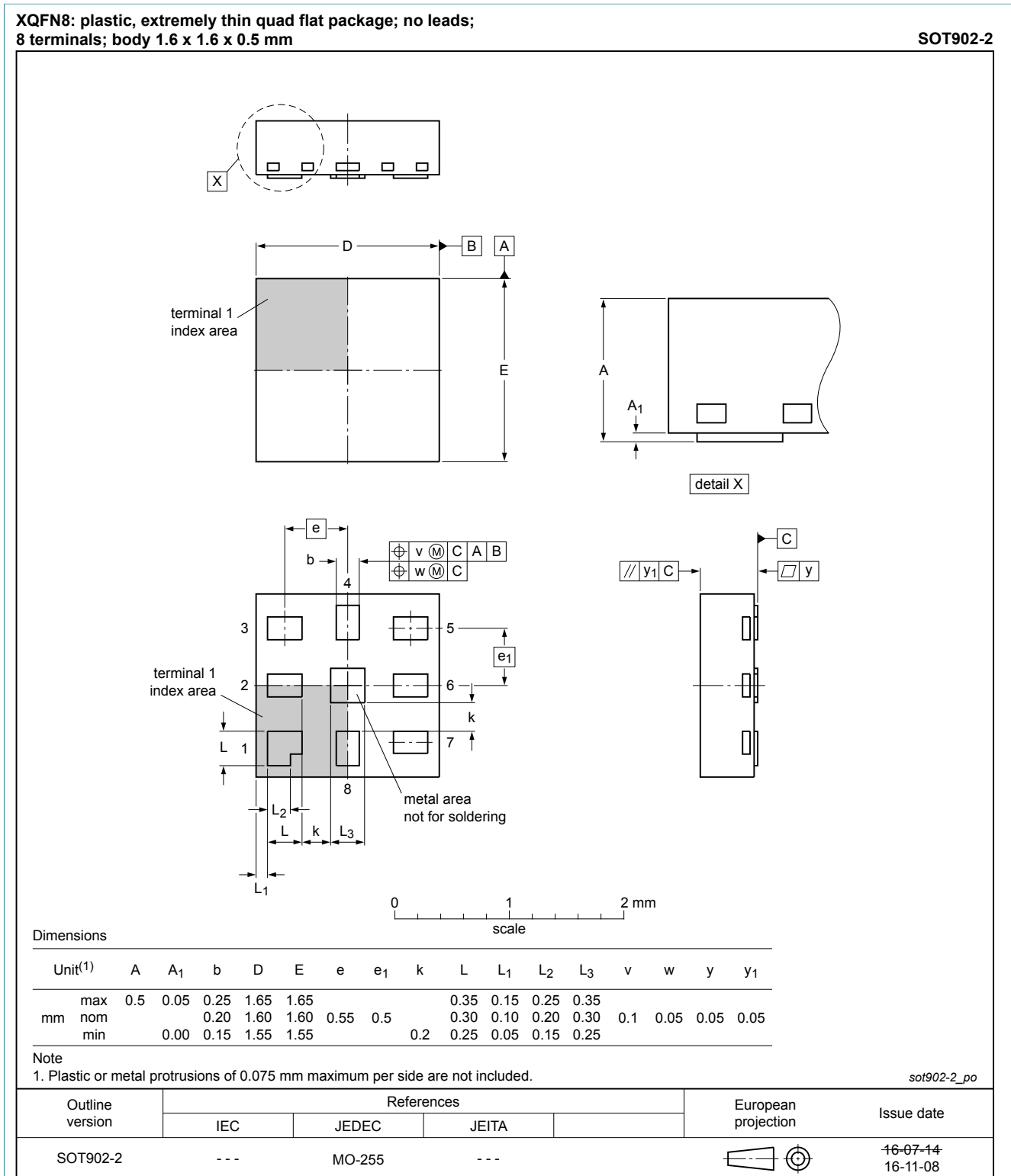
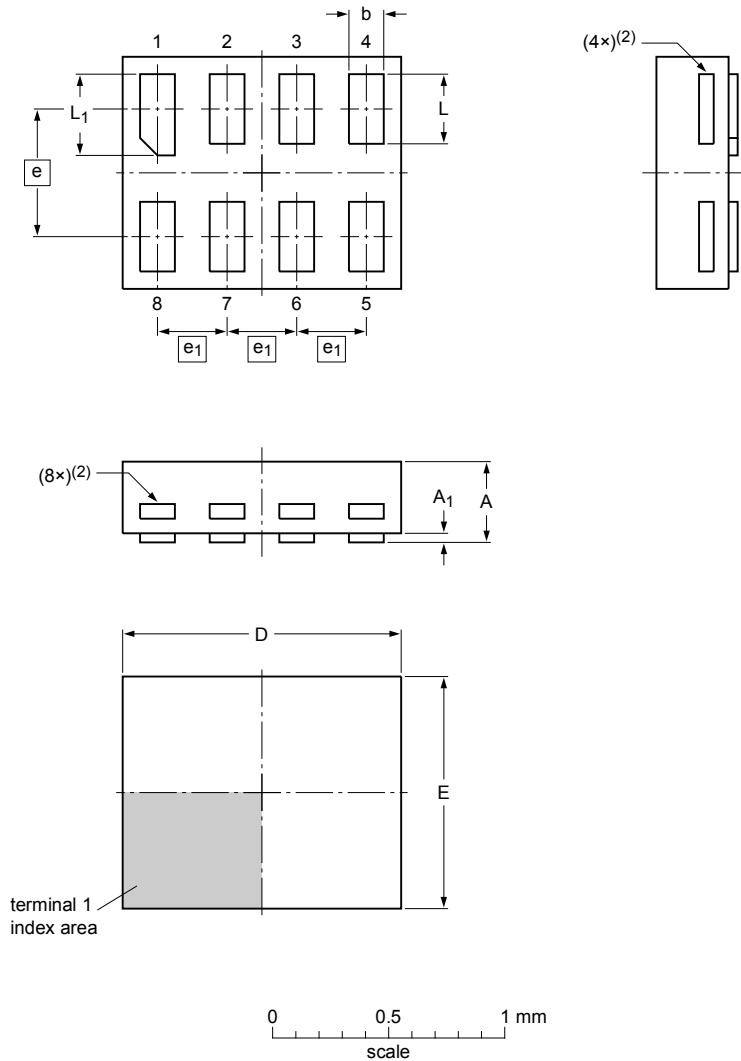


Figure 13. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116



Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
min			0.12	1.15	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

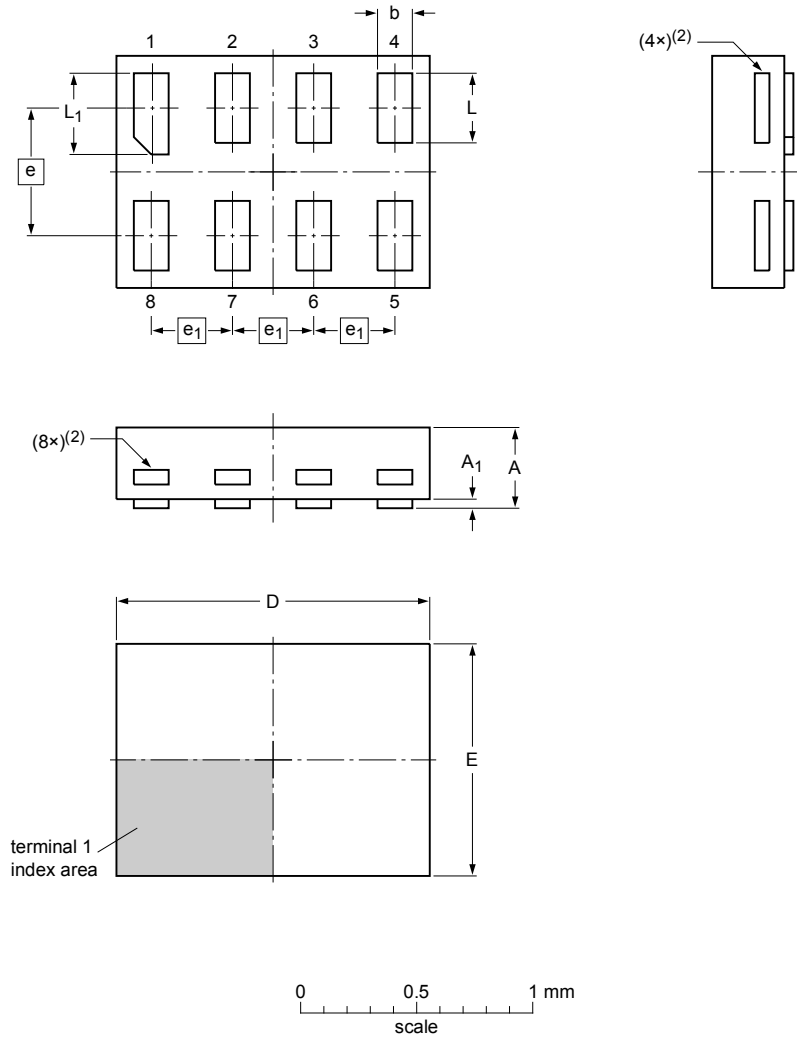
sot1116\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						-10-04-02- 10-04-07

Figure 14. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203



Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	max 0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom 0.15		1.35	1.00	0.55	0.35	0.30	0.35	
	min 0.12		1.30	0.95				0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1203\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						-10-04-02- 10-04-06

Figure 15. Package outline SOT1203 (XSON8)

## 13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G02 v.13	20180420	Product data sheet	-	74LVC2G02 v.12
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74LVC2G02GD (SOT996-2) removed.</li> </ul>			
74LVC2G02 v.12	20161212	Product data sheet	-	74LVC2G02 v.11
Modifications:	<ul style="list-style-type: none"> <li>Table 7: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC2G02 v.11	20130408	Product data sheet	-	74LVC2G02 v.10
Modifications:	<ul style="list-style-type: none"> <li>For type number 74LVC2G02GD XSON8U has changed to XSON8.</li> </ul>			
74LVC2G02 v.10	20120622	Product data sheet	-	74LVC2G02 v.9
Modifications:	<ul style="list-style-type: none"> <li>For type number 74LVC2G02GM the SOT code has changed to SOT902-2.</li> </ul>			
74LVC2G02 v.9	20111130	Product data sheet	-	74LVC2G02 v.8
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74LVC2G02 v.8	20101020	Product data sheet	-	74LVC2G02 v.7
74LVC2G02 v.7	20080606	Product data sheet	-	74LVC2G02 v.6
74LVC2G02 v.6	20080222	Product data sheet	-	74LVC2G02 v.5
74LVC2G02 v.5	20070904	Product data sheet	-	74LVC2G02 v.4
74LVC2G02 v.4	20060515	Product data sheet	-	74LVC2G02 v.3
74LVC2G02 v.3	20050201	Product specification	-	74LVC2G02 v.2
74LVC2G02 v.2	20040915	Product specification	-	74LVC2G02 v.1
74LVC2G02 v.1	20031015	Product specification	-	-

## 15 Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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