WINSOURCE ELECTRONICS

THE DATASHEET OF

FDP5500_F085

FAIRCHILD SEMICONDUCTOR®

April 2009

FDP5500_F085

N-Channel UltraFET Power MOSFET

55V, 80A, 7mΩ

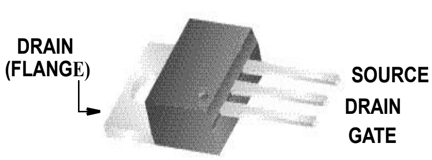
Features

- Typ $r_{DS(on)}$ = 5.1mΩ at V_{GS} = 10V, I_D = 80A
- Typ $Q_{g(10)}$ = 114nC at V_{GS} = 10V
- Simulation Models
  -Temperature Compensated PSPICE and SABER™ Models
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Qualified to AEC Q101
- RoHS Compliant

Applications

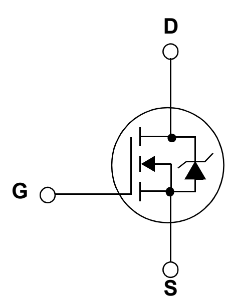
- DC Linear Mode Control
- Solenoid and Motor Control
- Switching Regulators
- Automotive Systems

Package



TO-220AB

Symbol



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage	(Note 1)	55	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20kΩ)	(Note 1)	55	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current Continuous (T_C < 135°C, V_{GS} = 10V)		80	A
	Pulsed		See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	860	mJ
P_D	Power Dissipation		375	W
	Derate above 25°C		2.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
T_L	Max. Lead Temp. for Soldering (at 1.6mm from case for 10sec)		300	
T_{pkg}	Max. Package Temp. for Soldering (Package Body for 10sec)		260	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	0.4	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220AB, 1in^2 copper pad area	62	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP5500	FDP5500_F085	TO-220AB	Tube	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		55	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 45V	T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		2	2.8	4	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 80A, V_{GS}= 10V		-	5.1	7	mΩ
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3565	-	pF
C_{oss}	Output Capacitance			-	1310	-	pF
C_{rss}	Reverse Transfer Capacitance			-	395	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 20V	V_{GS} = 0 to 20V	V_{DD} = 30V I_D = 80A R_L = 0.4Ω I_g = 1.0mA	-	207	269	nC
$Q_{g(10)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V		-	114	148	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	6.6	8.6	nC
Q_{gs}	Gate to Source Gate Charge			-	17.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	52	-	nC

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 30V$, $I_D = 80A$, $R_L = 0.4\Omega$, $V_{GS} = 10V$, $R_{GS} = 2.5\Omega$	-	-	75	ns
$t_{d(on)}$	Turn-On Delay Time		-	12	-	ns
t_r	Rise Time		-	34	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	37	-	ns
t_f	Fall Time		-	23	-	ns
t_{off}	Turn-Off Time		-	-	96	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80A$	-	0.9	1.25	V
t_{rr}	Reverse Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$	-	58	75	ns
Q_{rr}	Reverse Recovery Charge		-	71	92	nC

Notes:

1: Starting $T_J = 25^oC$ to175^oC.

2: Starting $T_J = 25^oC$, L = 0.42mH, I_{AS} = 64A

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

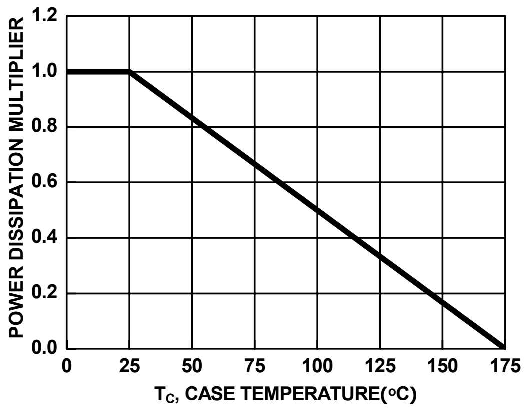


Figure 1. Normalized Power Dissipation vs Case Temperature

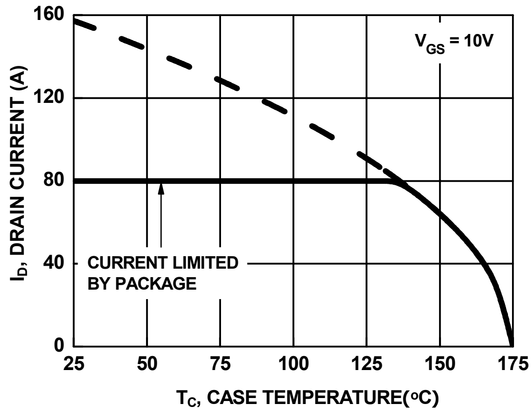


Figure 2. Maximum Continuous Drain Current vs Case Temperature

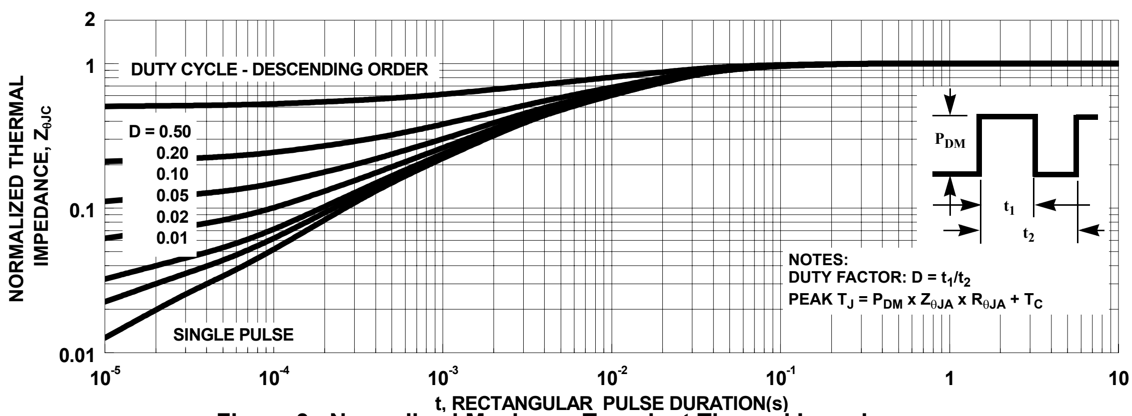


Figure 3. Normalized Maximum Transient Thermal Impedance

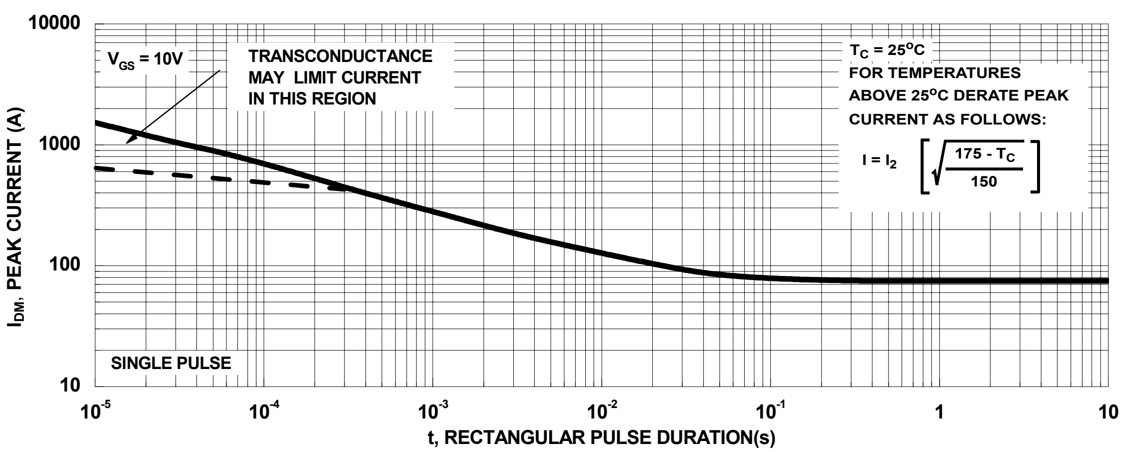


Figure 4. Peak Current Capability

Typical Characteristics

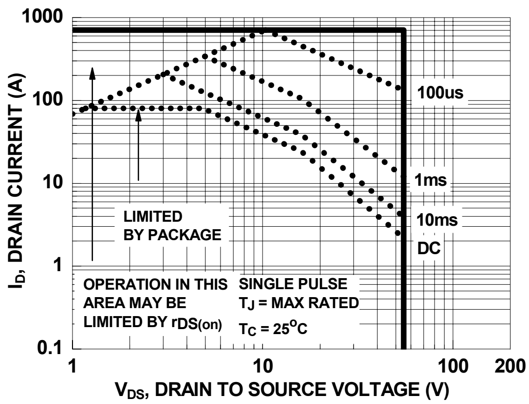
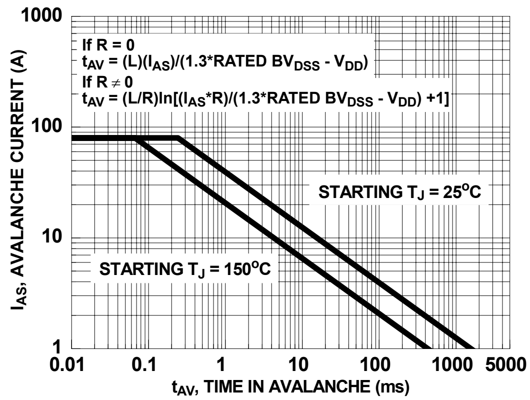


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

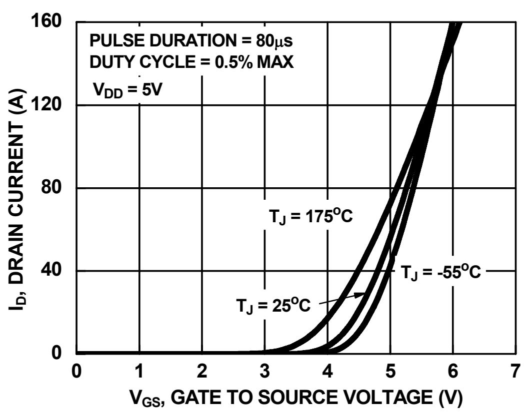


Figure 7. Transfer Characteristics

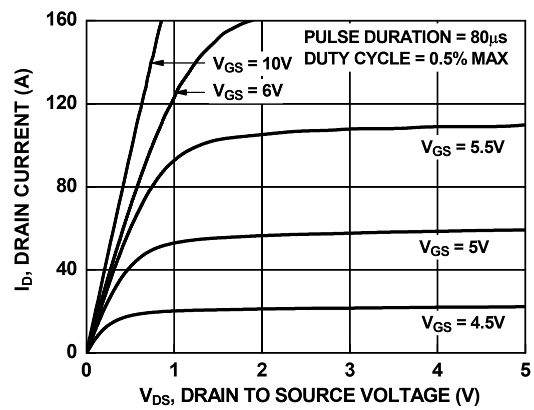


Figure 8. Saturation Characteristics

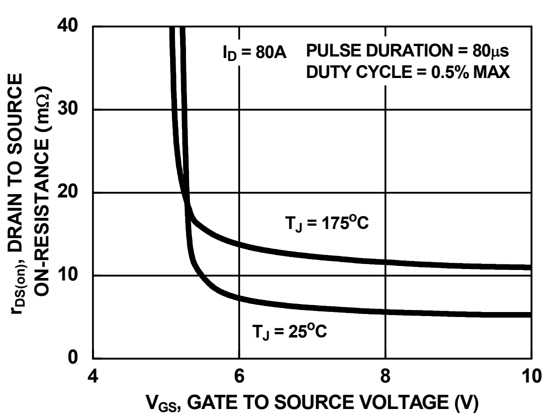


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

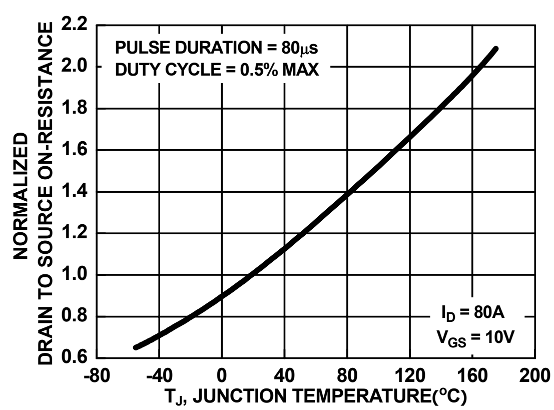


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

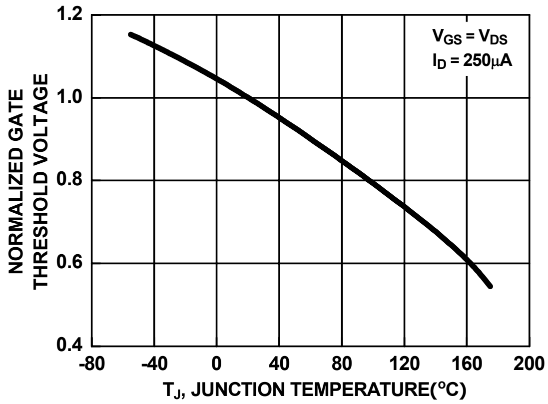


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

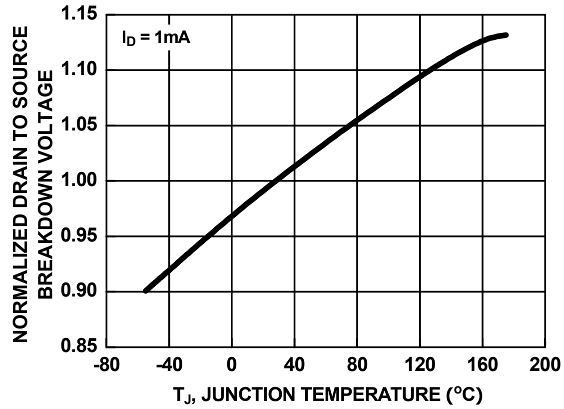


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

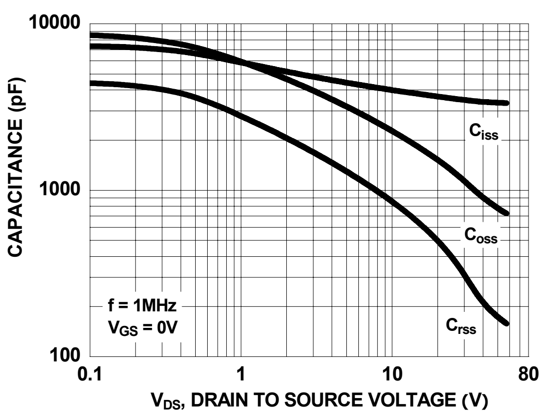


Figure 13. Capacitance vs Drain to Source Voltage

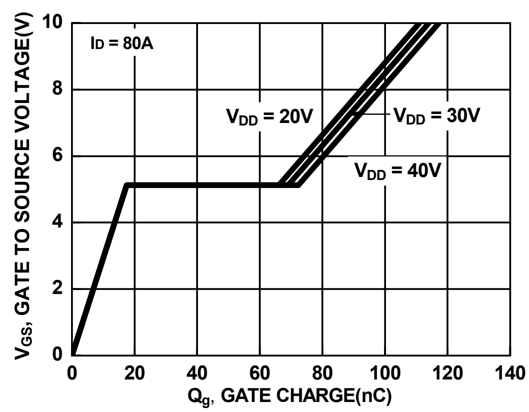


Figure 14. Gate Charge vs Gate to Source Voltage

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