



**THE DATASHEET OF  
PH20100S,115**





# PH20100S

## N-channel TrenchMOS standard level FET

Rev. 03 — 2 February 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Simple gate drive required due to low gate charge current
- Low conduction losses due to low on-state resistance

### 1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

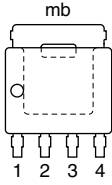
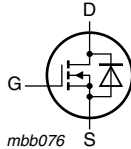
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> ; see <a href="#">Figure 1</a>	-	-	34.3	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	62.5	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 20\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>	-	8.9	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	19	23	m $\Omega$

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LFAK)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

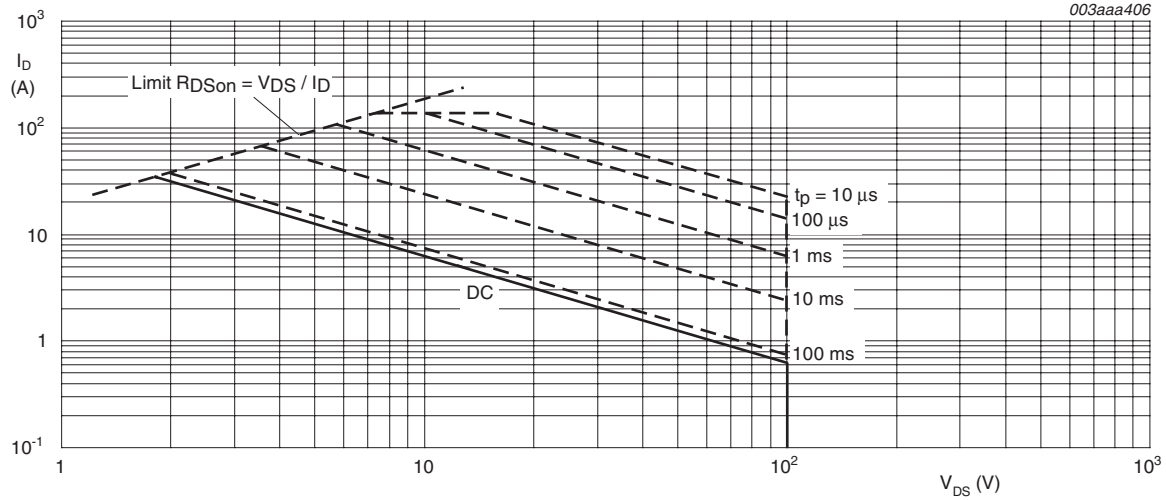
Type number	Package		Version
	Name	Description	
PH20100S	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

## 4. Limiting values

Table 4. Limiting values

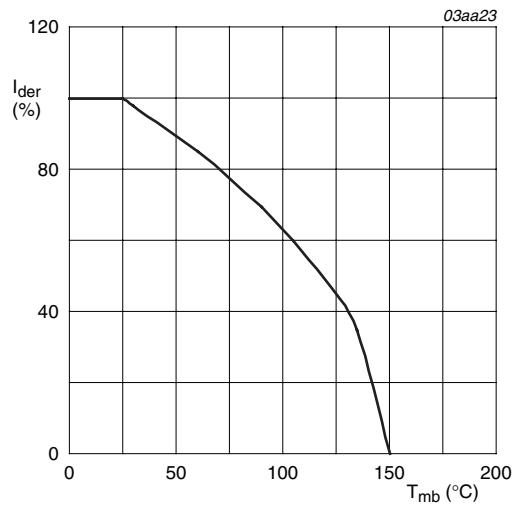
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 2</a>	-	21.6	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a> ; see <a href="#">Figure 1</a>	-	34.3	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	137	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	62.5	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	137	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 12\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; unclamped; $t_p = 0.3\text{ ms}$	-	250	mJ



$T_{mb} = 25^{\circ}\text{C}; I_{DM}$  is single pulse;  $V_{GS} = 10\text{V}$

Fig 1. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



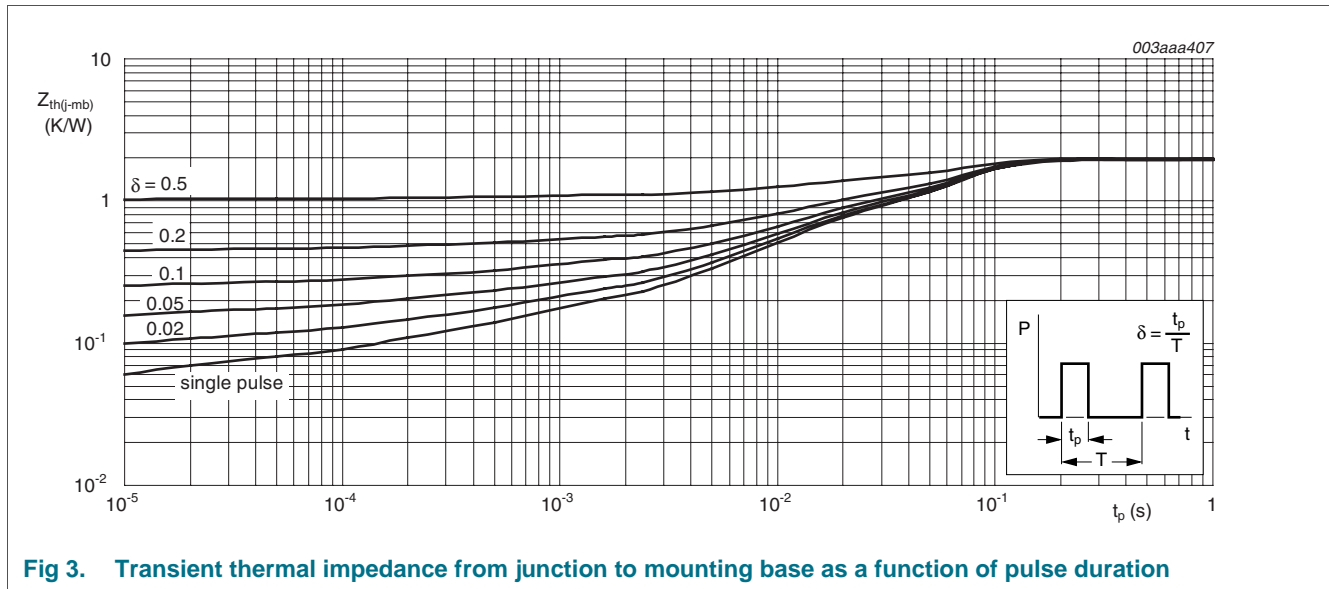
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 3</a>	-	-	2	K/W

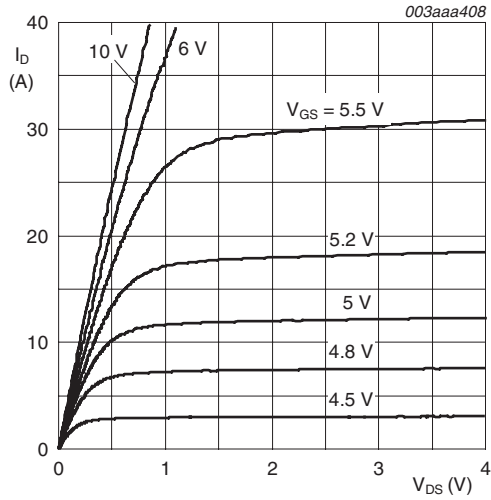


**Fig 3. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

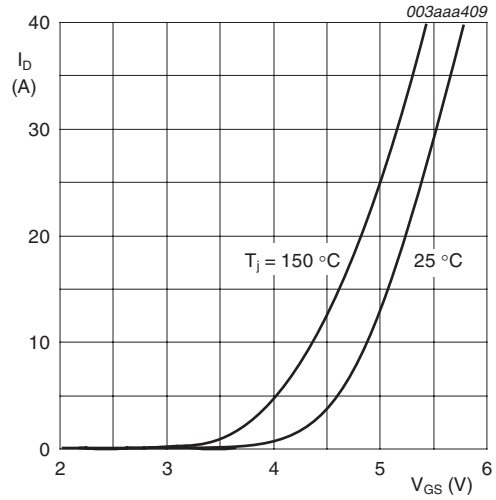
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 1 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a>	1.2	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.06	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	43	53	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	19	23	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 20 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	39	-	nC
$Q_{GS}$	gate-source charge		-	6.9	-	nC
$Q_{GD}$	gate-drain charge		-	8.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	2264	-	pF
$C_{oss}$	output capacitance		-	290	-	pF
$C_{rss}$	reverse transfer capacitance		-	111	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 5 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	23	-	ns
$t_r$	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	47	-	ns
$t_f$	fall time		-	9.3	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	110	-	ns



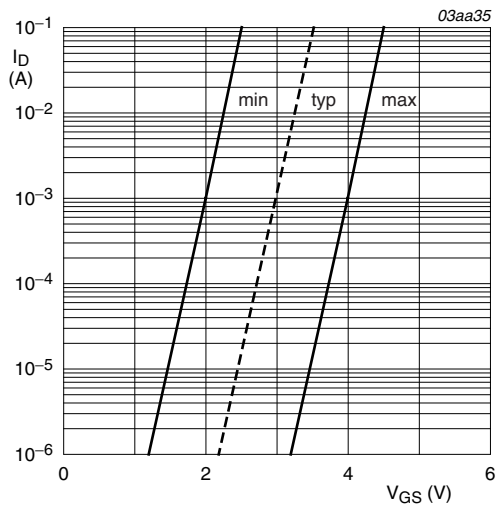
$T_j = 25^\circ\text{C}$

**Fig 4. Output characteristics: drain current as a function of drain-source voltage; typical values**



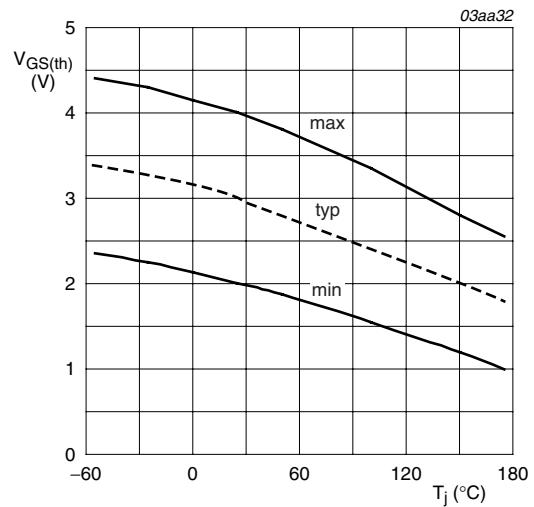
$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

**Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



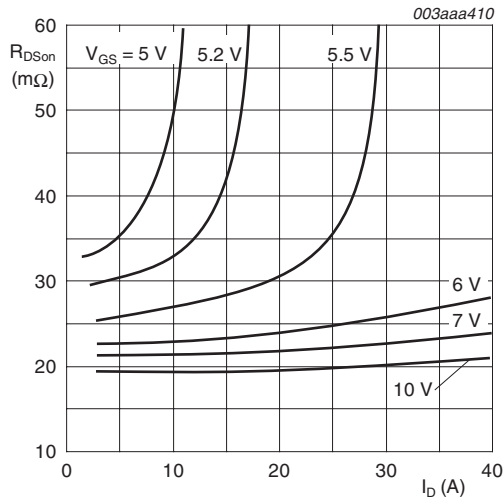
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

**Fig 6. Sub-threshold drain current as a function of gate-source voltage**



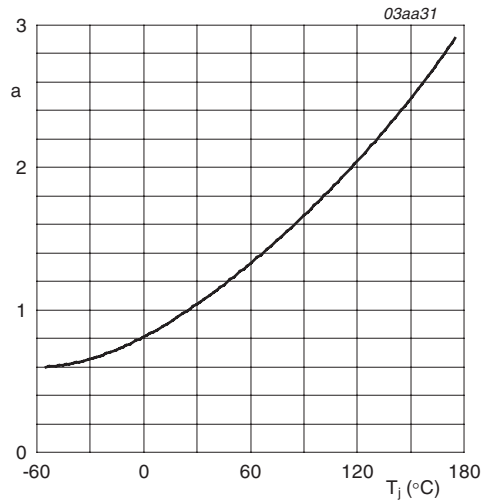
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

**Fig 7. Gate-source threshold voltage as a function of junction temperature**



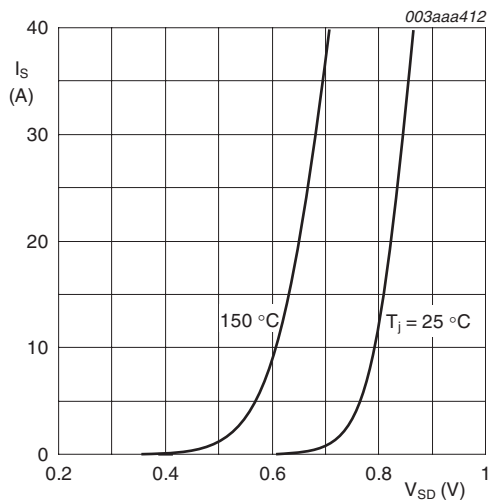
$T_j = 25^\circ\text{C}$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**



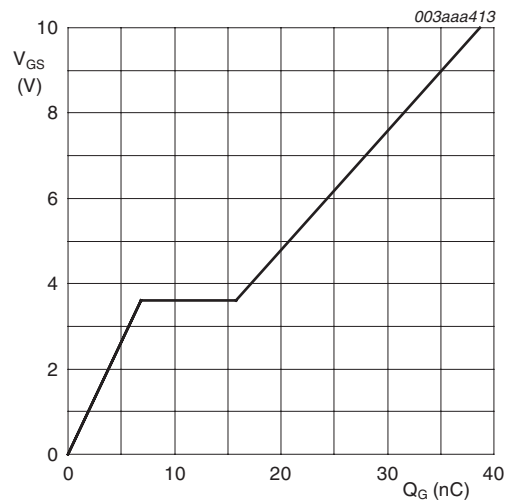
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature**



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}; V_{GS} = 0\text{V}$

**Fig 10. Source current as a function of source-drain voltage; typical values**



$I_D = 20\text{A}; V_{DS} = 50\text{V}$

**Fig 11. Gate-source voltage as a function of gate charge; typical values**

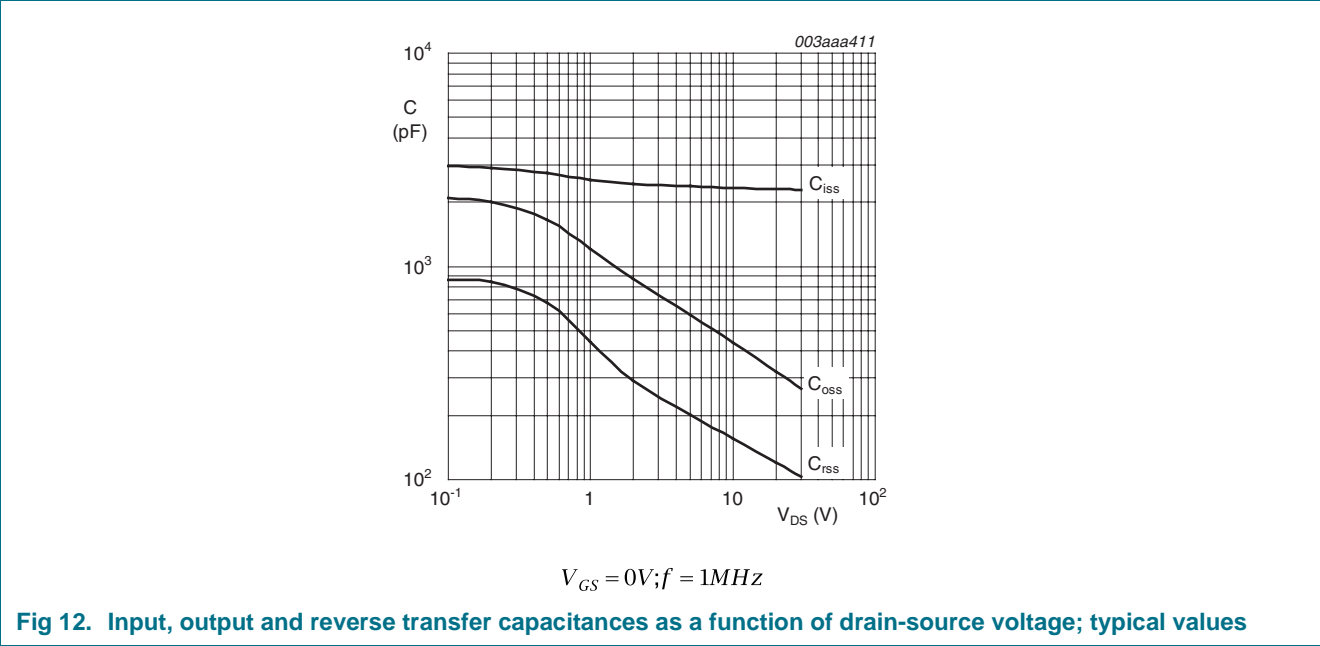
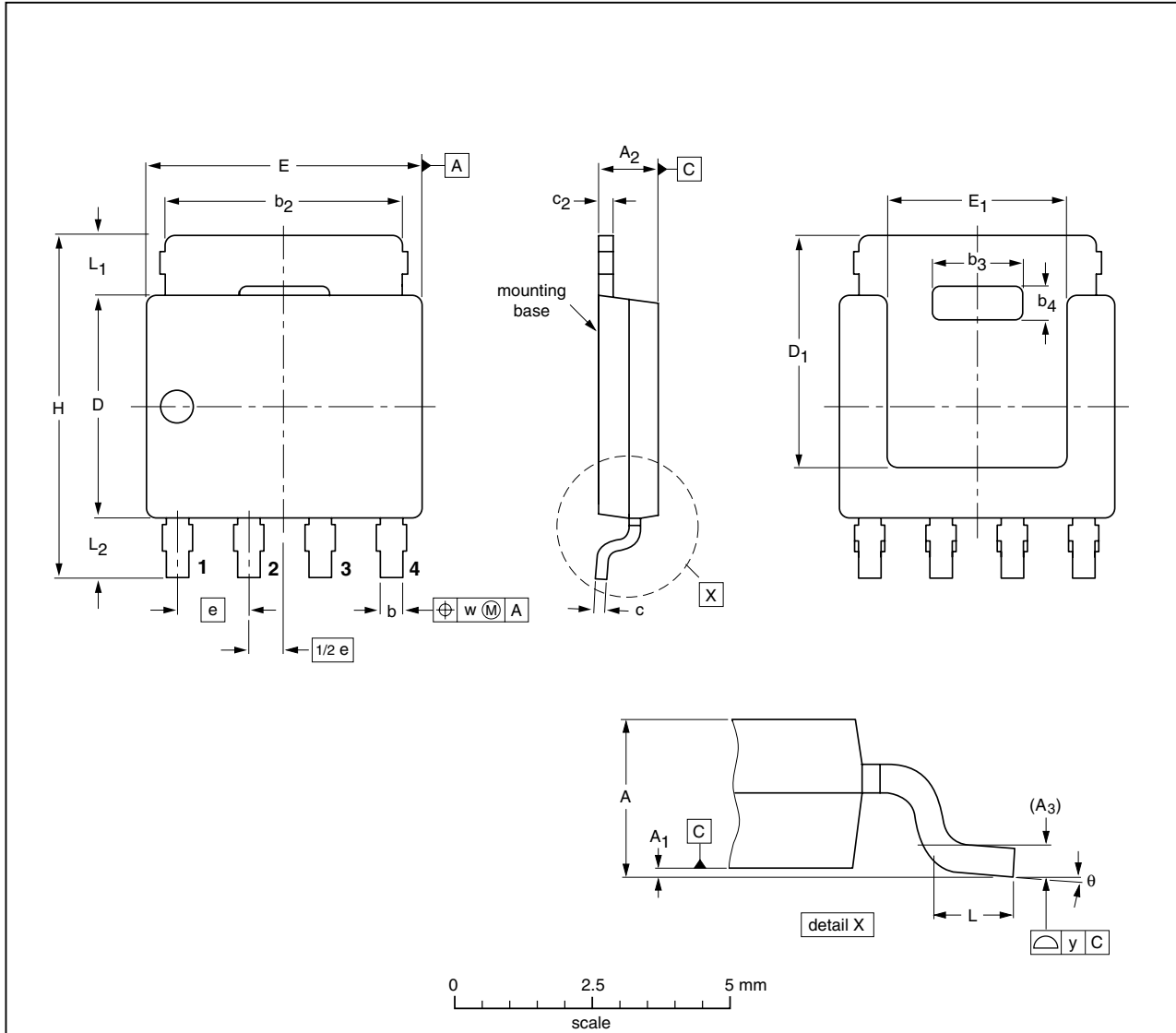


Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPACK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1) max</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				04-10-13 06-03-16

Fig 13. Package outline SOT669 (LFPACK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH20100S_3	20090202	Product data sheet	-	PH20100S_2
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>		
PH20100S_2 (9397 750 13698)	20040817	Product data sheet	-	PH20100S_1
PH20100S_1 (9397 750 12815)	20040305	Preliminary data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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