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August 2014

# FCD5N60 / FCU5N60

## N-Channel SuperFET<sup>®</sup> MOSFET

600 V, 4.6 A, 950 mΩ

### Features

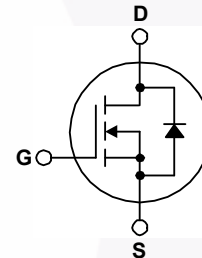
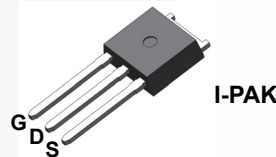
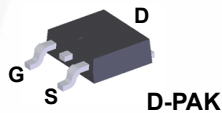
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 810\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 16\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 32\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Application

- LCD/LED TV and Monitor
- Lighting
- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET<sup>®</sup> MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD5N60TM FCD5N60TM_WS FCU5N60TU	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	4.6
		- Continuous ( $T_C = 100^\circ\text{C}$ )	2.9
$I_{DM}$	Drain Current	- Pulsed (Note 1)	13.8
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	159	mJ
$I_{AR}$	Avalanche Current (Note 1)	4.6	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	54
		- Derate Above $25^\circ\text{C}$	0.43
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCD5N60TM FCD5N60TM_WS FCU5N60TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

FCD5N60 / FCU5N60 — N-Channel SuperFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD5N60TM	FCD5N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCD5N60TM_WS	FCD5N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCU5N60TU	FCU5N60	IPAK	Tube	N/A	N/A	75 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.6	-	$\text{V}/^\circ\text{C}$
$BV_{DS}$	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 4.6\text{ A}$	-	700	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2.3\text{ A}$	-	0.81	0.95	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.3\text{ A}$	-	3.8	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	470	600	pF
$C_{oss}$	Output Capacitance		-	250	320	pF
$C_{rss}$	Reverse Transfer Capacitance		-	22	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	12	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	32	-	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 4.6\text{ A}, V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	-	12	30	ns
$t_r$	Turn-On Rise Time		-	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		-	47	95	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	22	55
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480\text{ V}, I_D = 4.6\text{ A}, V_{GS} = 10\text{ V}$	-	16	-	nC
$Q_{gs}$	Gate to Source Gate Charge		-	2.8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	7	-

### Drain-Source Diode Characteristics

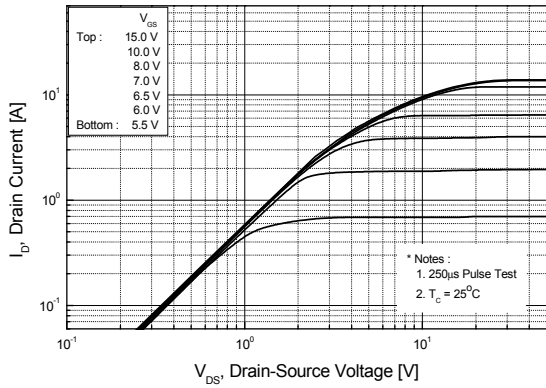
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	4.6	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	13.8	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 4.6\text{ A}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 4.6\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	295	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	2.7	-	$\mu\text{C}$

#### Notes:

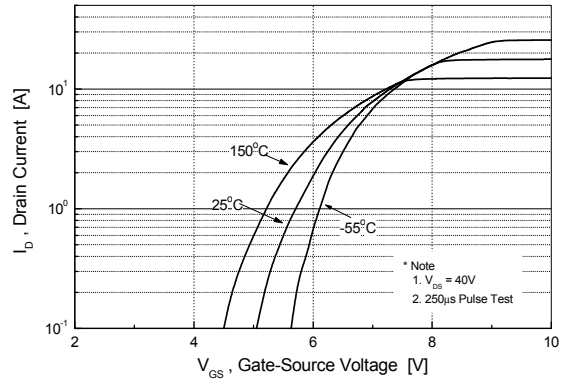
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 2.3\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 4.6\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

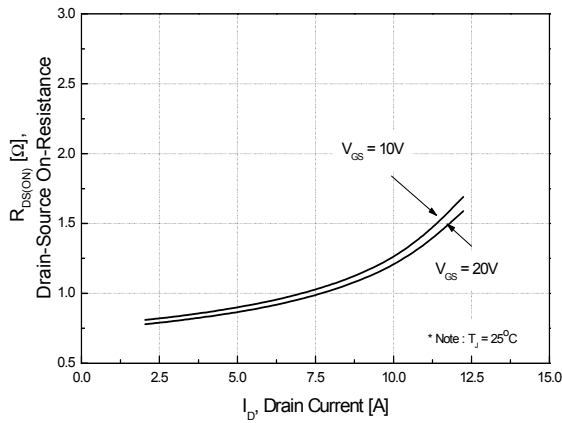
**Figure 1. On-Region Characteristics**



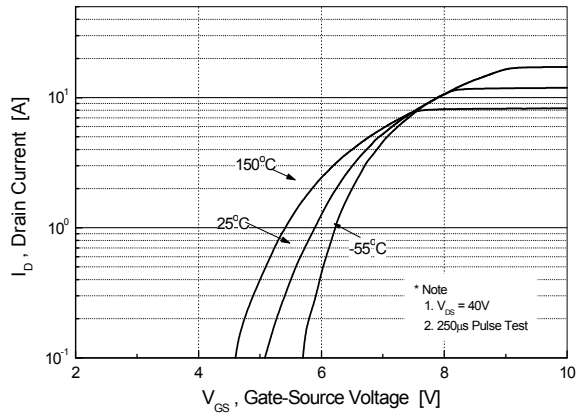
**Figure 2. Transfer Characteristics**



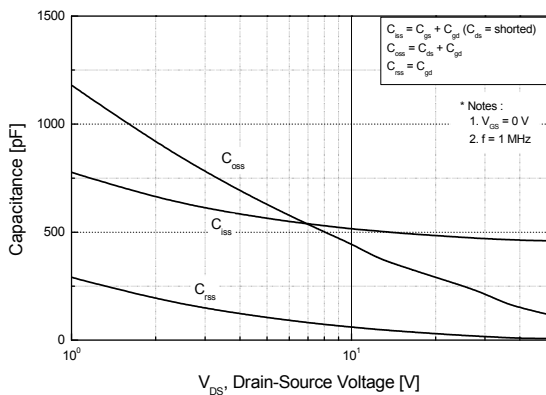
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



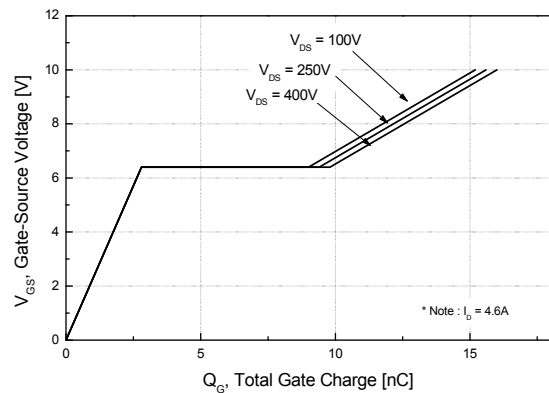
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

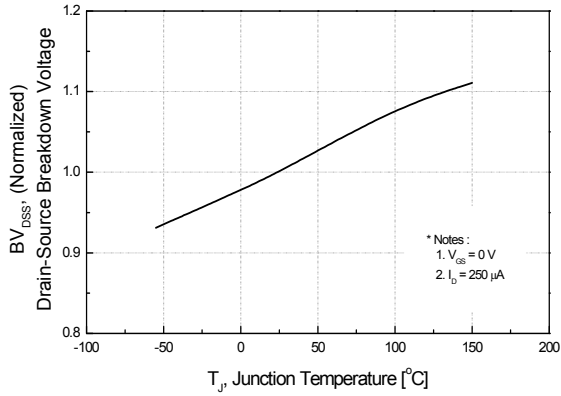


**Figure 6. Gate Charge Characteristics**

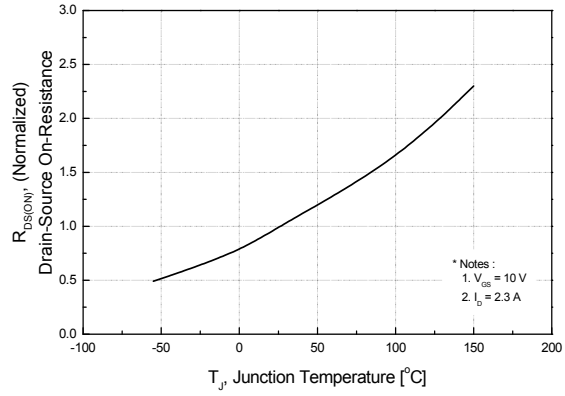


## Typical Performance Characteristics (Continued)

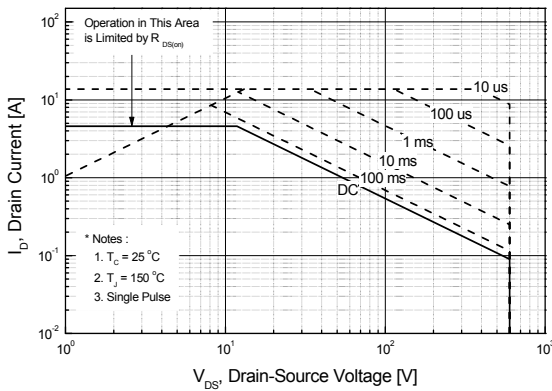
**Figure 7. Breakdown Voltage Variation vs. Temperature**



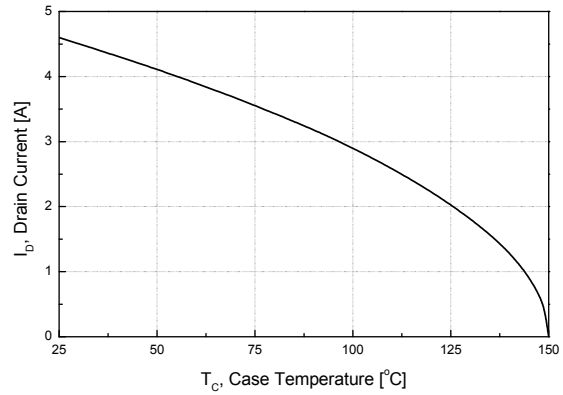
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

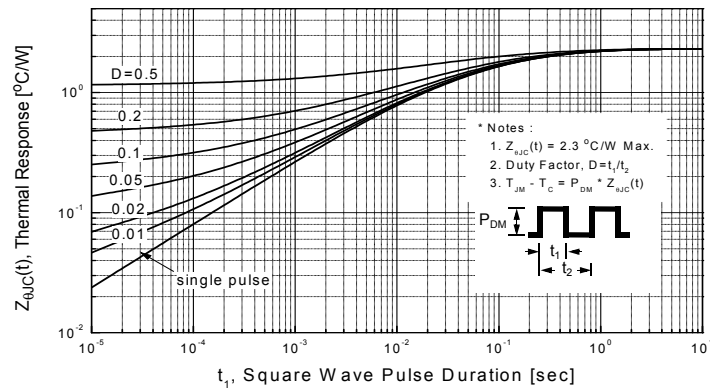




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

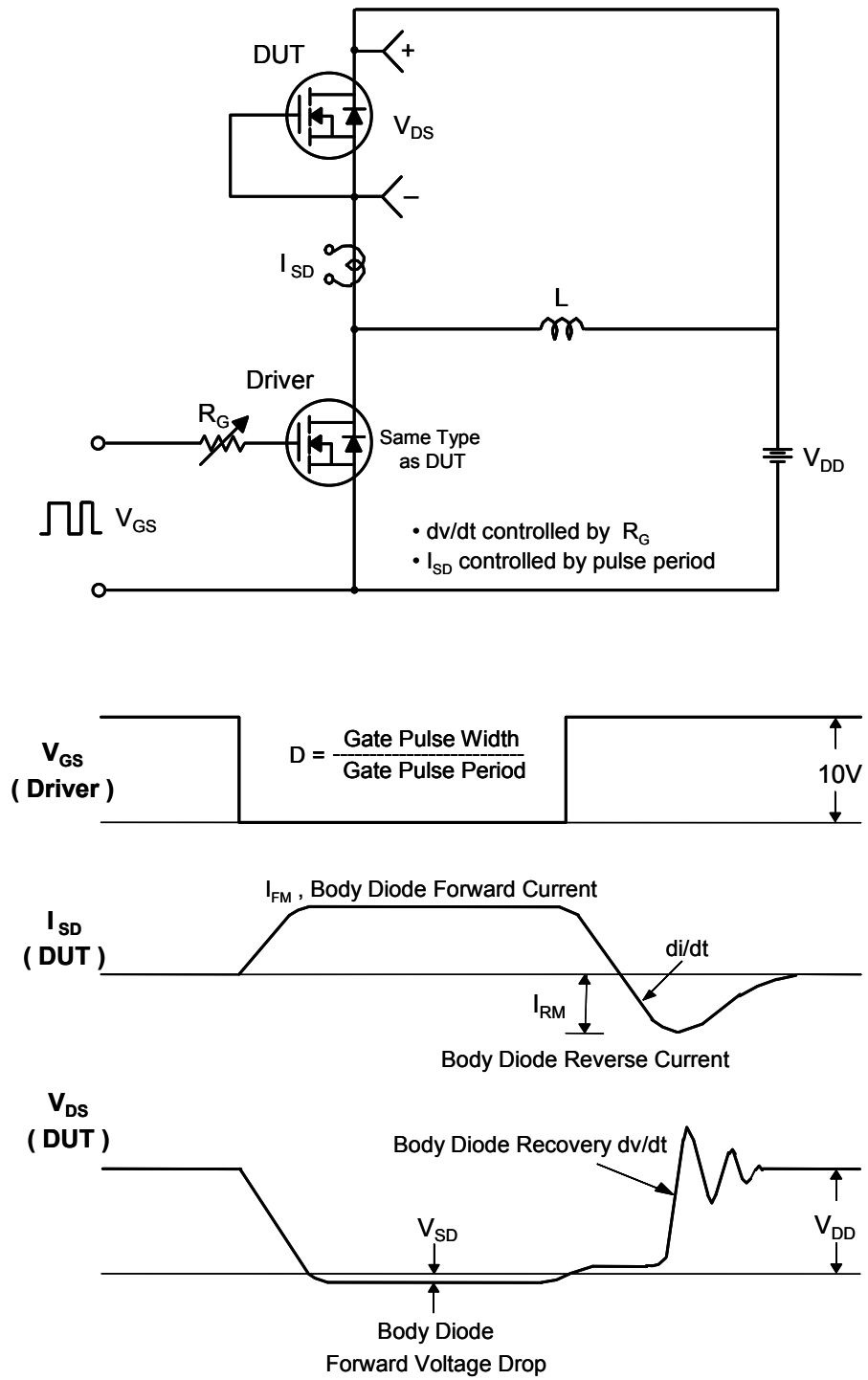


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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