

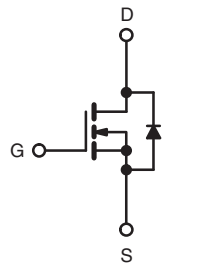
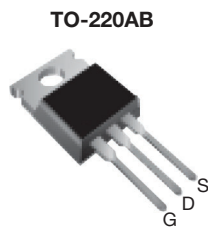


THE DATASHEET OF IRFZ44RSTRR



Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.028
Q_g (Max.) (nC)	67	
Q_{gs} (nC)	18	
Q_{gd} (nC)	25	
Configuration	Single	



N-Channel MOSFET

FEATURES

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dV/dt Rating
- 175 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Drop in Replacement of the IRFZ44, SiHFZ44 for Linear/Audio Applications
- Compliant to RoHS Directive 2002/95/EC


RoHS*
 COMPLIANT

DESCRIPTION

Advanced Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFZ44RPbF
	SiHFZ44R-E3
SnPb	IRFZ44R
	SiHFZ44R



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	60	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ^e	V_{GS} at 10 V	I_D	$T_C = 25$ °C	50	A
Continuous Drain Current			$T_C = 100$ °C	36	
Pulsed Drain Current ^a		I_{DM}	200		
Linear Derating Factor			1.0	W/°C	
Single Pulse Avalanche Energy ^b		E_{AS}	100	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	150	W	
Peak Diode Recovery dV/dt^c		dV/dt	4.5	V/ns	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature) ^d	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 44$ μ H, $R_g = 25$ Ω , $I_{AS} = 51$ A (see fig. 12).
- $I_{SD} \leq 51$ A, $dV/dt \leq 250$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.
- Current limited by the package, (die current = 51 A).

* Pb containing terminations are not RoHS compliant, exemptions may apply

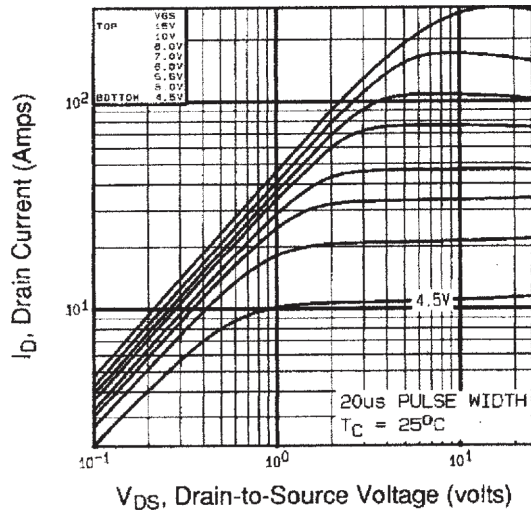
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 31\text{ A}^b$	-	-	0.028	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 31\text{ A}^b$	15	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	1900	-	pF
Output Capacitance	C_{oss}		-	920	-	
Reverse Transfer Capacitance	C_{rss}		-	170	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 51\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b	-	-	67	nC
Gate-Source Charge	Q_{gs}		-	-	18	
Gate-Drain Charge	Q_{gd}		-	-	25	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $I_D = 51\text{ A}$, $R_g = 9.1\text{ }\Omega$, $R_D = 0.55\text{ }\Omega$, see fig. 10 ^b	-	14	-	ns
Rise Time	t_r		-	110	-	
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	
Fall Time	t_f		-	92	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	50 ^c	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	200	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 51\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 51\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}^b$	-	120	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.53	0.80	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

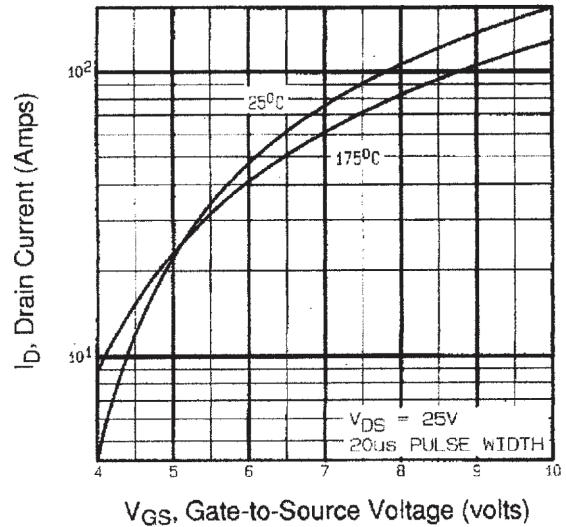
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Current limited by the package (die current = 51 A).

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



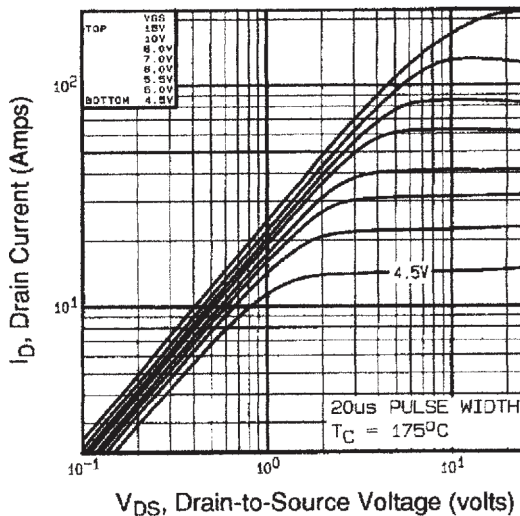
V_{DS} , Drain-to-Source Voltage (volts)

Fig. 1 - Typical Output Characteristics



V_{GS} , Gate-to-Source Voltage (volts)

Fig. 3 - Typical Transfer Characteristics



V_{DS} , Drain-to-Source Voltage (volts)

Fig. 2 - Typical Output Characteristics

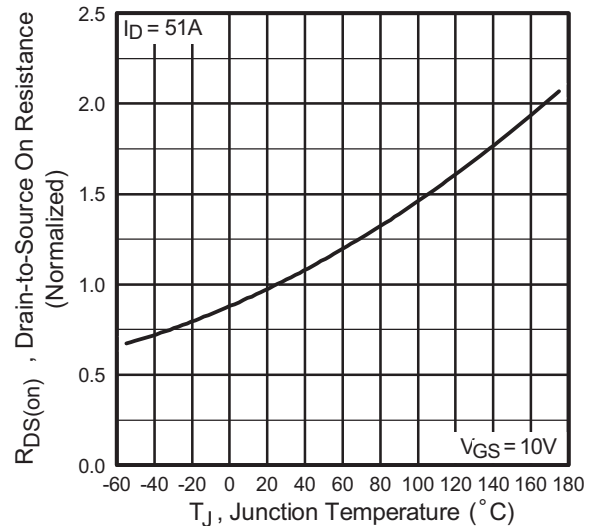


Fig. 4 - Normalized On-Resistance vs. Temperature

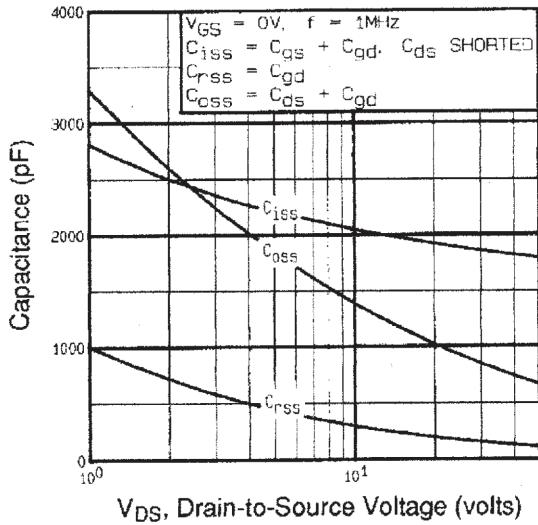


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

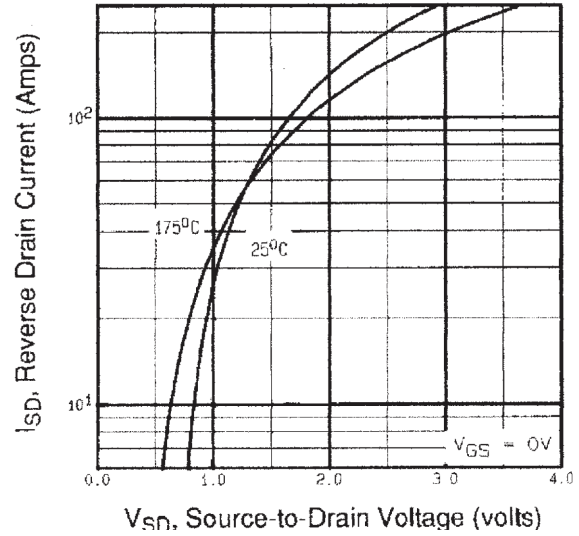


Fig. 7 - Typical Source-Drain Diode Forward Voltage

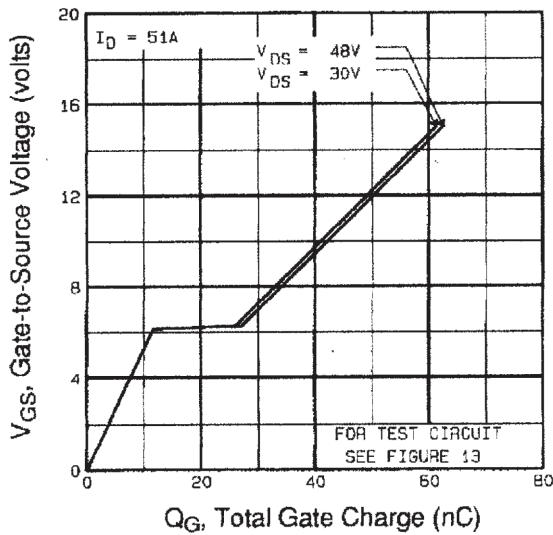


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

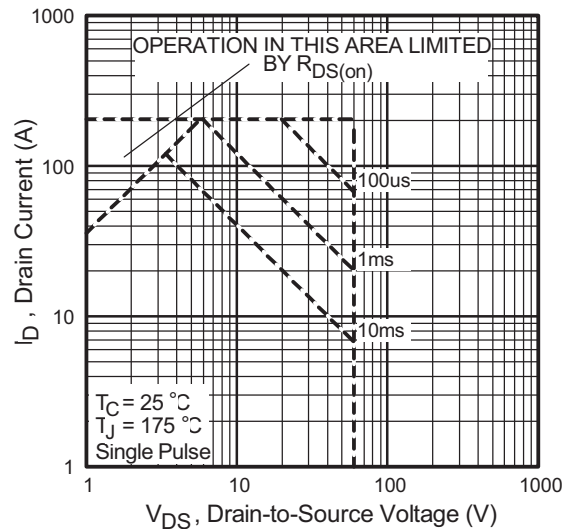


Fig. 8 - Maximum Safe Operating Area

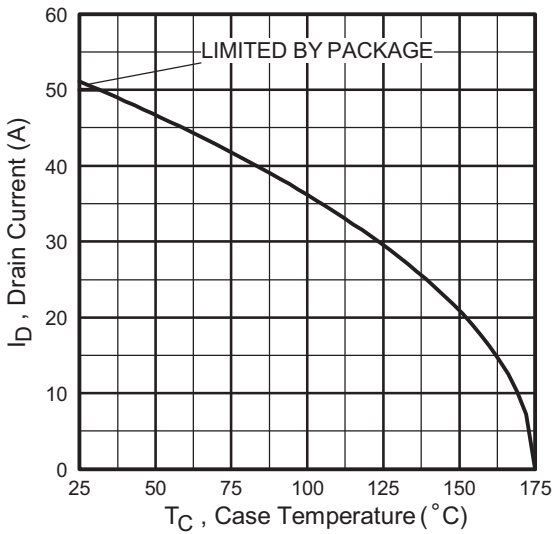


Fig. 9 - Maximum Drain Current vs. Case Temperature

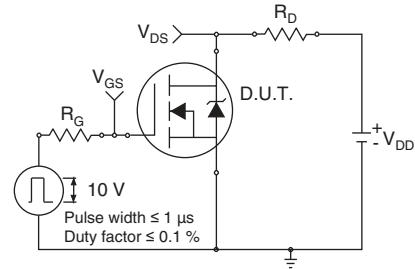


Fig. 10a - Switching Time Test Circuit

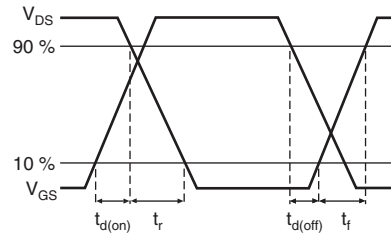


Fig. 10b - Switching Time Waveforms

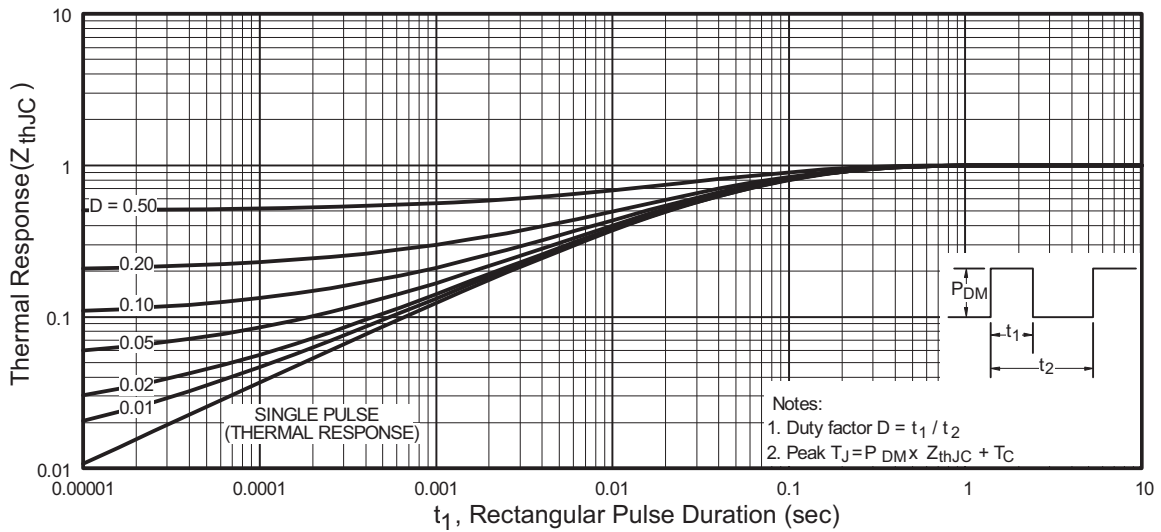


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

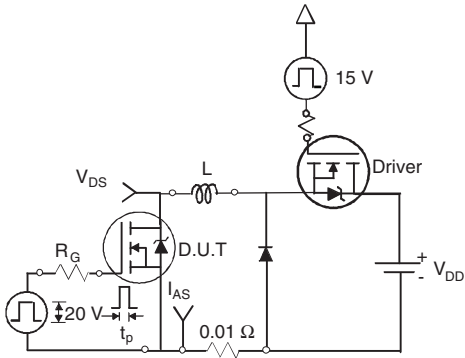


Fig. 12a - Unclamped Inductive Test Circuit

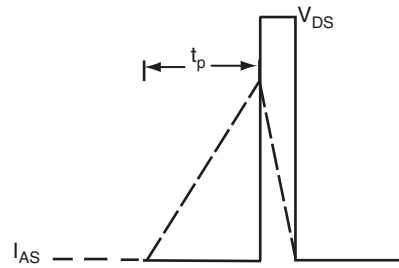


Fig. 12b - Unclamped Inductive Waveforms

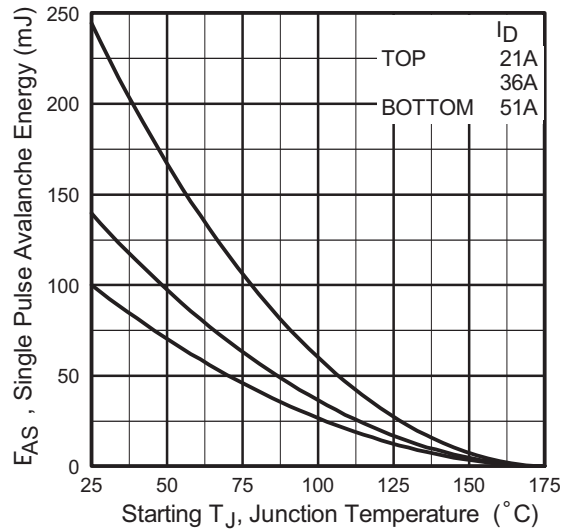


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

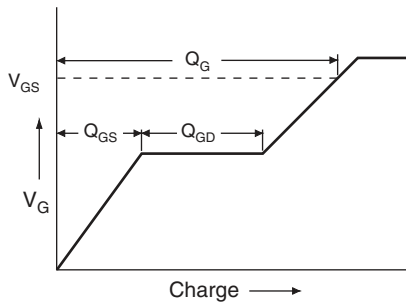


Fig. 13a - Basic Gate Charge Waveform

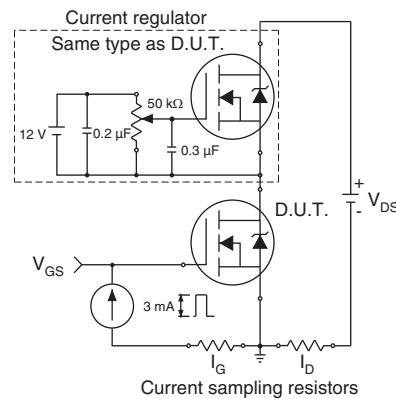
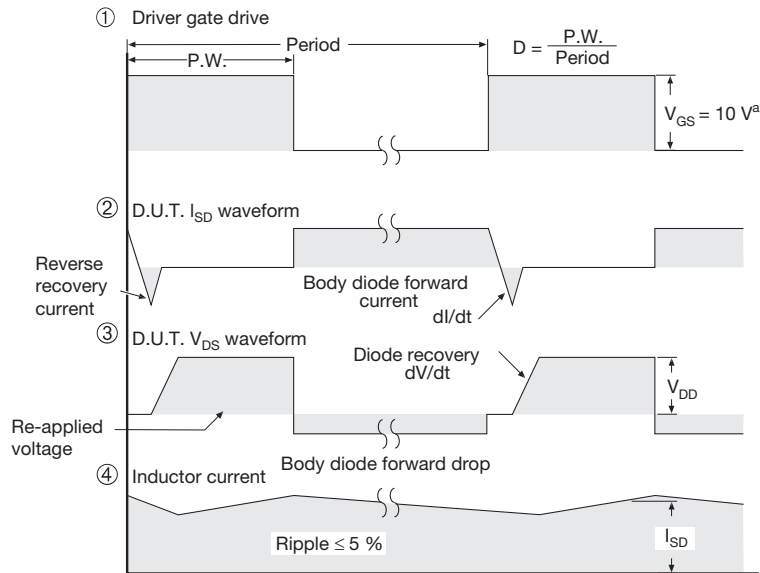
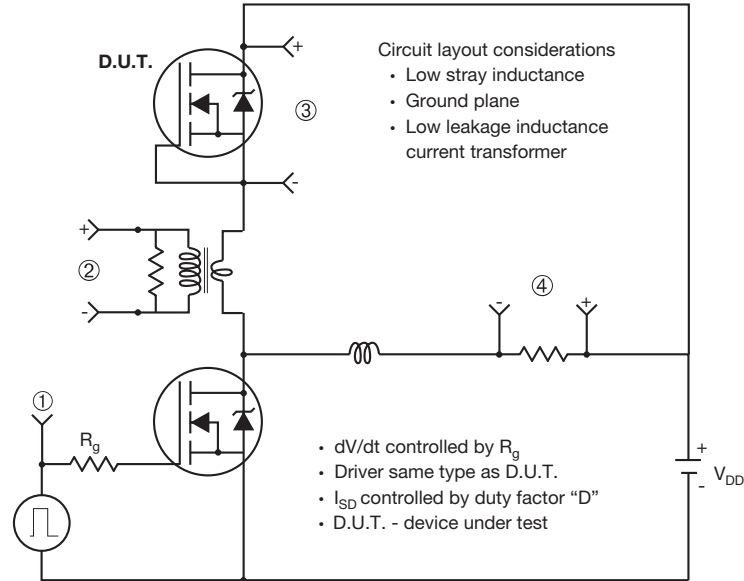


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



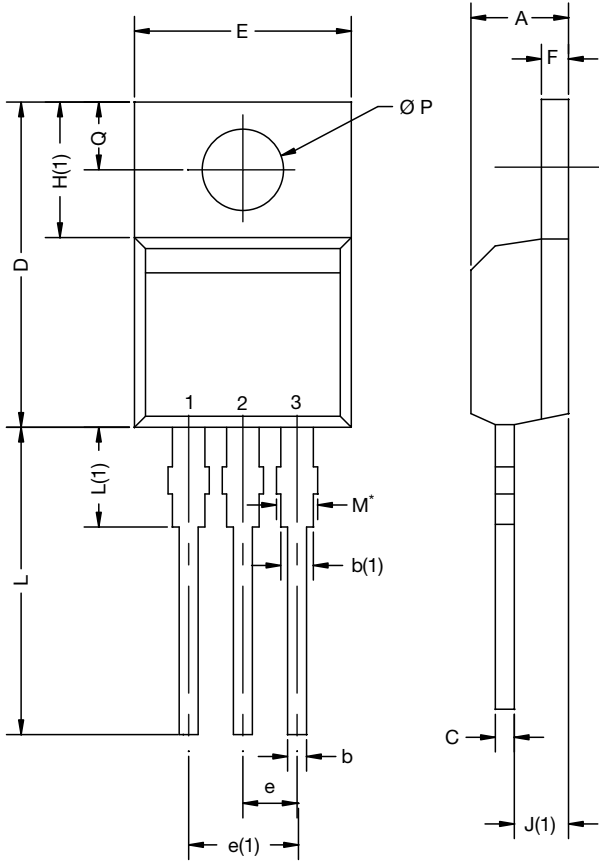
Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM





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