



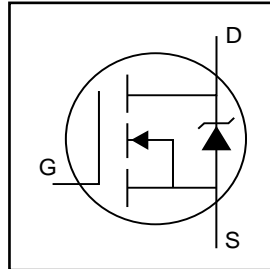
**THE DATASHEET OF  
IRL3303STRR**



# IRL3303S/L

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRL3303S)
- Low-profile through-hole (IRL3303L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



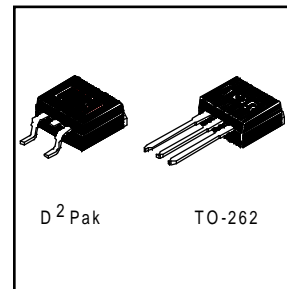
$V_{DS} = 30V$
$R_{DS(on)} = 0.026\Omega$
$I_D = 38A$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRL3303L) is available for low-profile applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	38	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	27	
$I_{DM}$	Pulsed Drain Current ①⑤	140	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
$V_{GS}$	Gate-to-Source Voltage	±16	V
$E_{AS}$	Single Pulse Avalanche Energy ②⑤	130	mJ
$I_{AR}$	Avalanche Current ①	20	A
$E_{AR}$	Repetitive Avalanche Energy ①	6.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

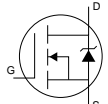
## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted,steady-state)**	—	40	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.026	$\Omega$	$V_{GS} = 10V, I_D = 20A$ ④
		—	—	0.040		$V_{GS} = 4.5V, I_D = 17A$ ④ $T_J = 150^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	12	—	—	S	$V_{DS} = 25V, I_D = 20A$ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
$Q_g$	Total Gate Charge	—	—	26	nC	$I_D = 20A$
$Q_{gs}$	Gate-to-Source Charge	—	—	8.8		$V_{DS} = 24V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	15		$V_{GS} = 4.5V$ , See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	7.4	—		$V_{DD} = 15V$
$t_r$	Rise Time	—	200	—	$I_D = 20A$ $R_G = 6.5\Omega$ $R_D = 0.7\Omega$ , See Fig. 10 ④⑤	
$t_{d(off)}$	Turn-Off Delay Time	—	14	—		
$t_f$	Fall Time	—	36	—		
$L_S$	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
$C_{iss}$	Input Capacitance	—	870	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	340	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	170	—		$f = 1.0\text{MHz}$ , See Fig. 5⑤

## Source-Drain Ratings and Characteristics

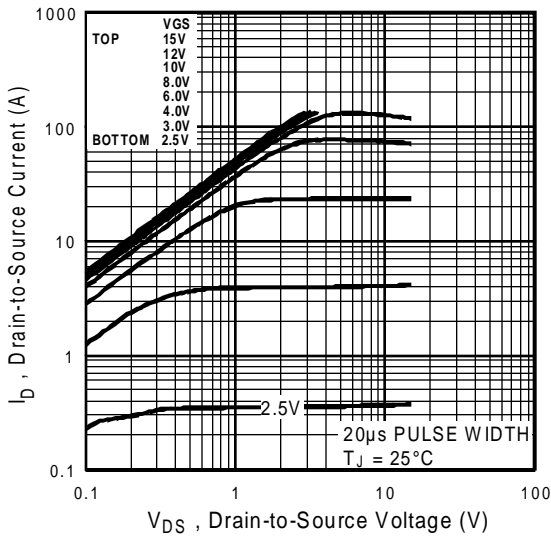
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	140		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	72	110	ns	$T_J = 25^\circ\text{C}, I_F = 20A$
$Q_{rr}$	Reverse Recovery Charge	—	180	280	$\mu\text{C}$	$di/dt = 100A/\mu\text{s}$ ④⑤
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

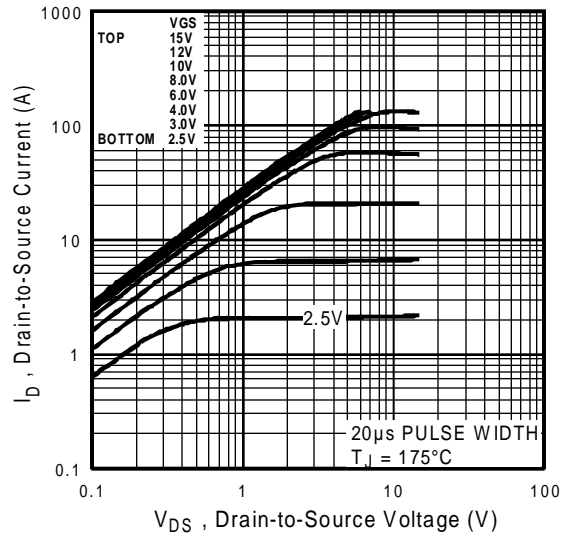
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{DD} = 15V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 470\mu\text{H}$   
 $R_G = 25\Omega, I_{AS} = 20A$ . (See Figure 12)
- ③  $I_{SD} \leq 20A, di/dt \leq 140A/\mu\text{s}, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤ Uses IRL3303 data and test conditions.

\*\* When mounted on 1" square PCB ( FR-4 or G-10 Material ).

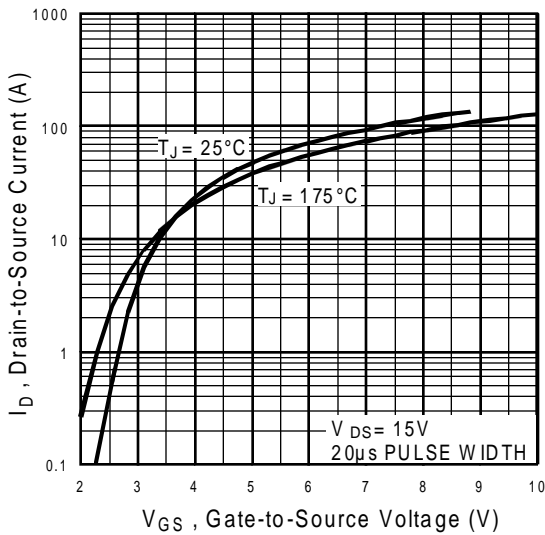
For recommended footprint and soldering techniques refer to application note #AN-994.



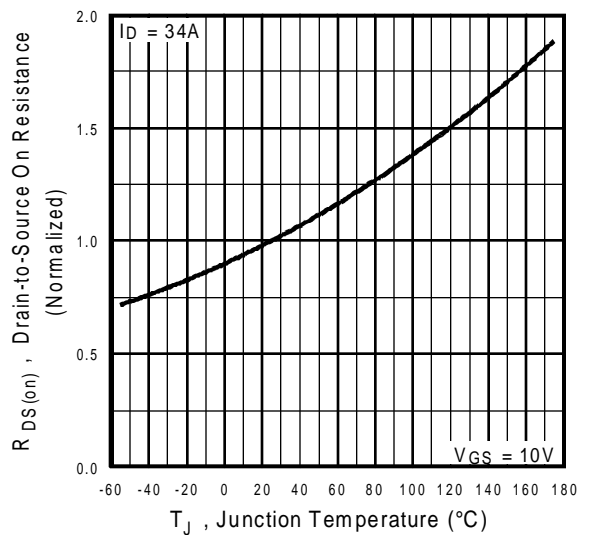
**Fig 1.** Typical Output Characteristics



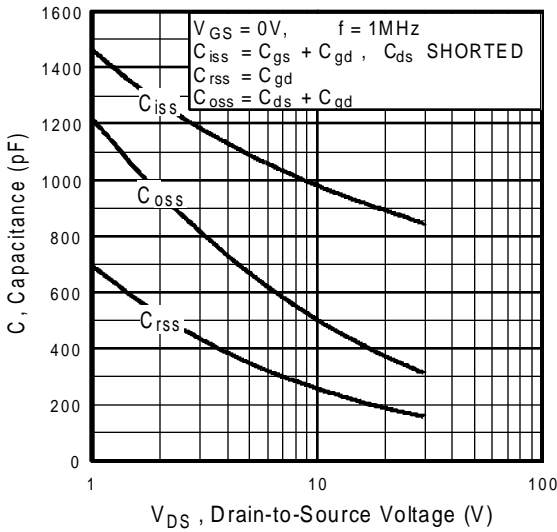
**Fig 2.** Typical Output Characteristics



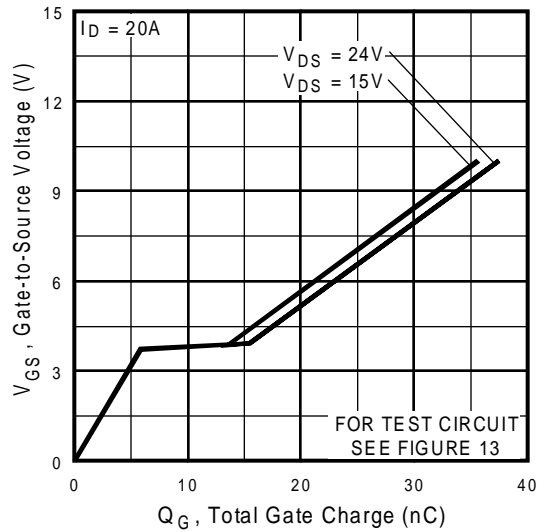
**Fig 3.** Typical Transfer Characteristics



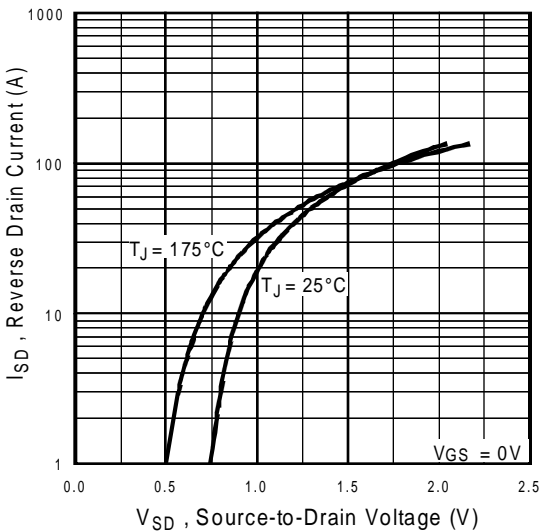
**Fig 4.** Normalized On-Resistance Vs. Temperature



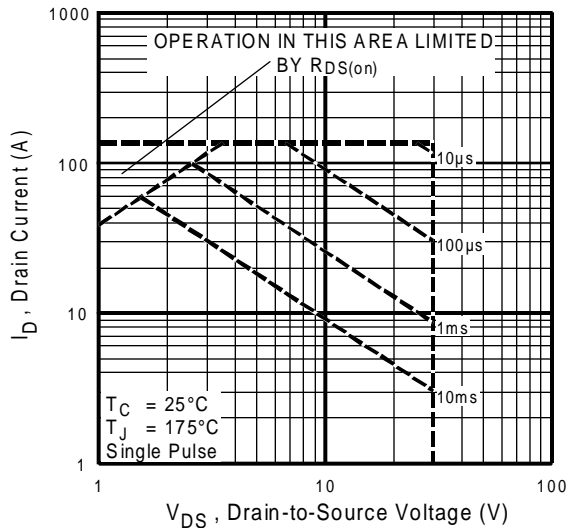
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



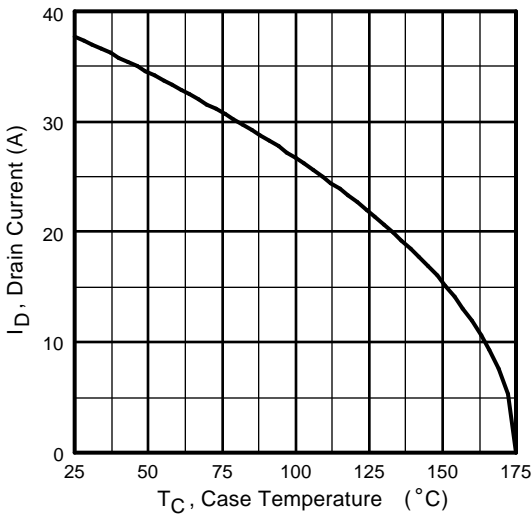
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



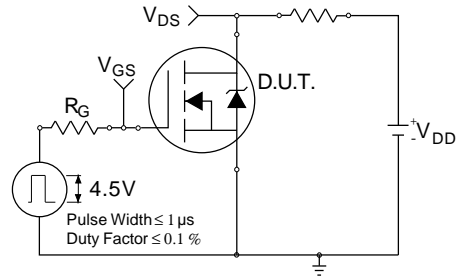
**Fig 7.** Typical Source-Drain Diode Forward Voltage



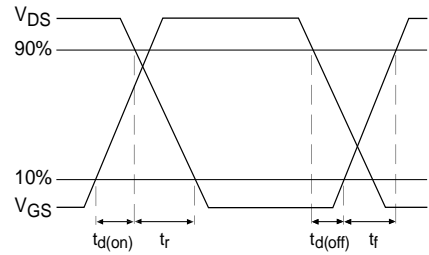
**Fig 8.** Maximum Safe Operating Area



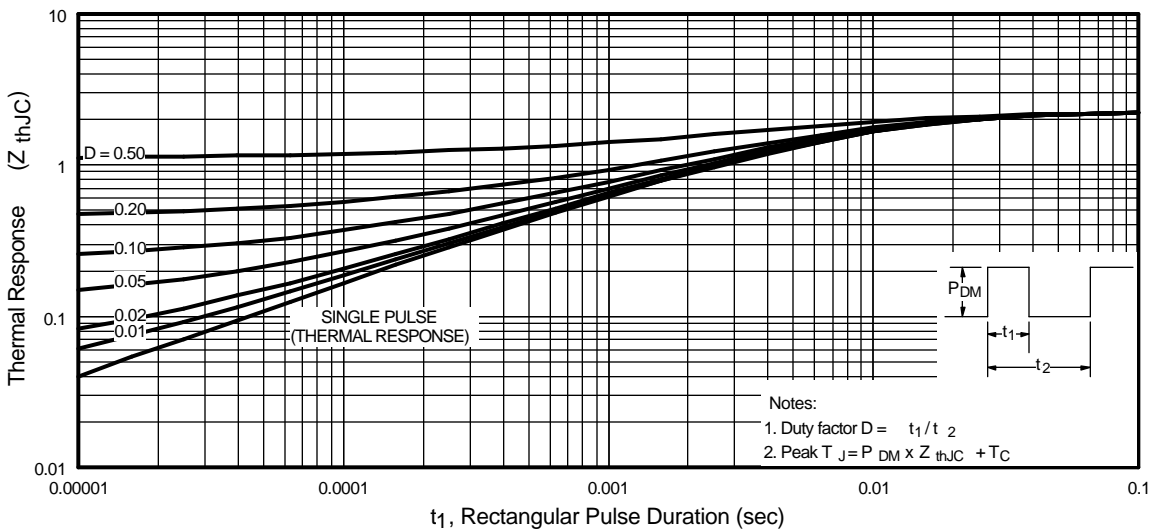
**Fig 9.** Maximum Drain Current vs. Case Temperature



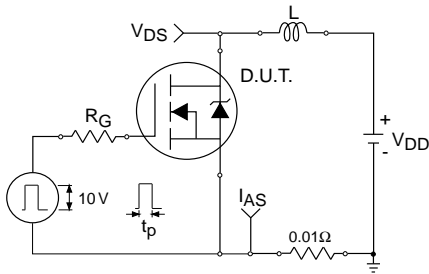
**Fig 10a.** Switching Time Test Circuit



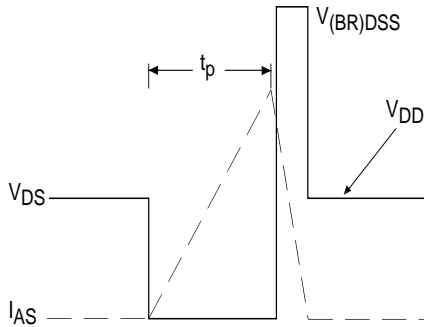
**Fig 10b.** Switching Time Waveforms



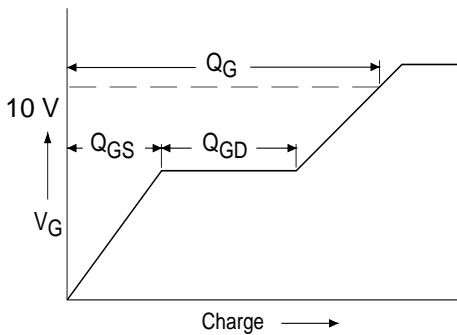
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



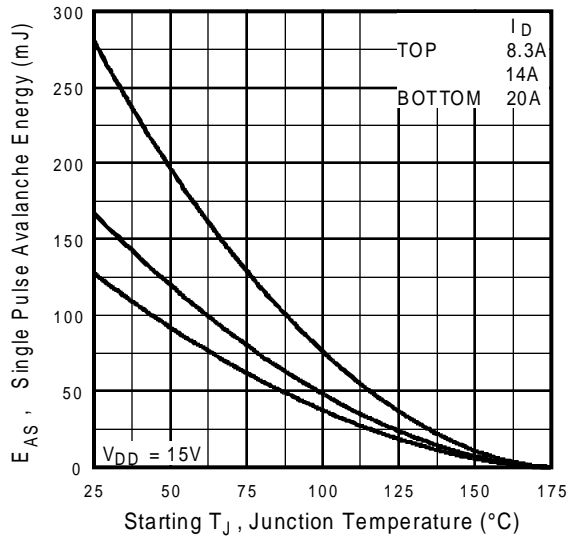
**Fig 12a.** Unclamped Inductive Test Circuit



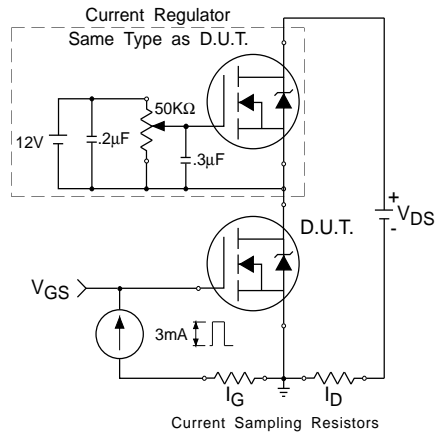
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

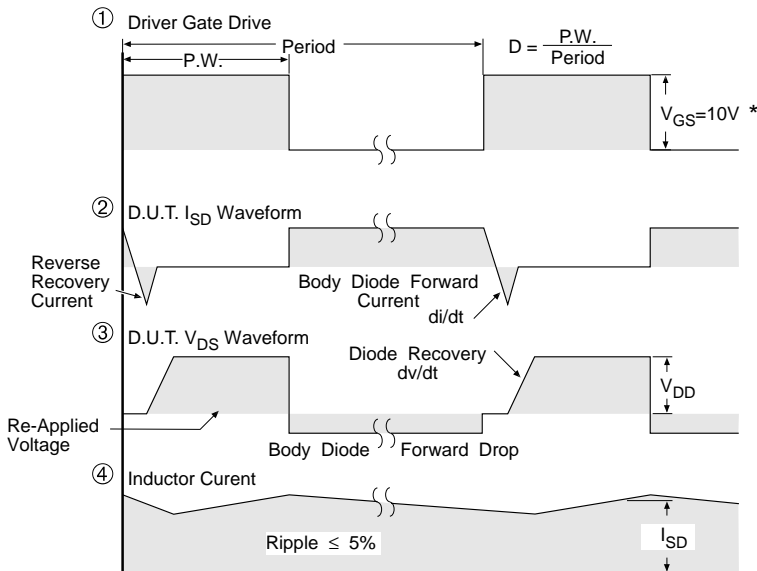
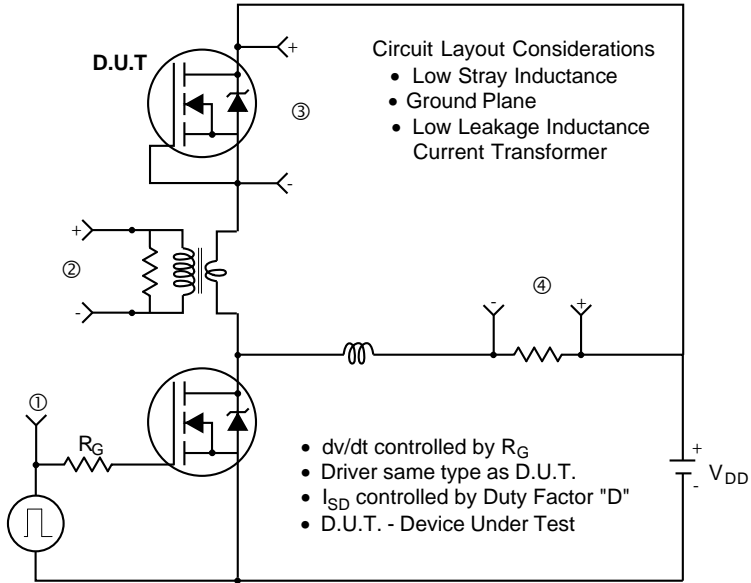


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

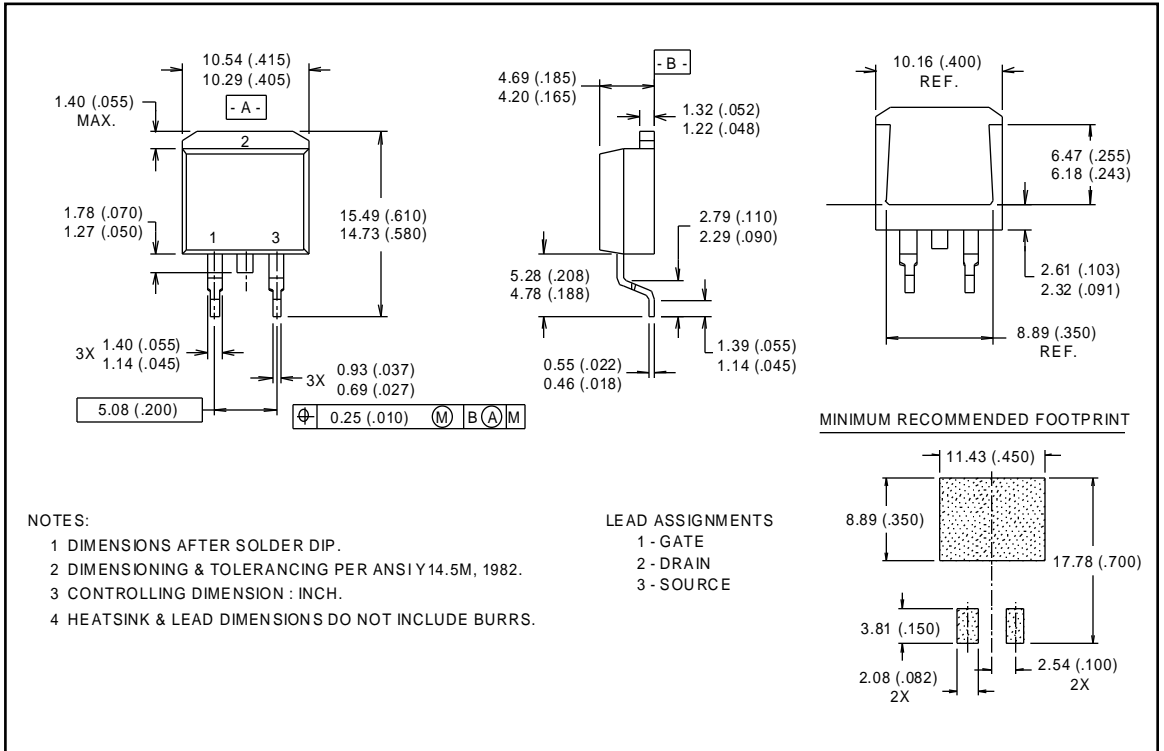
Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

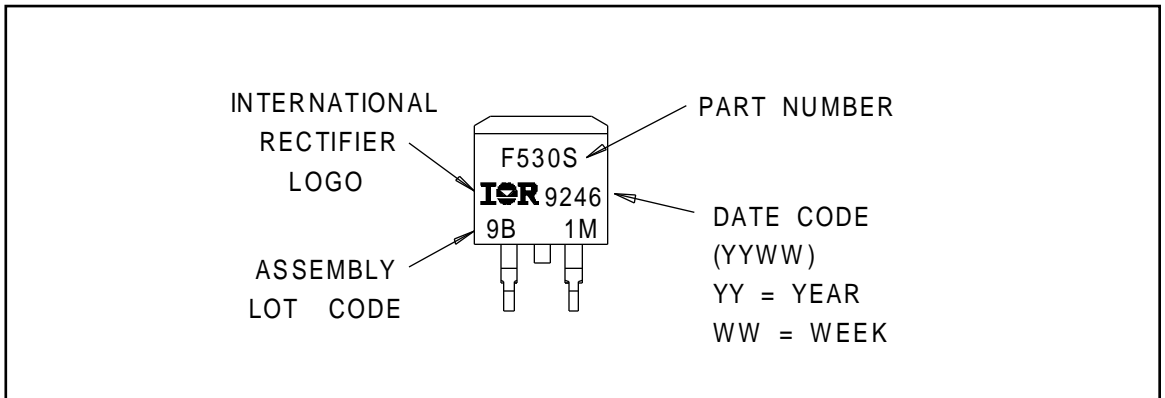
Fig 14. For N-Channel HEXFETS

## D<sup>2</sup>Pak Package Outline



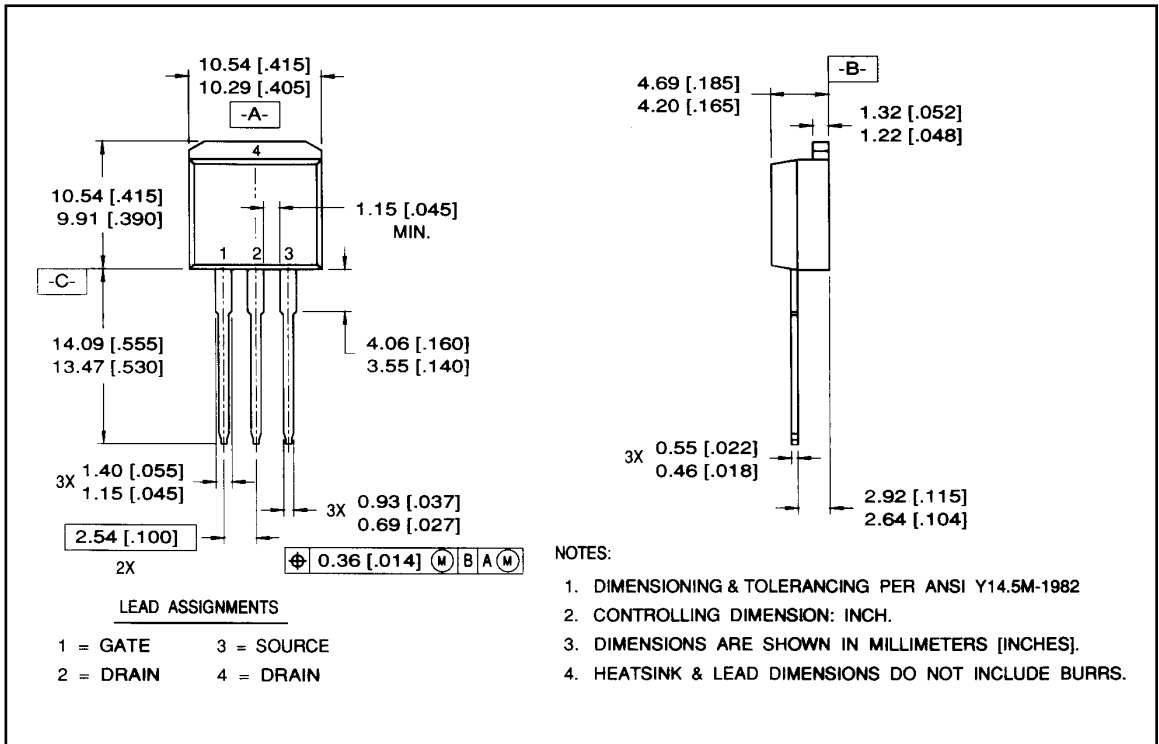
## Part Marking Information

### D<sup>2</sup>Pak



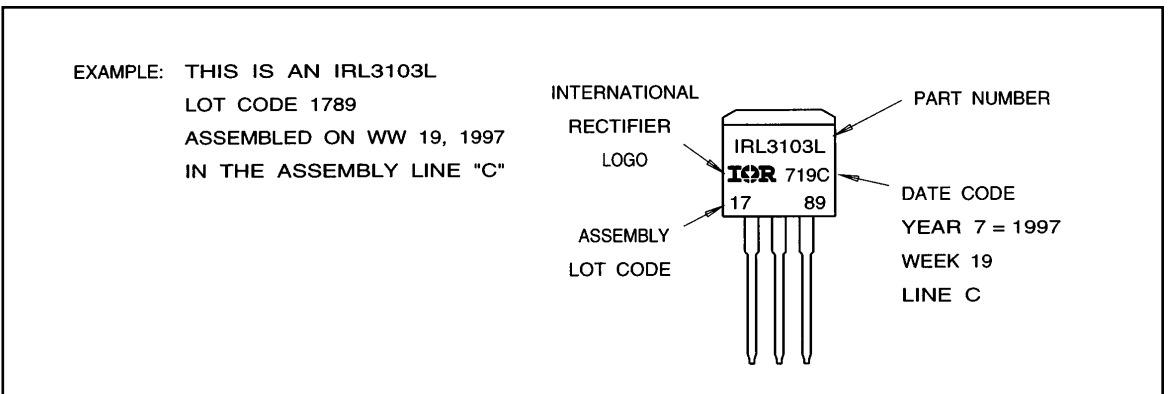
## Package Outline

### TO-262 Outline



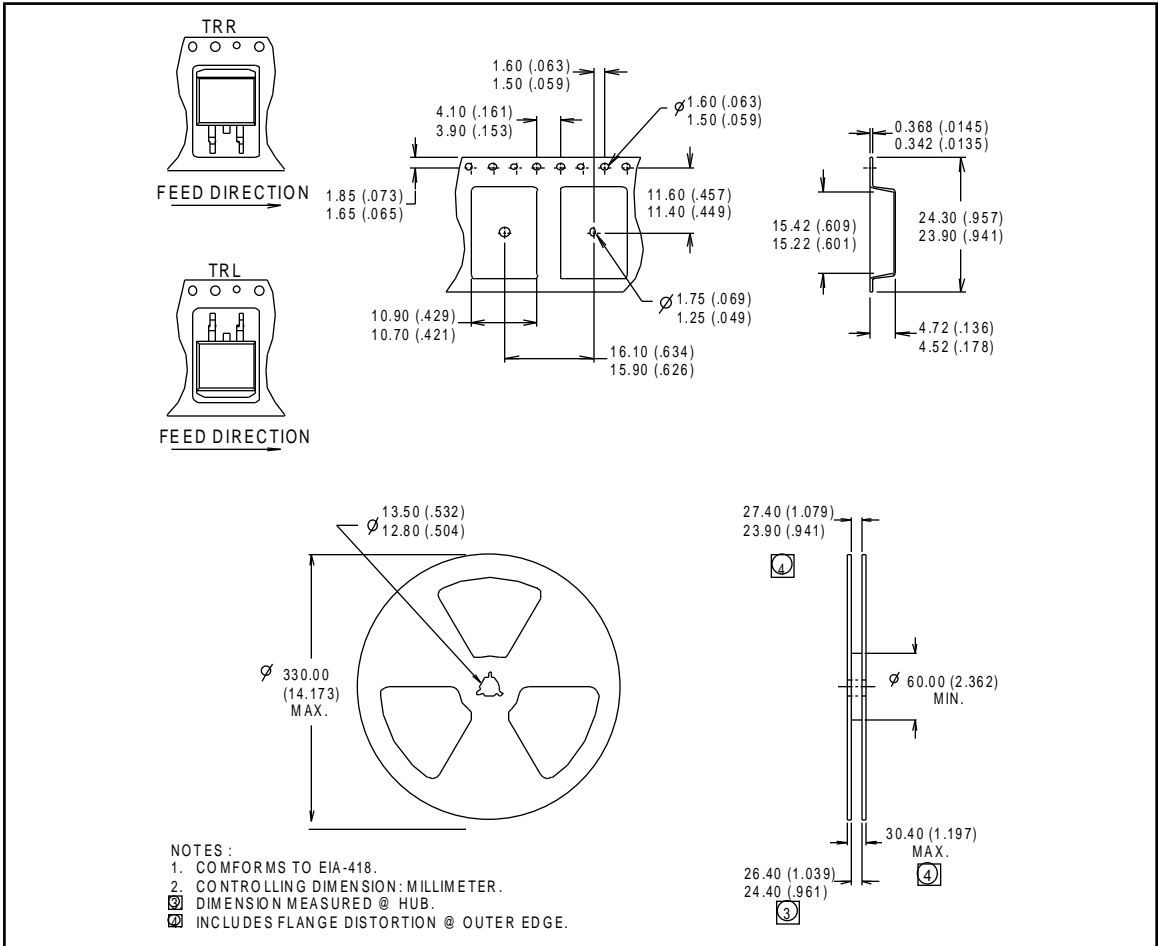
## Part Marking Information

### TO-262



## Tape & Reel Information

D<sup>2</sup>Pak









Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

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