



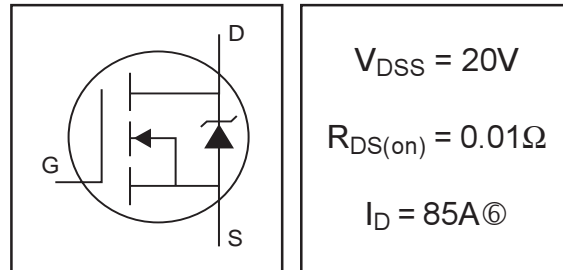
**THE DATASHEET OF
IRL3402S**



IRL3402S

HEXFET® Power MOSFET

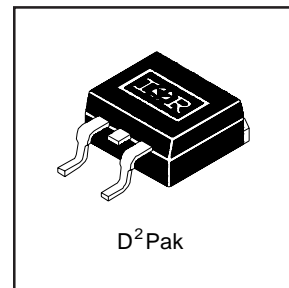
- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching



Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V\text{⑤}$	85⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V\text{⑤}$	54	
I_{DM}	Pulsed Drain Current ①③	340	
$P_D @ T_C = 25^\circ C$	Power Dissipation	110	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
V_{GSM}	Gate-to-Source Voltage (Start Up Transient, $t_p = 100\mu s$)	14	V
E_{AS}	Single Pulse Avalanche Energy②③	290	mJ
I_{AR}	Avalanche Current④	51	A
E_{AR}	Repetitive Avalanche Energy④	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	

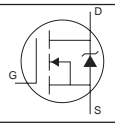
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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.010	Ω	V _{GS} = 4.5V, I _D = 51A ^④
		—	—	0.008		V _{GS} = 7.0V, I _D = 51A ^④
V _{GS(th)}	Gate Threshold Voltage	0.70	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	65	—	—	S	V _{DS} = 10V, I _D = 51A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 20V, V _{GS} = 0V
		—	—	250		V _{DS} = 16V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 10V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	78	nC	I _D = 51A
Q _{gs}	Gate-to-Source Charge	—	—	18		V _{DS} = 10V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	30		V _{GS} = 4.5V, See Fig. 6 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} = 10V
t _r	Rise Time	—	140	—		I _D = 51A
t _{d(off)}	Turn-Off Delay Time	—	80	—		R _G = 5.0Ω, V _{GS} = 4.5V
t _f	Fall Time	—	120	—		R _D = 0.19Ω, ^{④⑤}
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	3300	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1400	—		V _{DS} = 15V
C _{rss}	Reverse Transfer Capacitance	—	510	—		f = 1.0MHz, See Fig. 5 ^⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^{①⑤}	—	—	340		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 51A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	72	110	ns	T _J = 25°C, I _F = 51A
Q _{rr}	Reverse Recovery Charge	—	160	240	nC	di/dt = 100A/μs ^{④⑤}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T_J = 25°C, L = 220μH
R_G = 25Ω, I_{AS} = 51A.
- ③ I_{SD} ≤ 51A, di/dt ≤ 82A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRL3402 data and test conditions
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

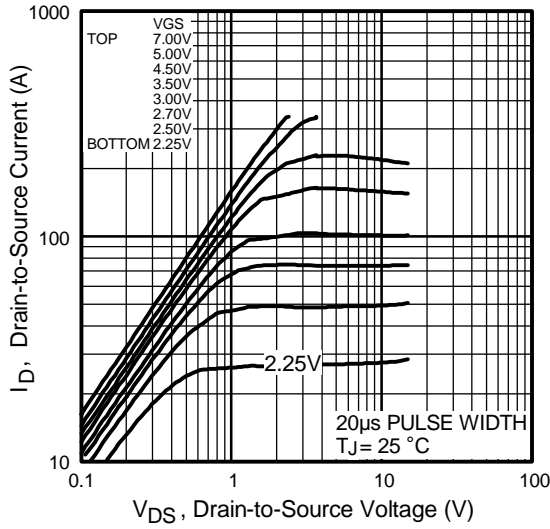


Fig 1. Typical Output Characteristics

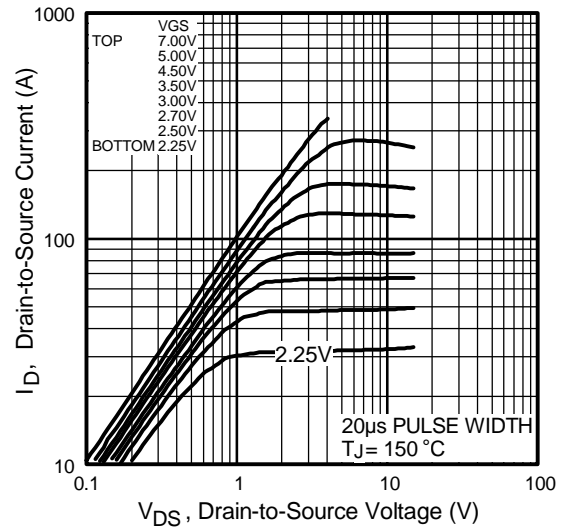


Fig 2. Typical Output Characteristics

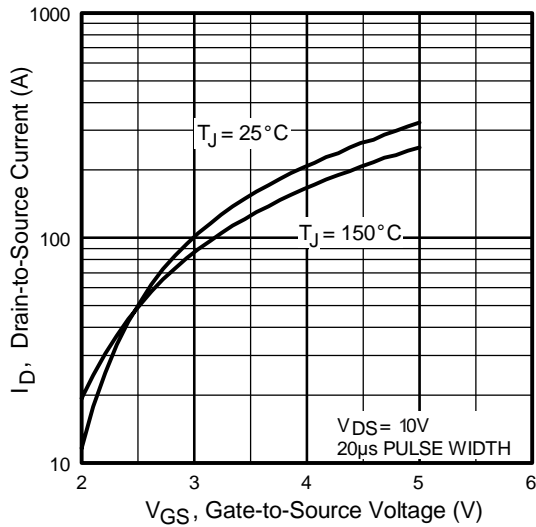


Fig 3. Typical Transfer Characteristics

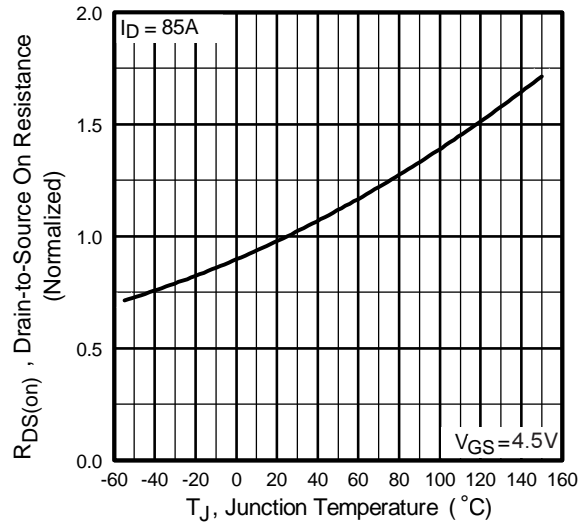


Fig 4. Normalized On-Resistance Vs. Temperature

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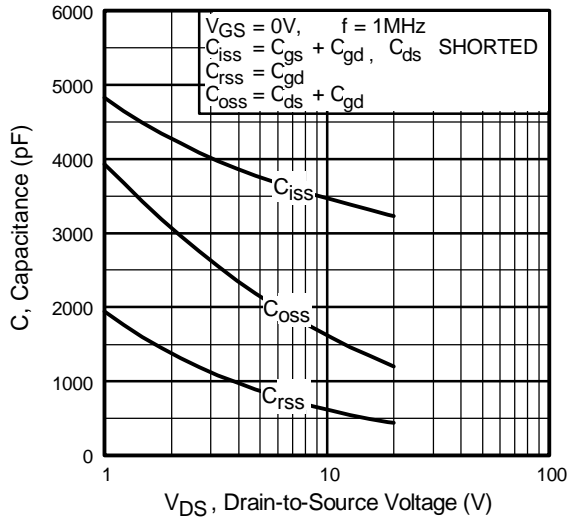


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

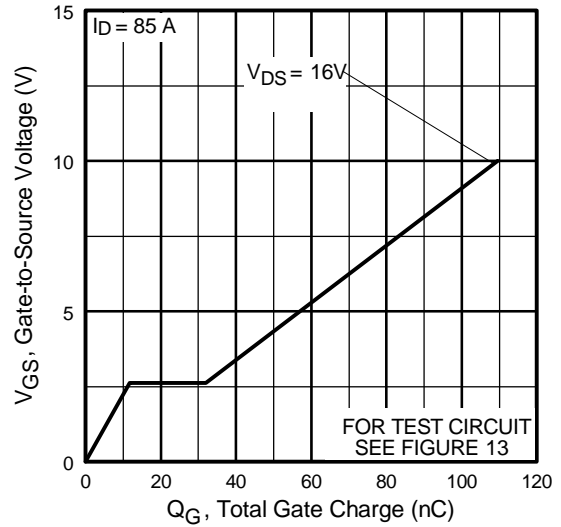


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

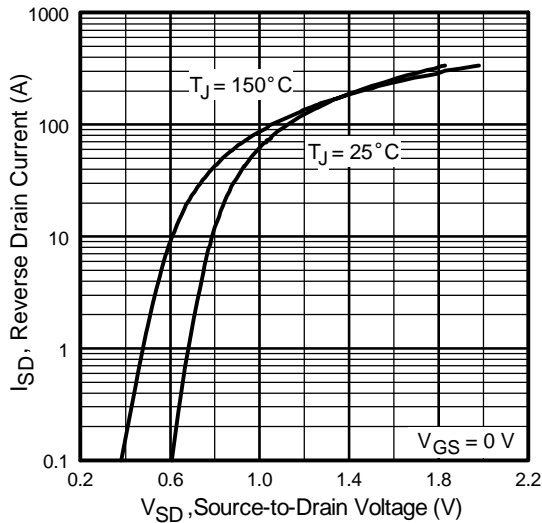


Fig 7. Typical Source-Drain Diode Forward Voltage

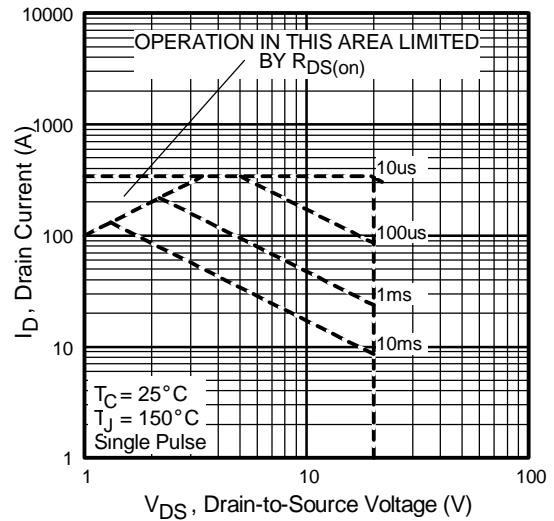


Fig 8. Maximum Safe Operating Area

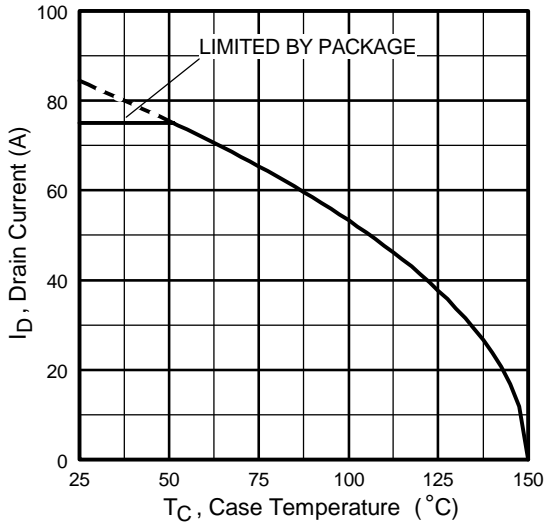


Fig 9. Maximum Drain Current Vs. Case Temperature

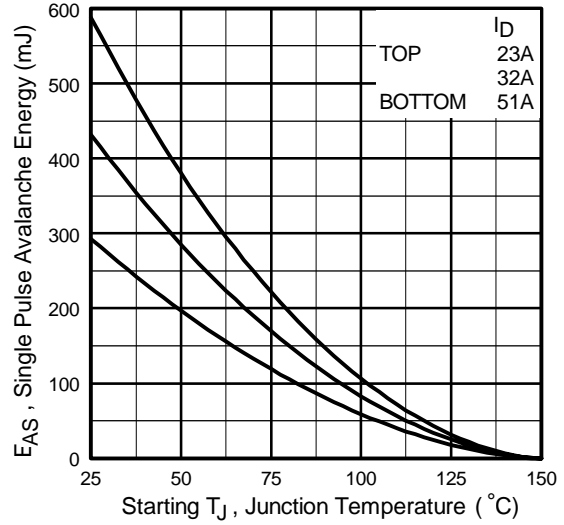


Fig 10. Maximum Avalanche Energy Vs. Drain Current

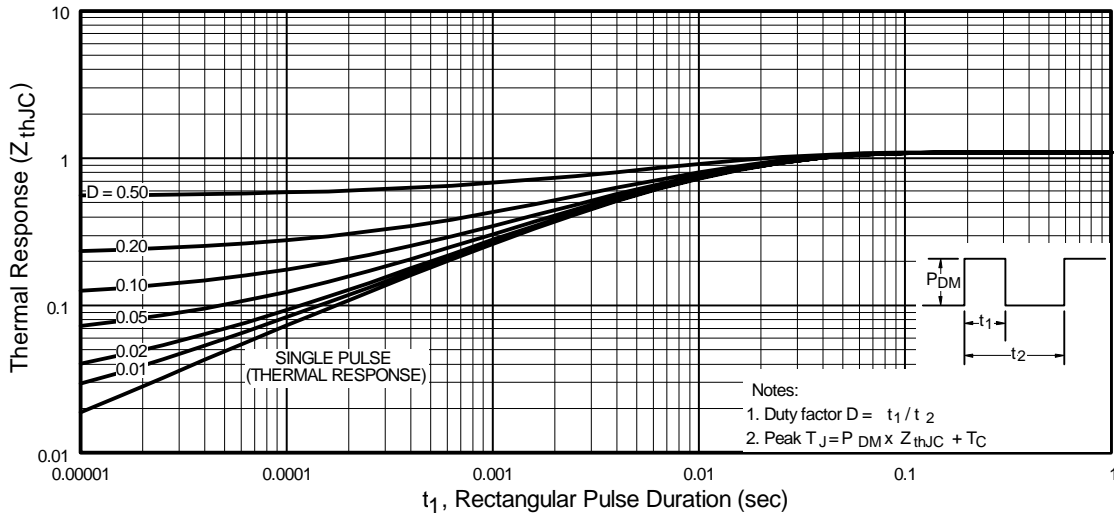


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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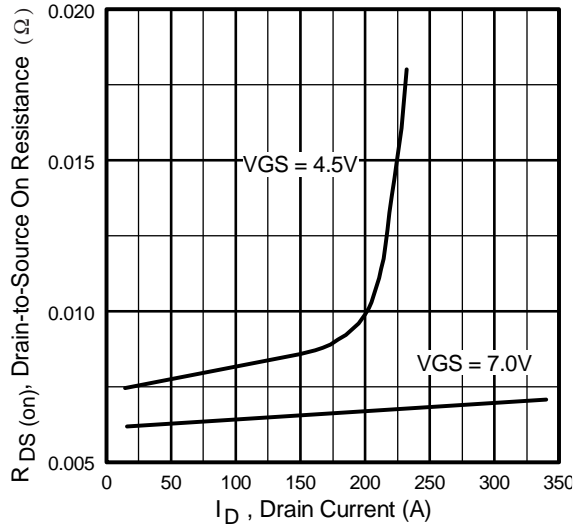


Fig 12. On-Resistance Vs. Drain Current

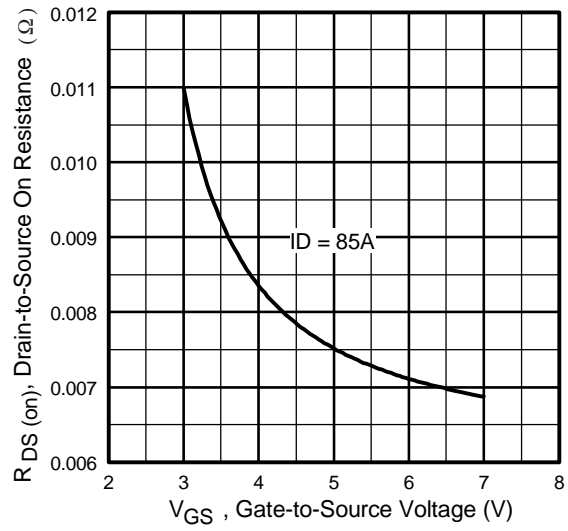
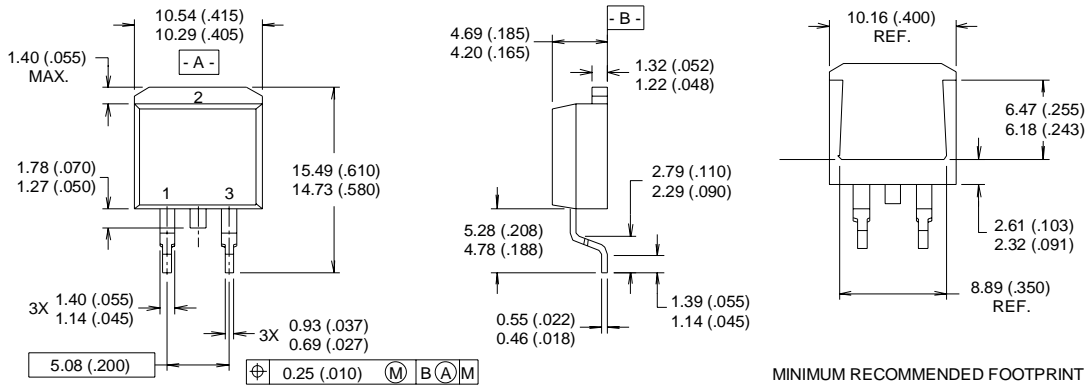


Fig 13. On-Resistance Vs. Gate Voltage

D²Pak Package Outline



NOTES:

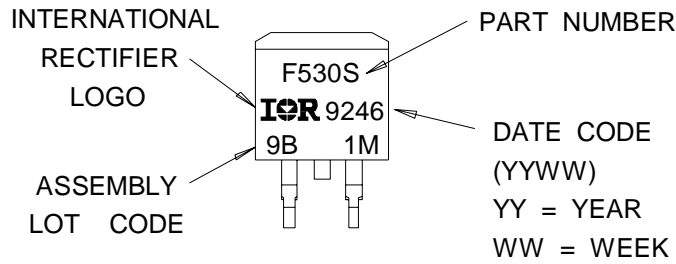
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

Part Marking Information

D²Pak

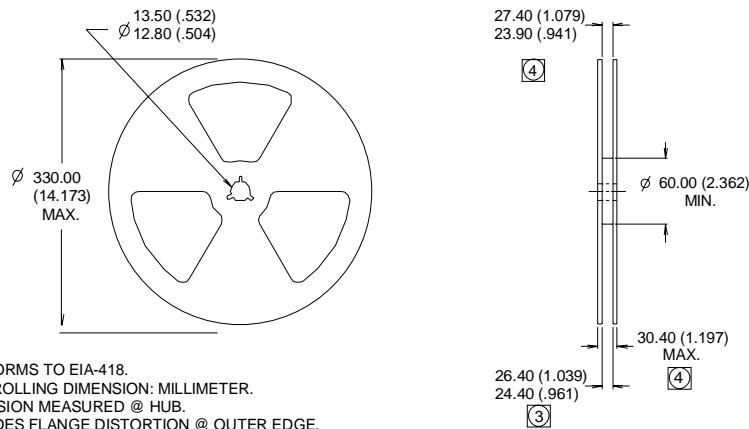
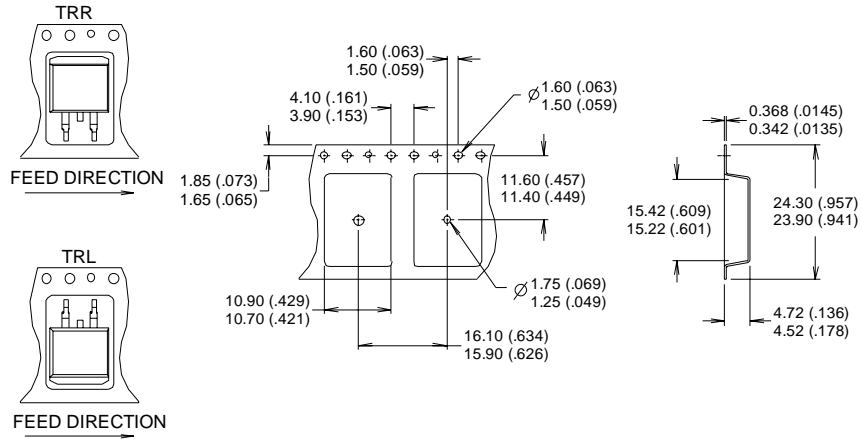


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Tape & Reel Information

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Data and specifications subject to change without notice.

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