



**THE DATASHEET OF
IRL3714STRL**



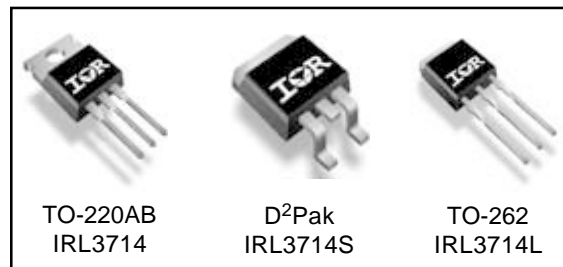
Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power

V_{DSS}	R_{DS(on)} max	I_D
20V	20mΩ	36A

Benefits

- Ultra-Low Gate Impedance
- Very Low R_{DS(on)} at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	20	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	36	A
I _D @ T _C = 70°C	Continuous Drain Current, V _{GS} @ 10V	31	
I _{DM}	Pulsed Drain Current ^①	140	
P _D @ T _C = 25°C	Maximum Power Dissipation ^③	47	W
P _D @ T _C = 70°C	Maximum Power Dissipation ^③	33	W
	Linear Derating Factor	0.31	W/°C
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	3.2	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface ^④	0.50	—	
R _{θJA}	Junction-to-Ambient ^④	—	62	
R _{θJA}	Junction-to-Ambient (PCB mount) ^⑤	—	40	

Notes ① through ⑥ are on page 11

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	15	20	m Ω	$V_{GS} = 10V, I_D = 18A$ ③
		—	21	28		$V_{GS} = 4.5V, I_D = 14A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$

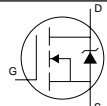
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	17	—	—	S	$V_{DS} = 10V, I_D = 14A$
Q_g	Total Gate Charge	—	6.5	9.7	nC	$I_D = 14A$
Q_{gs}	Gate-to-Source Charge	—	1.8	—		$V_{DS} = 10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.9	—		$V_{GS} = 4.5V$
Q_{oss}	Output Gate Charge	—	7.1	—		$V_{GS} = 0V, V_{DS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	8.7	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	78	—		$I_D = 14A$
$t_{d(off)}$	Turn-Off Delay Time	—	10	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	4.5	—		$V_{GS} = 4.5V$ ③
C_{iss}	Input Capacitance	—	670	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	470	—		$V_{DS} = 10V$
C_{rss}	Reverse Transfer Capacitance	—	68	—		$f = 1.0\text{MHz}$

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	72	mJ
I_{AR}	Avalanche Current①	—	14	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	36	—	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	140	—		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ③
		—	0.88	—		$T_J = 125^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	35	53	ns	$T_J = 25^\circ\text{C}, I_F = 18A, V_R = 10V$
Q_{rr}	Reverse Recovery Charge	—	34	51	nC	$di/dt = 100A/\mu s$ ③
t_{rr}	Reverse Recovery Time	—	35	53	ns	$T_J = 125^\circ\text{C}, I_F = 18A, V_R = 10V$
Q_{rr}	Reverse Recovery Charge	—	35	53	nC	$di/dt = 100A/\mu s$ ③

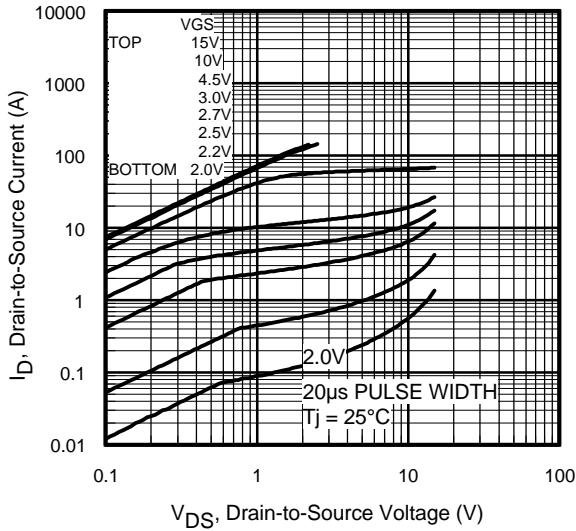


Fig 1. Typical Output Characteristics

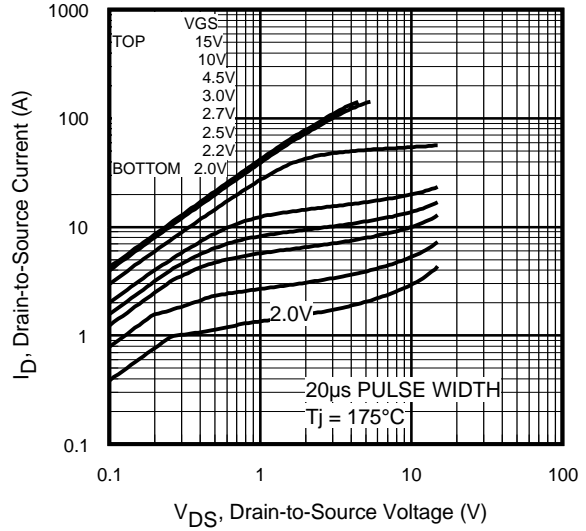


Fig 2. Typical Output Characteristics

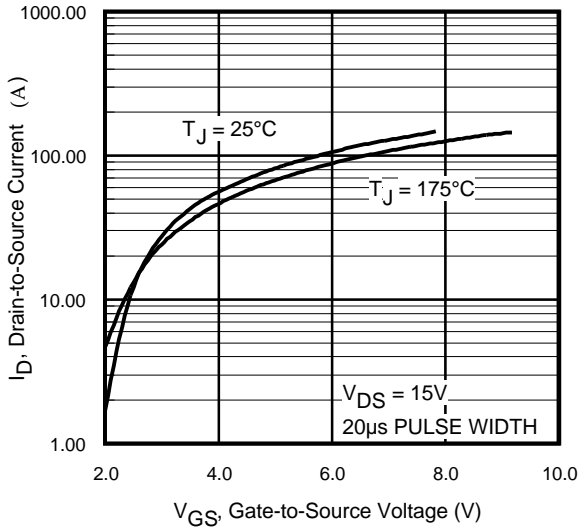


Fig 3. Typical Transfer Characteristics

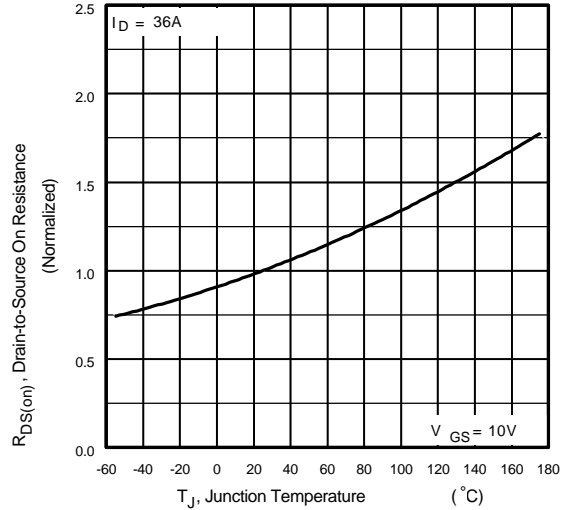


Fig 4. Normalized On-Resistance Vs. Temperature

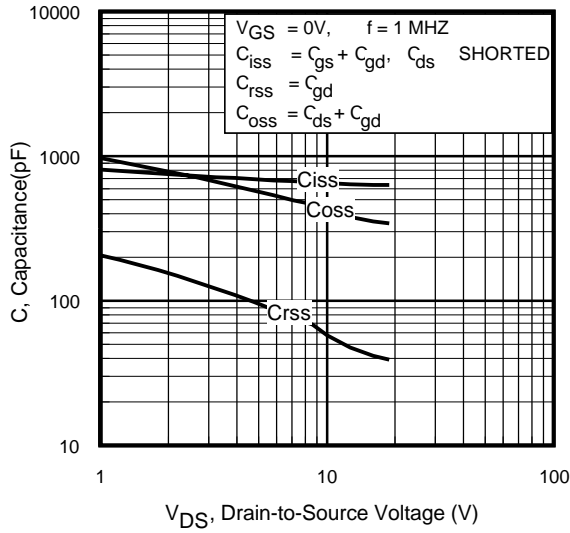


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

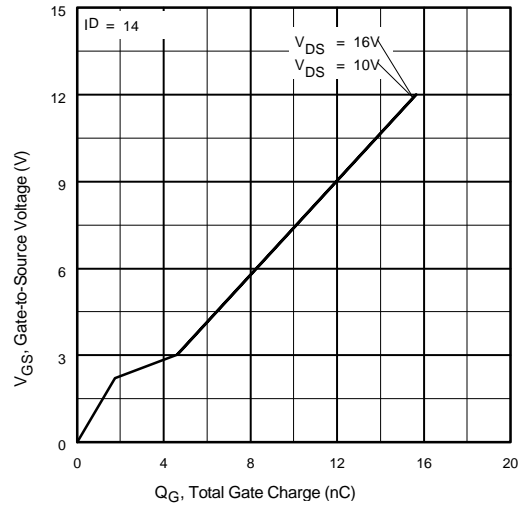


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

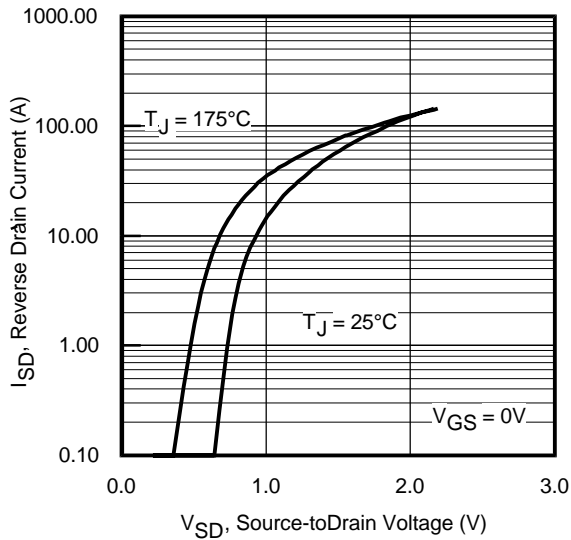


Fig 7. Typical Source-Drain Diode Forward Voltage

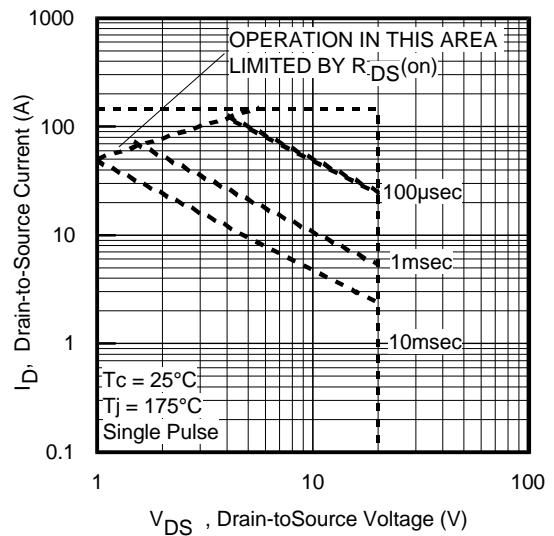


Fig 8. Maximum Safe Operating Area

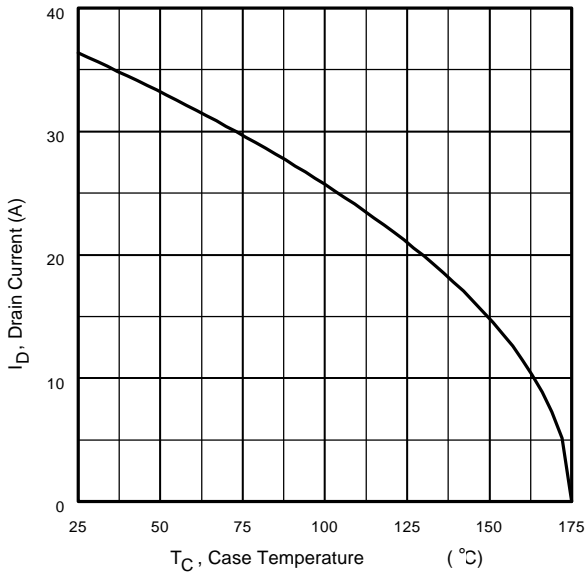


Fig 9. Maximum Drain Current Vs. Case Temperature

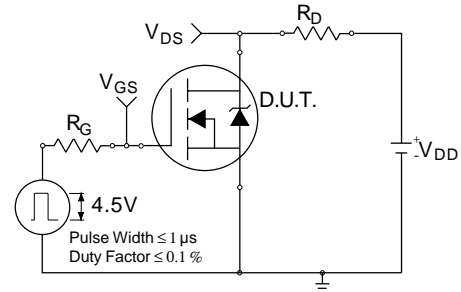


Fig 10a. Switching Time Test Circuit

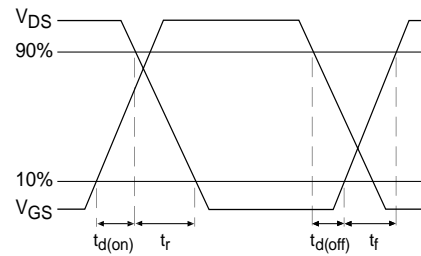


Fig 10b. Switching Time Waveforms

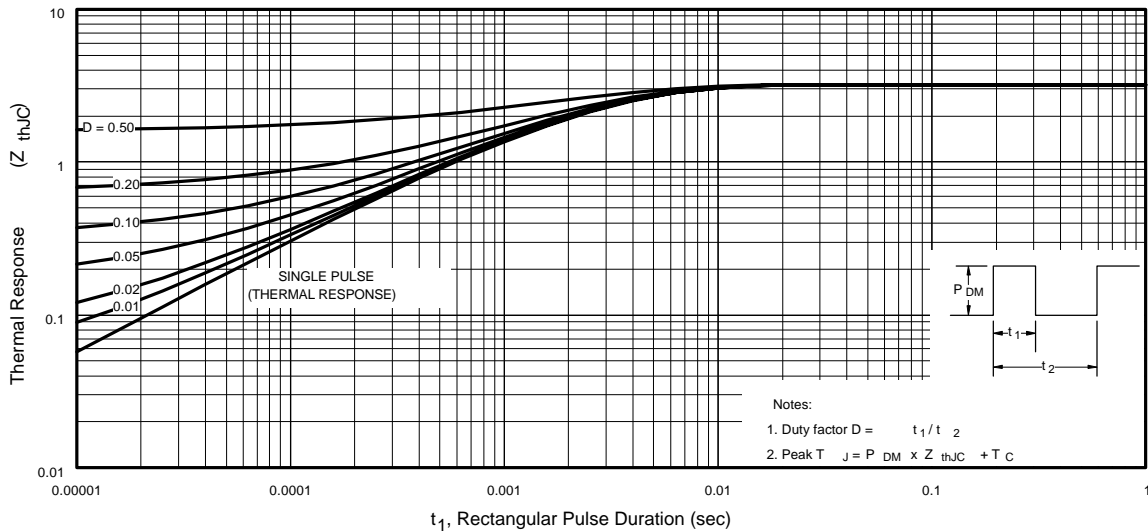


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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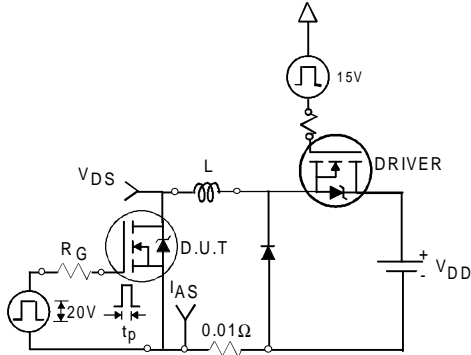


Fig 12a. Unclamped Inductive Test Circuit

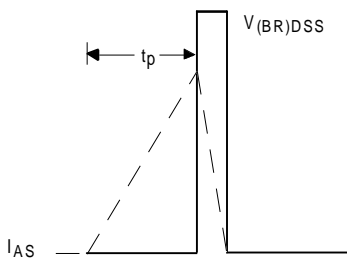


Fig 12b. Unclamped Inductive Waveforms

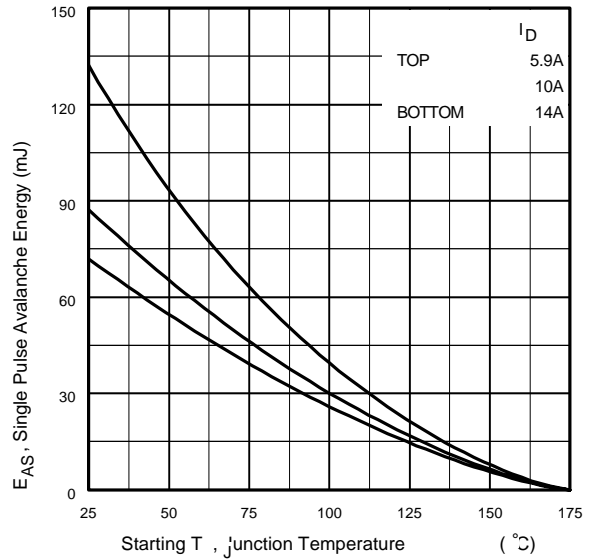


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

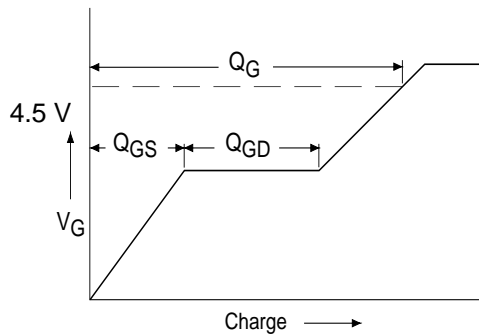


Fig 13a. Basic Gate Charge Waveform

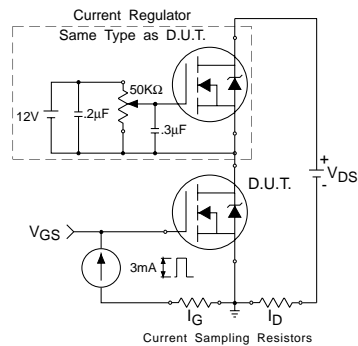
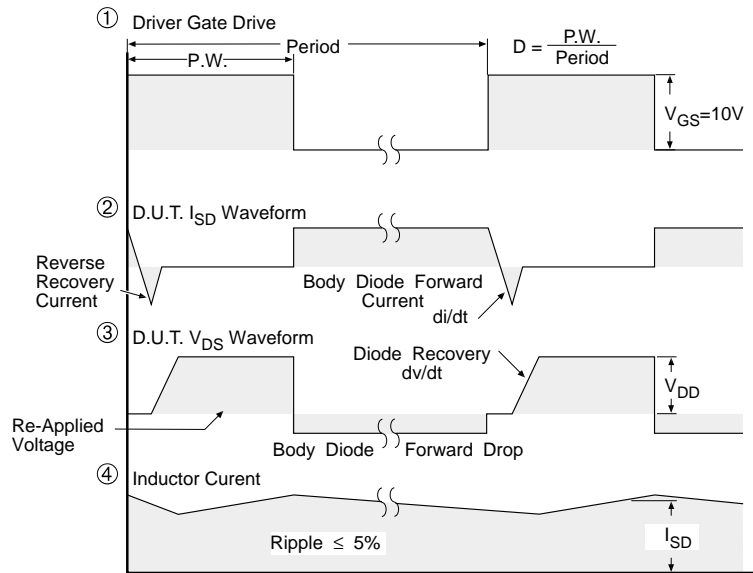
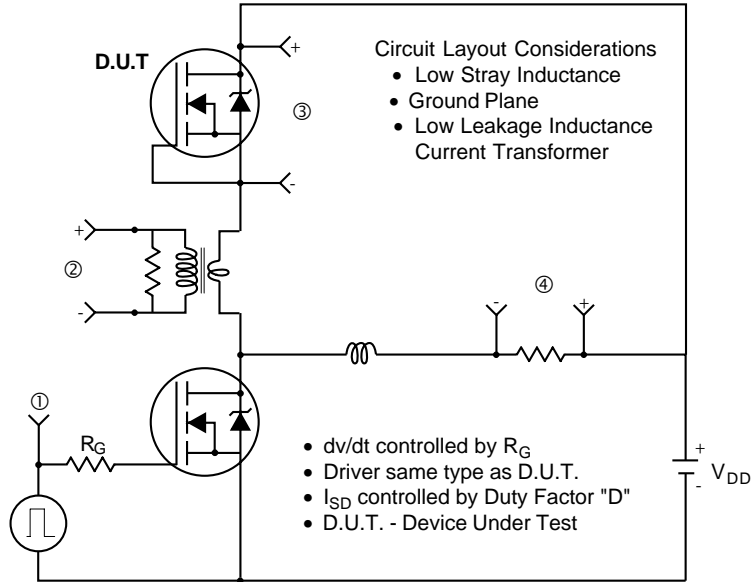


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

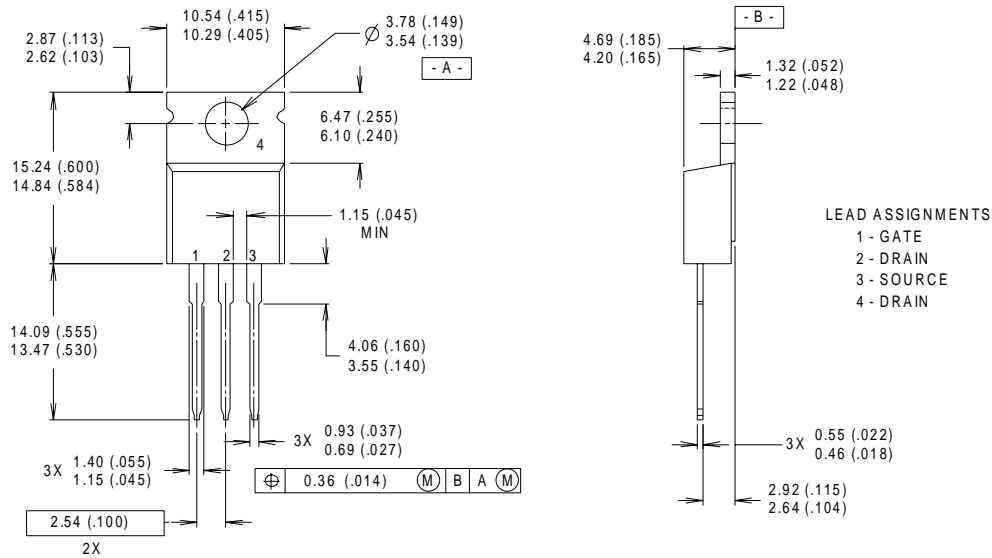
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



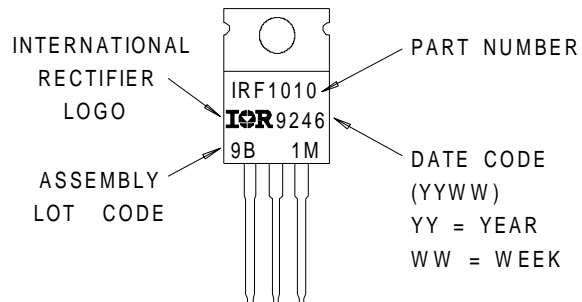
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

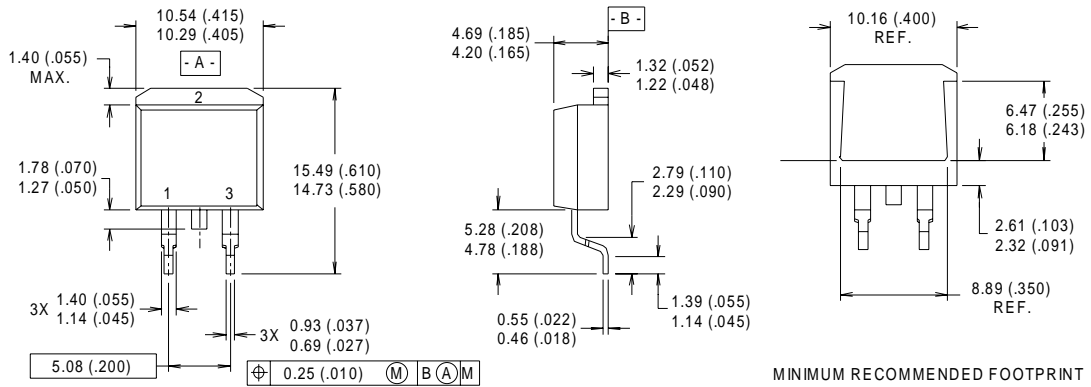
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



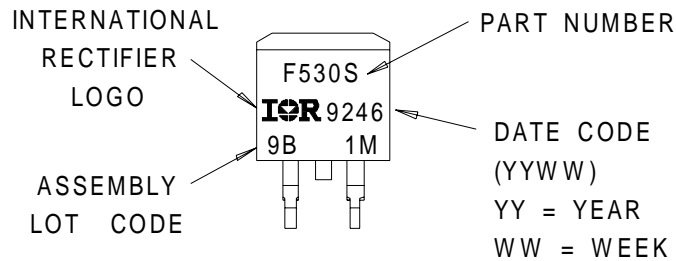
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

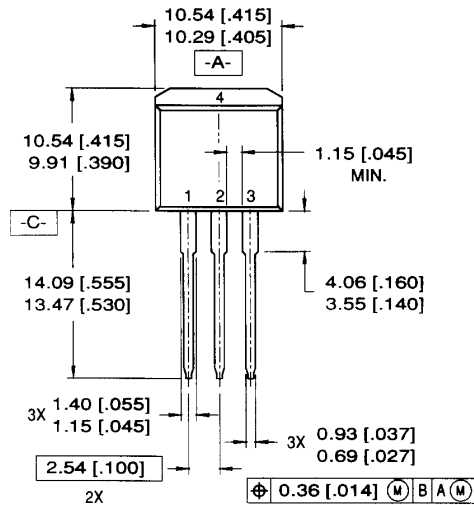
D²Pak Part Marking Information



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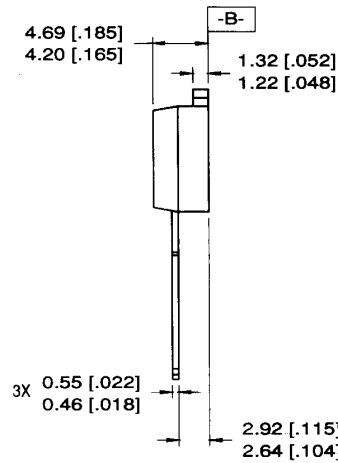
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TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

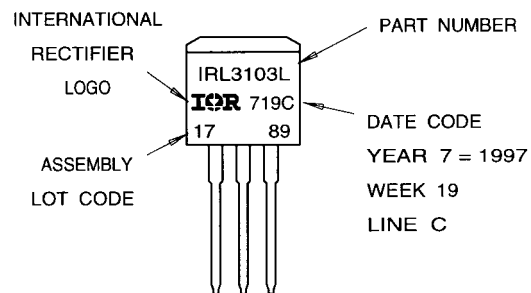


NOTES:

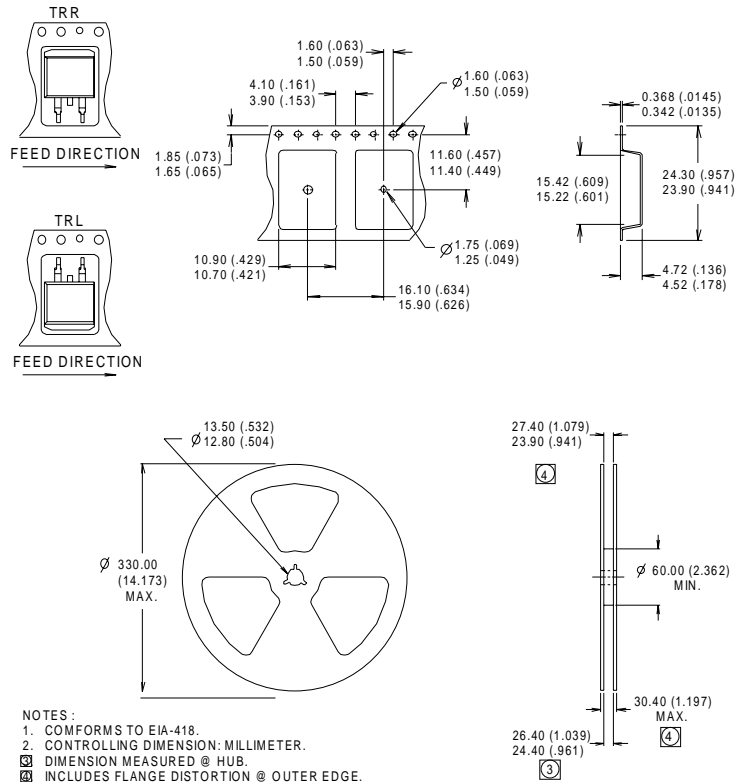
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



NOTES:
 1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.69\text{ mH}$
 $R_G = 25\Omega$, $I_{AS} = 14\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ This is only applied to TO-220AB package.
- ⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 These products have been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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