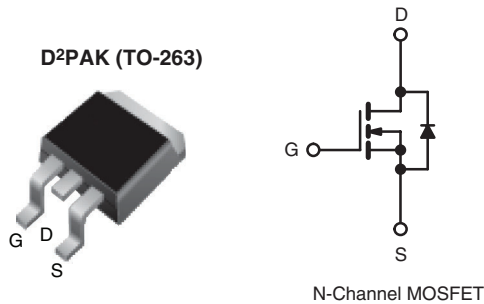




## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	100
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5\text{ V}$ 0.27
$Q_g$ (Max.) (nC)	12
$Q_{gs}$ (nC)	3.0
$Q_{gd}$ (nC)	7.1
Configuration	Single



### FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4\text{ V}$  and  $5\text{ V}$
- 175°C Operating Temperature

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION	
Package	D <sup>2</sup> PAK (TO-263)
SnPb	IRL520S
	SiHL520S

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 10$		
Continuous Drain Current	$V_{GS}$ at 5 V	$T_C = 25\text{ }^\circ\text{C}$	9.2	A
		$T_C = 100\text{ }^\circ\text{C}$	6.5	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	36	W/ $^\circ\text{C}$	
Linear Derating Factor		0.40		
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.025		
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	170	mJ	
Avalanche Current <sup>a</sup>	$I_{AR}$	9.2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	6.0	mJ	
Maximum Power Dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	60	W
		$T_A = 25\text{ }^\circ\text{C}$	3.7	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		



### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3.0\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 9.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$ ,  $dI/dt \leq 110\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.5	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5\text{ V}$	$I_D = 5.5\text{ A}^b$	-	-	0.27	$\Omega$
		$V_{GS} = 4\text{ V}$	$I_D = 4.6\text{ A}^b$	-	-	0.38	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 5.5\text{ A}^b$		3.2	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	490	-	pF
Output Capacitance	$C_{oss}$			-	150	-	
Reverse Transfer Capacitance	$C_{rss}$			-	30	-	
Total Gate Charge	$Q_g$	$V_{GS} = 5\text{ V}$	$I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	12	nC
Gate-Source Charge	$Q_{GS}$			-	-	3.0	
Gate-Drain Charge	$Q_{GD}$			-	-	7.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 9.2\text{ A}, R_G = 9\text{ }\Omega, R_D = 5.2\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	9.8	-	ns
Rise Time	$t_r$			-	64	-	
Turn-Off Delay Time	$t_{d(off)}$			-	21	-	
Fall Time	$t_f$			-	27	-	
<b>Dynamic</b>							
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	9.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	36	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.2\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	130	190	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.83	1.0	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

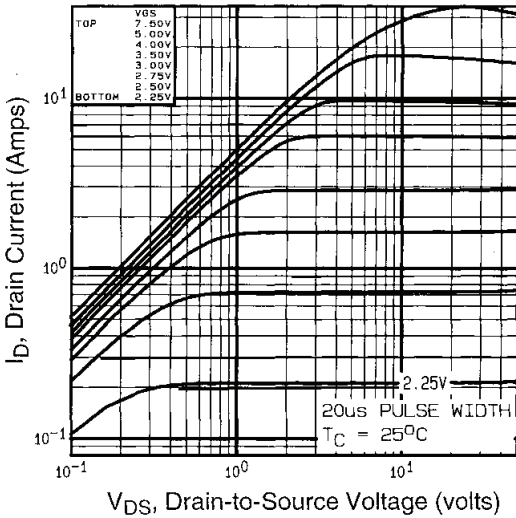


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

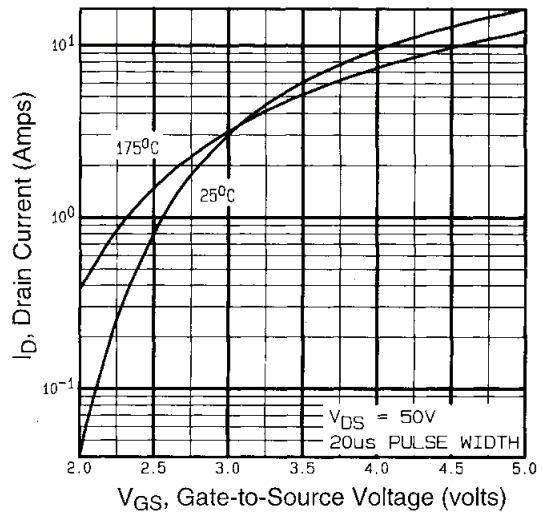


Fig. 3 - Typical Transfer Characteristics

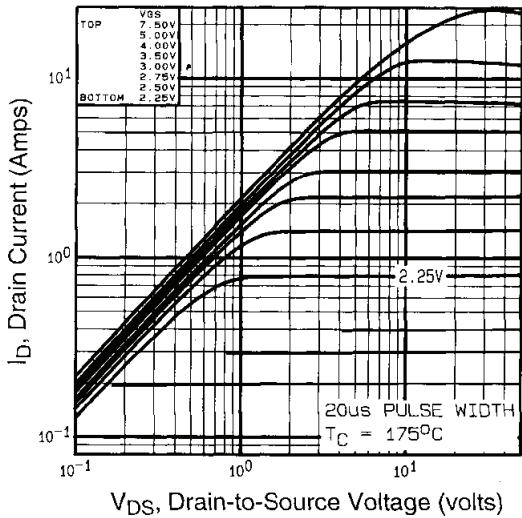


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

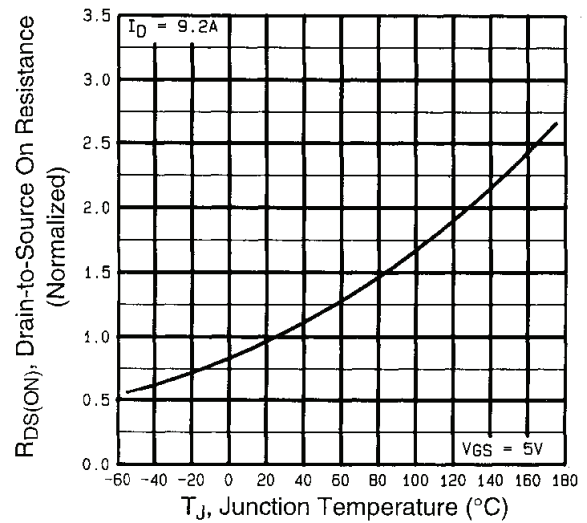


Fig. 4 - Normalized On-Resistance vs. Temperature

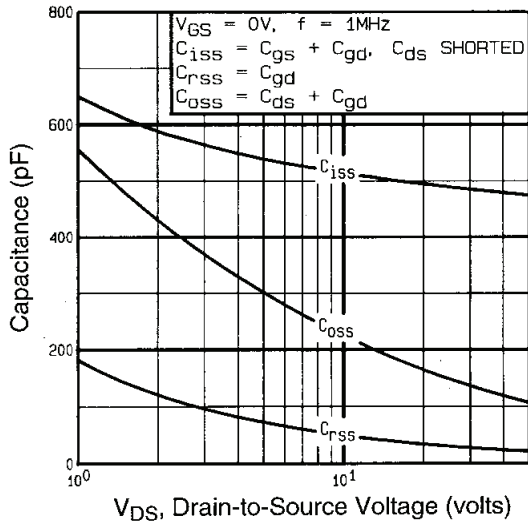


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

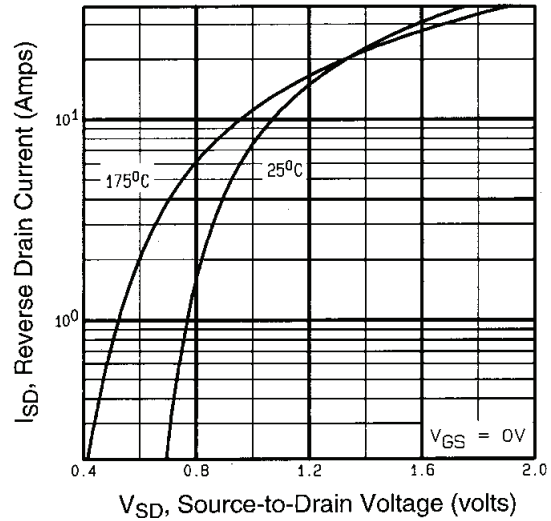


Fig. 7 - Typical Source-Drain Diode Forward Voltage

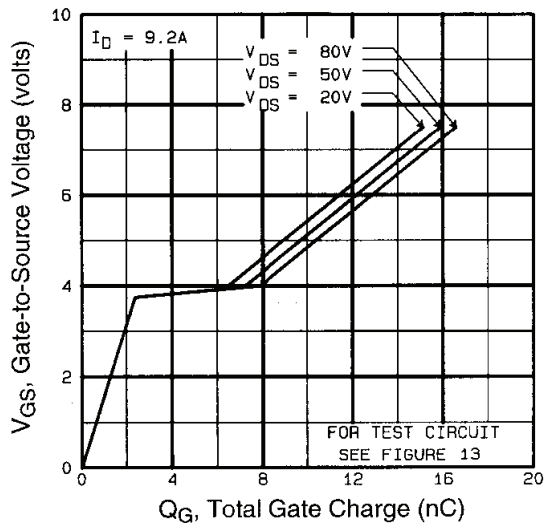


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

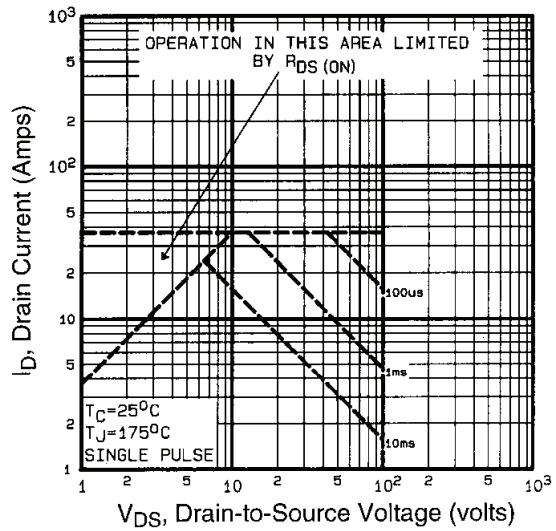
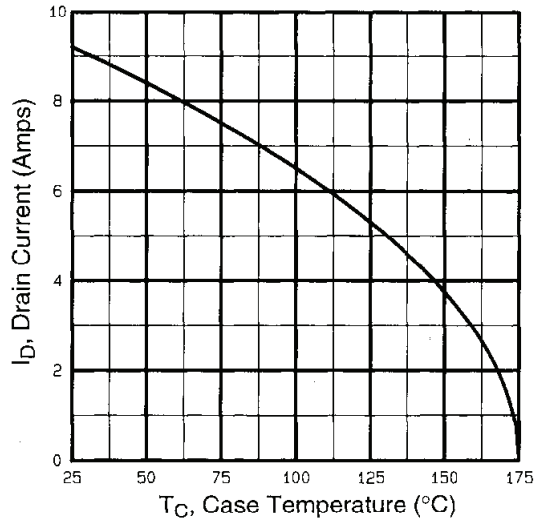
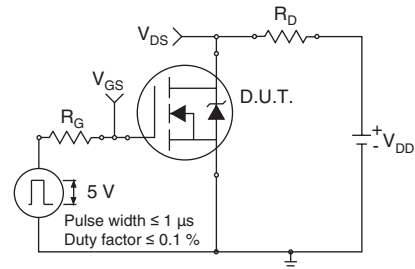


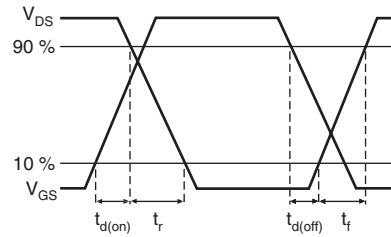
Fig. 8 - Maximum Safe Operating Area



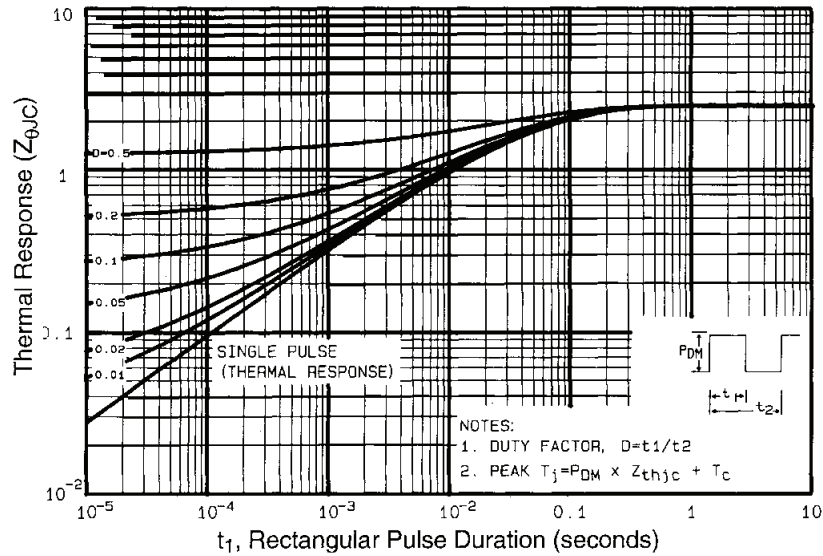
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

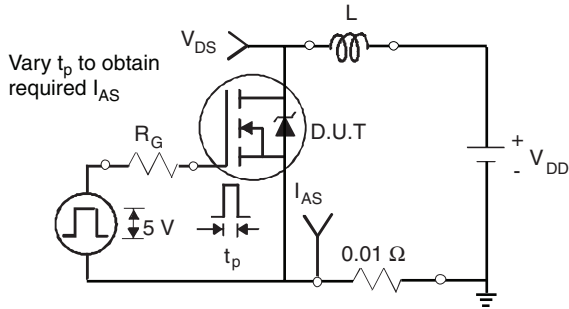


Fig. 12a - Unclamped Inductive Test Circuit

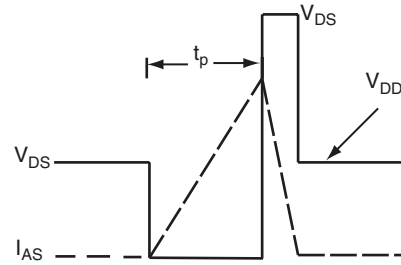


Fig. 12b - Unclamped Inductive Waveforms

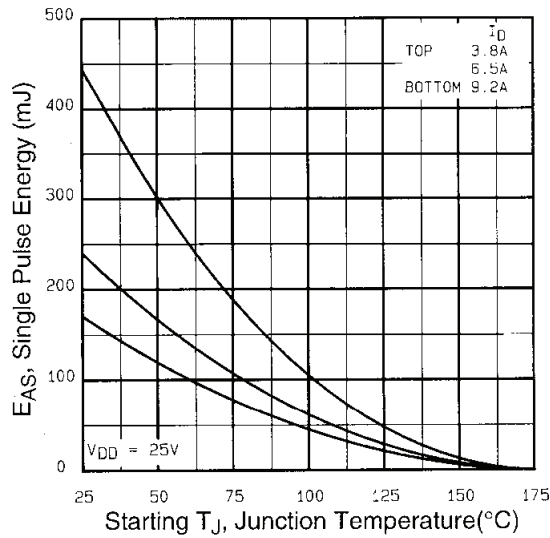


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

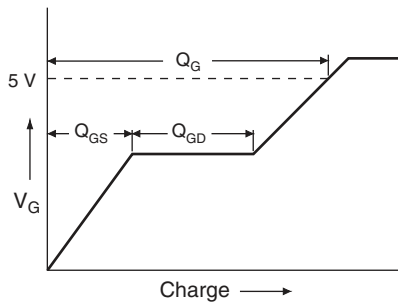


Fig. 13a - Basic Gate Charge Waveform

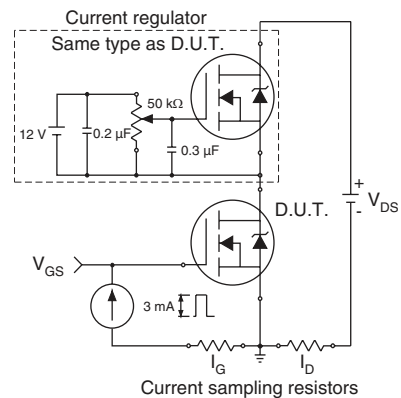
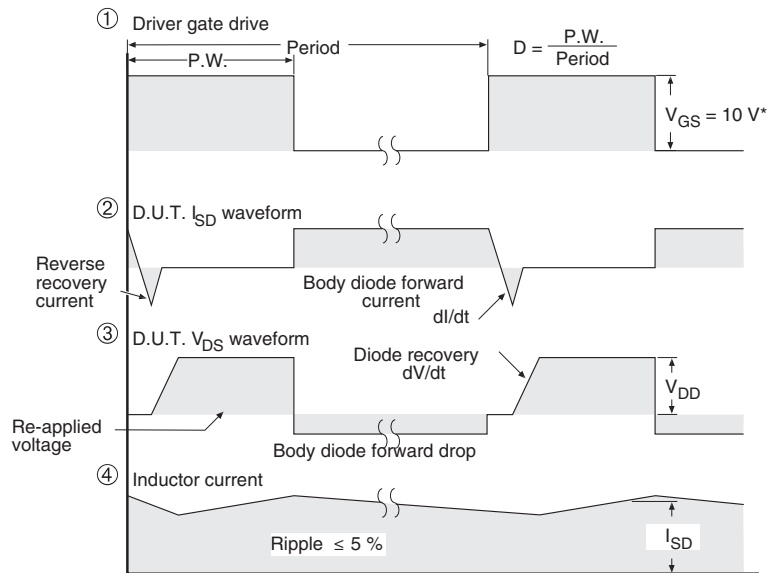
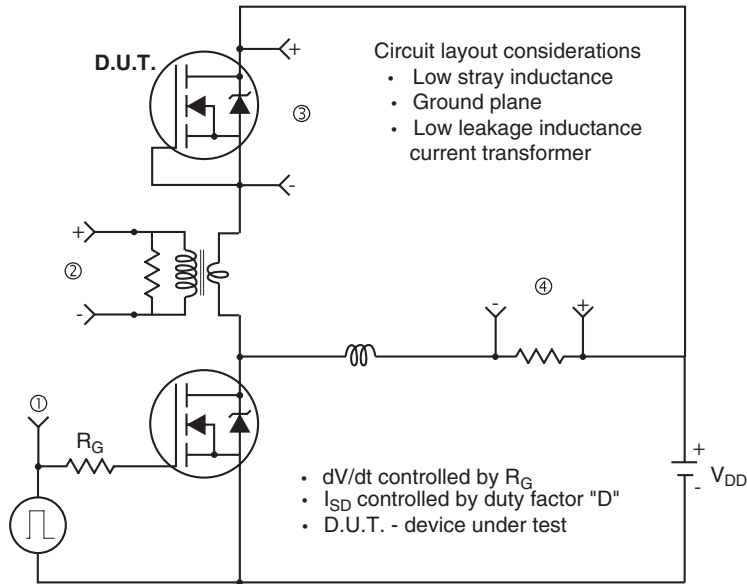


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



\*  $V_{GS} = 5\text{ V}$  for logic level and  $3\text{ V}$  drive devices

**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?90382](http://www.vishay.com/ppg?90382).



## Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View IRL520STRL on WIN SOURCE](#)

 [Vishay Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management