



THE DATASHEET OF NDF11N50ZH



NDF11N50Z

N-Channel Power MOSFET 500 V, 0.52 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	NDF	Unit
Drain–to–Source Voltage	V_{DSS}	500	V
Continuous Drain Current, $R_{\theta JC}$ (Note 1)	I_D	12	A
Continuous Drain Current $T_A = 100^\circ\text{C}$, $R_{\theta JC}$ (Note 1)	I_D	7.4	A
Pulsed Drain Current, $t_p = 10 \mu\text{s}$	I_{DM}	44	A
Power Dissipation, $R_{\theta JC}$	P_D	39	W
Gate–to–Source Voltage	V_{GS}	± 30	V
Single Pulse Avalanche Energy, $I_D = 10 \text{ A}$	E_{AS}	420	mJ
ESD (HBM) (JESD22–A114)	V_{esd}	4000	V
RMS Isolation Voltage ($t = 0.3 \text{ sec.}$, R.H. $\leq 30\%$, $T_A = 25^\circ\text{C}$) (Figure 14)	V_{ISO}	4500	V
Peak Diode Recovery (Note 2)	dv/dt	4.5	V/ns
MOSFET dV/dt	dV/dt	60	V/ns
Continuous Source Current (Body Diode)	I_S	12	A
Maximum Temperature for Soldering Leads	T_L	260	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

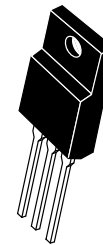
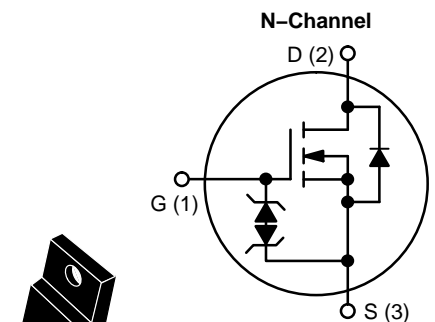
1. Limited by maximum junction temperature
2. $I_d \leq 10.5 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ\text{C}$.



ON Semiconductor®

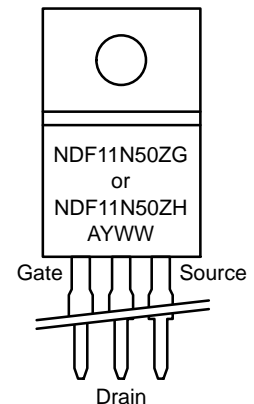
www.onsemi.com

V_{DSS}	$R_{DS(ON)} \text{ (MAX) @ } 4.5 \text{ A}$
500 V	0.52 Ω



NDF11N50ZG
NDF11N50ZH
TO–220FP
CASE 221AH

MARKING DIAGRAM



- A = Location Code
- Y = Year
- WW = Work Week
- G, H = Pb–Free, Halogen–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NDF11N50Z

THERMAL RESISTANCE

Parameter	Symbol	NDF11N50Z	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.2	°C/W
Junction-to-Ambient Steady State (Note 3)	$R_{\theta JA}$	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
----------------	-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	500			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D = 1\text{ mA}$	$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	25°C		1	μA
			125°C		50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	I_{GSS}			±10	μA

ON CHARACTERISTICS (Note 4)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	$R_{DS(on)}$		0.48	0.52	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	$V_{GS(th)}$	3.0	3.9	4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 4.5\text{ A}$	g_{FS}		7.7		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 5)	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	C_{iss}	1097	1375	1645	pF
Output Capacitance (Note 5)		C_{oss}	132	166	199	
Reverse Transfer Capacitance (Note 5)		C_{rss}	30	40	50	
Total Gate Charge (Note 5)	$V_{DD} = 250\text{ V}, I_D = 10.5\text{ A},$ $V_{GS} = 10\text{ V}$	Q_g	23	46	69	nC
Gate-to-Source Charge (Note 5)		Q_{gs}	4.5	8.7	13	
Gate-to-Drain ("Miller") Charge (Note 5)		Q_{gd}	12.5	25	37.5	
Plateau Voltage		V_{GP}		6.2		V
Gate Resistance		R_g		1.4		Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 10.5\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$	$t_{d(on)}$		15		ns
Rise Time		t_r		32		
Turn-Off Delay Time		$t_{d(off)}$		40		
Fall Time		t_f		23		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 10.5\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 10.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}		310		ns
Reverse Recovery Charge		Q_{rr}		2.5		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Insertion mounted
4. Pulse Width $\leq 380\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
5. Guaranteed by design.

NDF11N50Z

TYPICAL CHARACTERISTICS

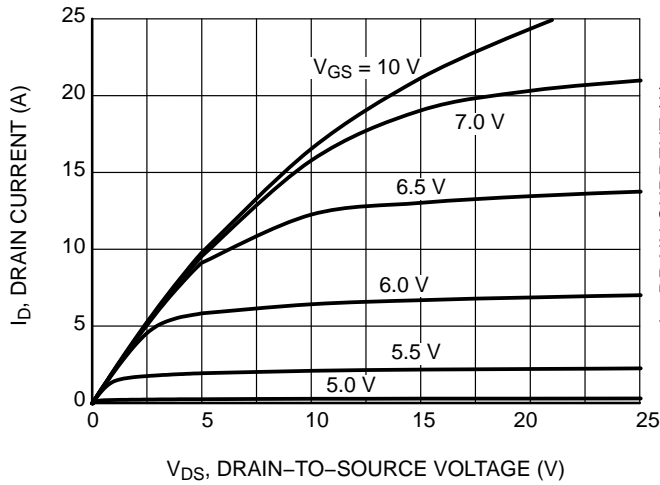


Figure 1. On-Region Characteristics

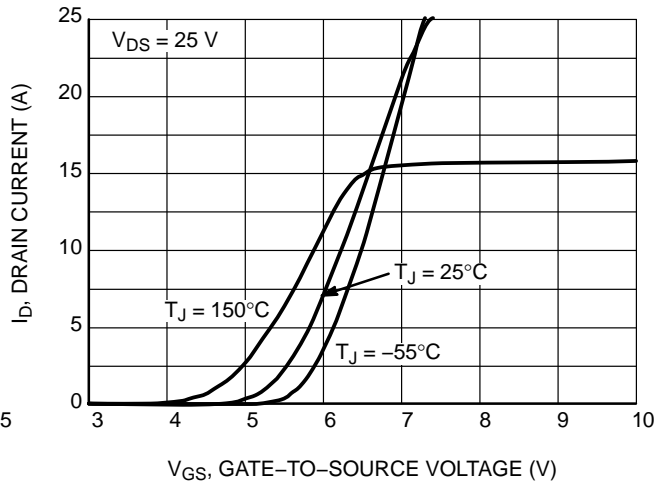


Figure 2. Transfer Characteristics

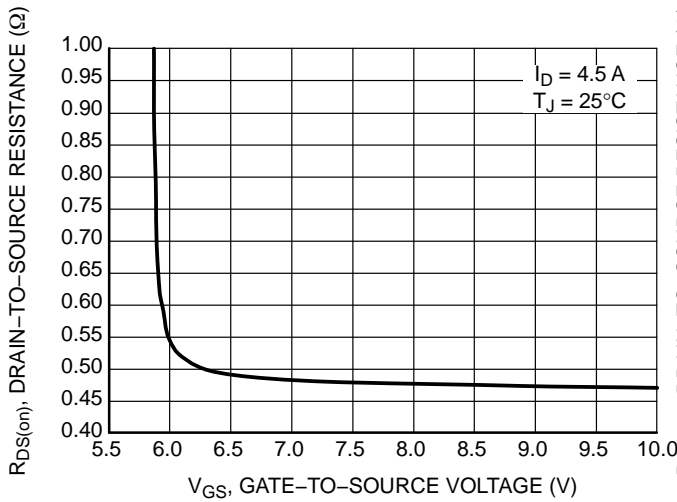


Figure 3. On-Region versus Gate-to-Source Voltage

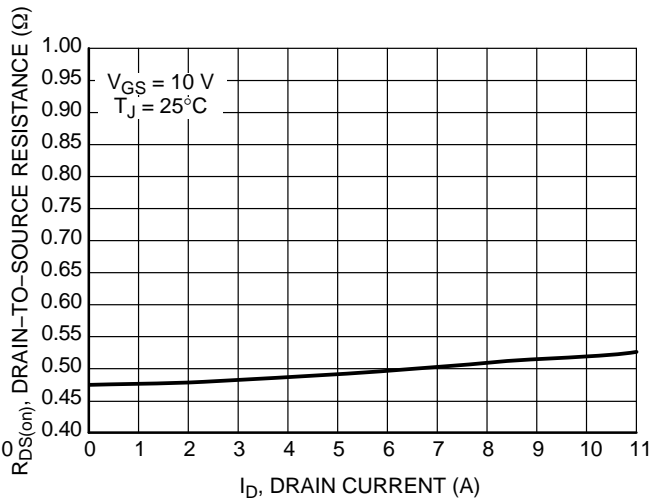


Figure 4. On-Resistance versus Drain Current and Gate Voltage

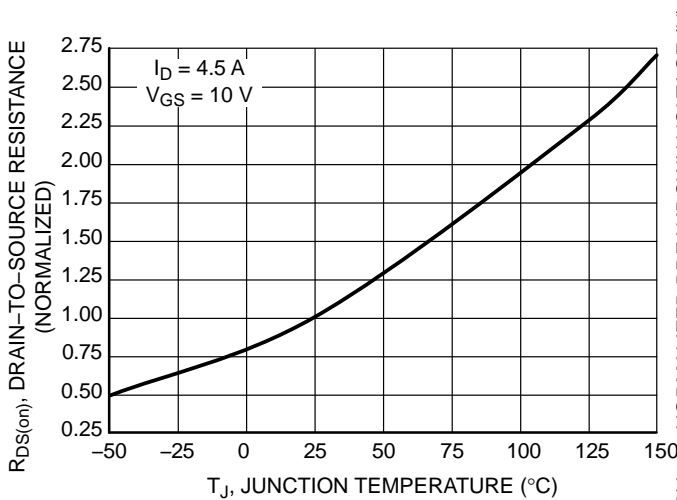


Figure 5. On-Resistance Variation with Temperature

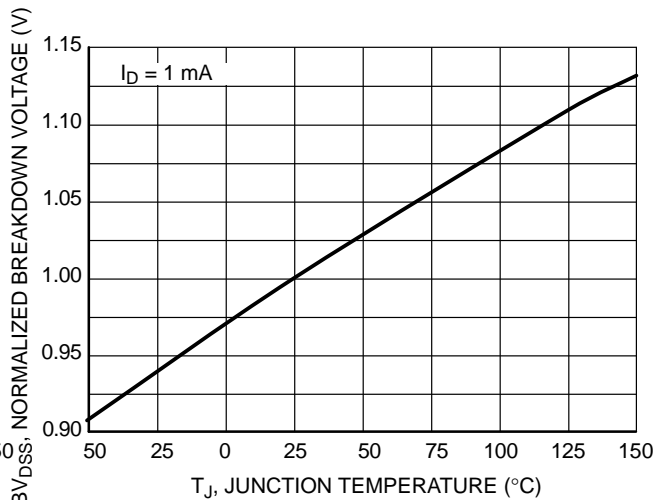


Figure 6. BV_{DSS} Variation with Temperature

NDF11N50Z

TYPICAL CHARACTERISTICS

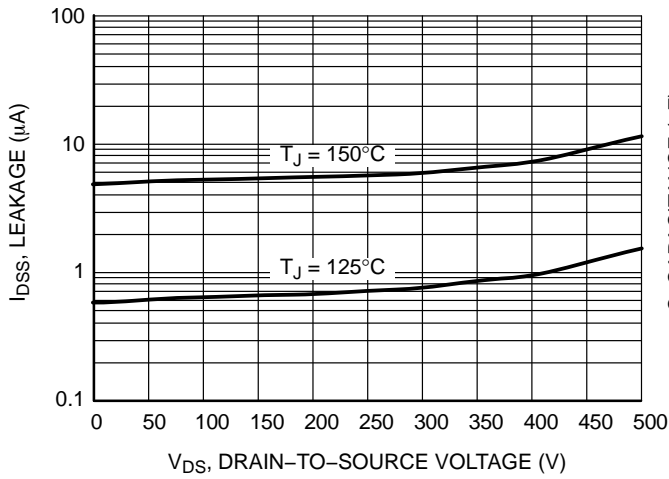


Figure 7. Drain-to-Source Leakage Current versus Voltage

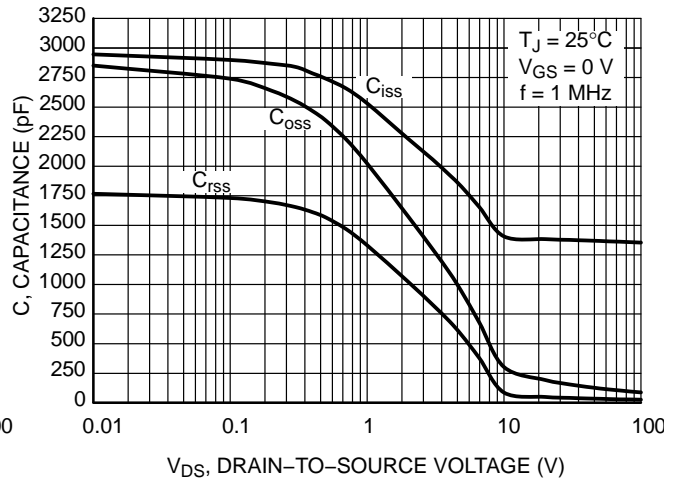


Figure 8. Capacitance Variation

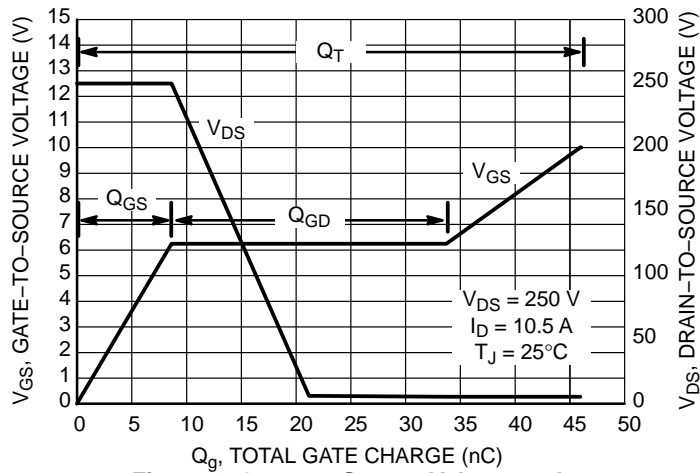


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

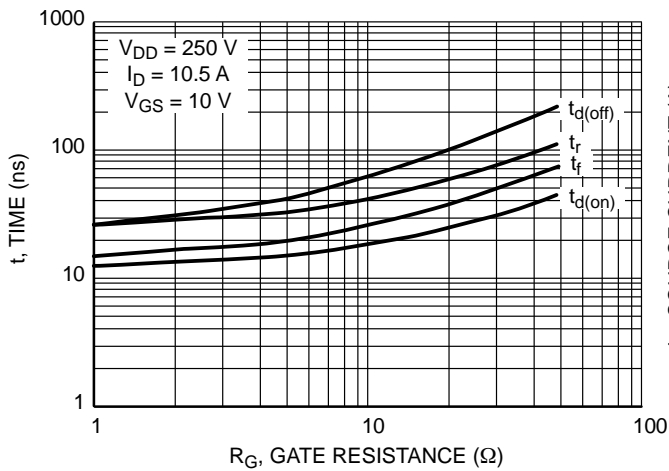


Figure 10. Resistive Switching Time Variation versus Gate Resistance

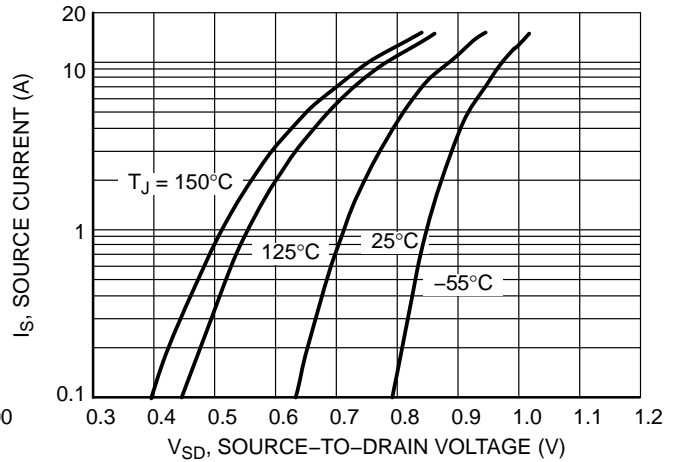


Figure 11. Diode Forward Voltage versus Current

NDF11N50Z

TYPICAL CHARACTERISTICS

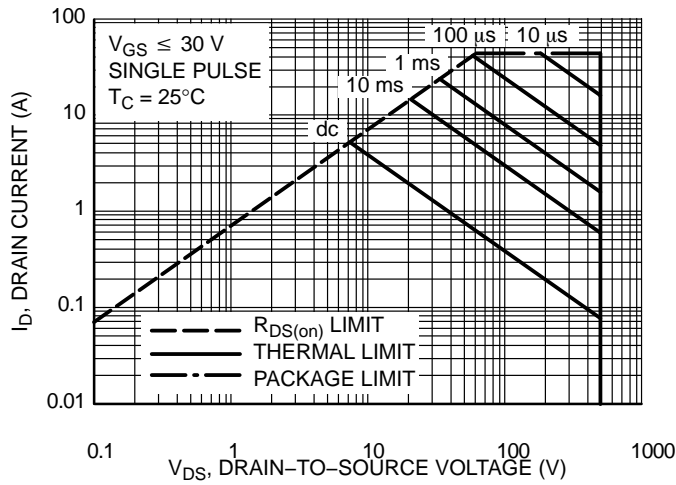


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDF11N50Z

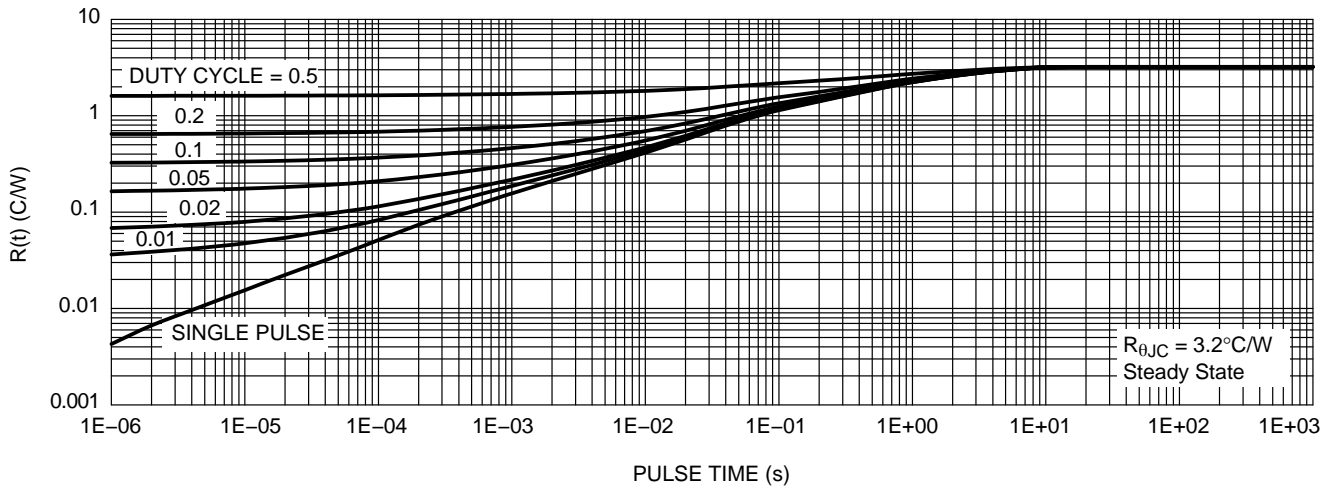


Figure 13. Thermal Impedance (Junction-to-Case) for NDF11N50Z

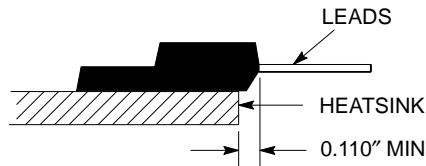


Figure 14. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NDF11N50Z

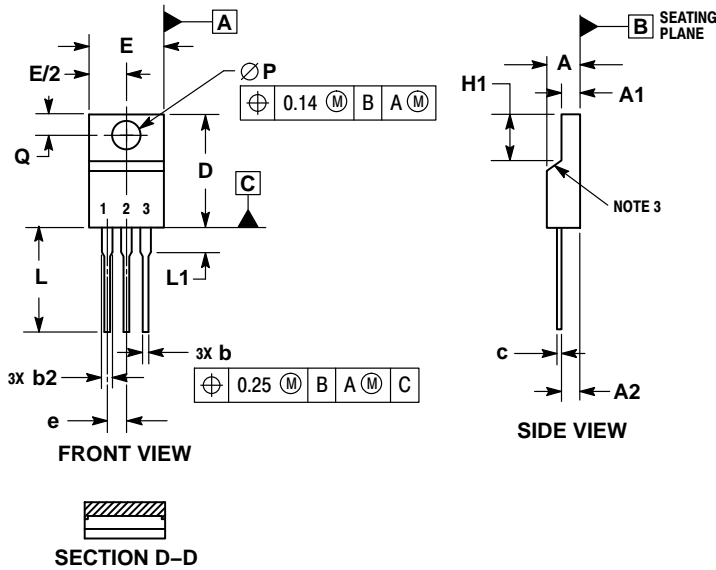
ORDERING INFORMATION

Order Number	Package	Shipping
NDF11N50ZG	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDF11N50ZH	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail

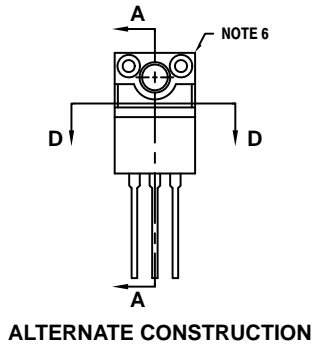
NDF11N50Z

PACKAGE DIMENSIONS

TO-220 FULLPACK, 3-LEAD CASE 221AH ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. CONTOUR UNCONTROLLED IN THIS AREA.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
 5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
 6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.



ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NDF11N50ZH on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management