PHP/PHU66NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 06 — 12 August 2004 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Low on-state resistance.

1.3 Applications

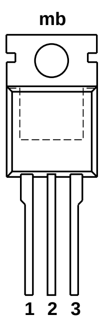
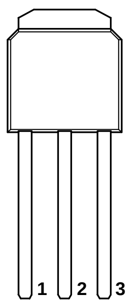
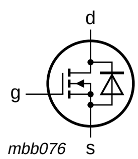
- DC-to-DC converters
- General purpose switching.

1.4 Quick reference data

- $V_{DS} \leq 25$ V
- $R_{DSon} \leq 10.5$ mΩ
- $I_D \leq 66$ A
- $Q_{gd} = 3.6$ nC (typ).

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline		Symbol
1	gate (g)	 SOT78 (TO-220AB)	 Top view SOT533 (I-PAK)	
2	drain (d)			
3	source (s)			
mb	mounting base; connected to drain (d)			

3. Ordering information

Table 2: Ordering information

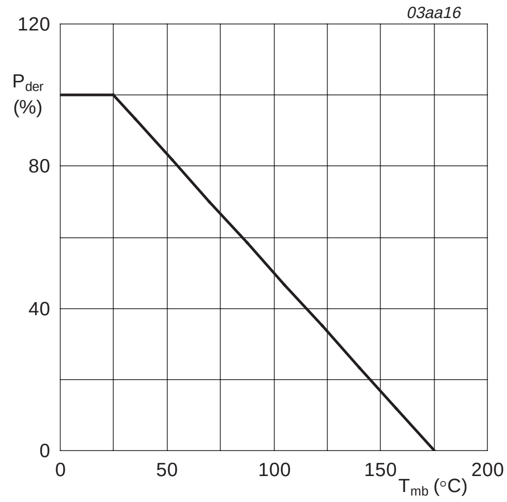
Type number	Package		
	Name	Description	Version
PHP66NQ03LT	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 lead TO-220AB	SOT78
PHU66NQ03LT	I-PAK	Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line)	SOT533

4. Limiting values

Table 3: Limiting values

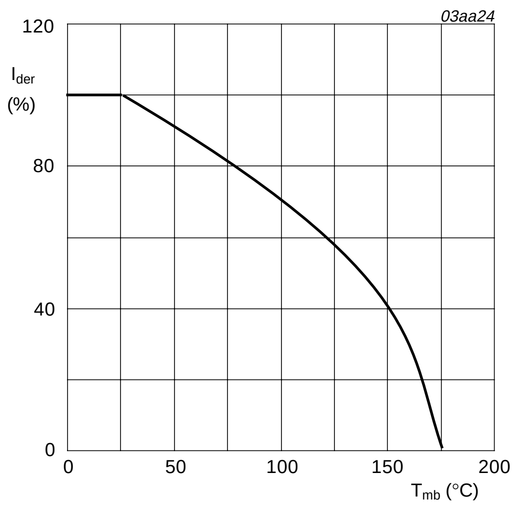
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	25	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	-	57	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	-	40	A
		T_{mb} = 25 °C; V_{GS} = 10 V	-	66	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	45	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	228	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	93	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	57	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	228	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 43 A; t_p = 0.15 ms; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	90	mJ



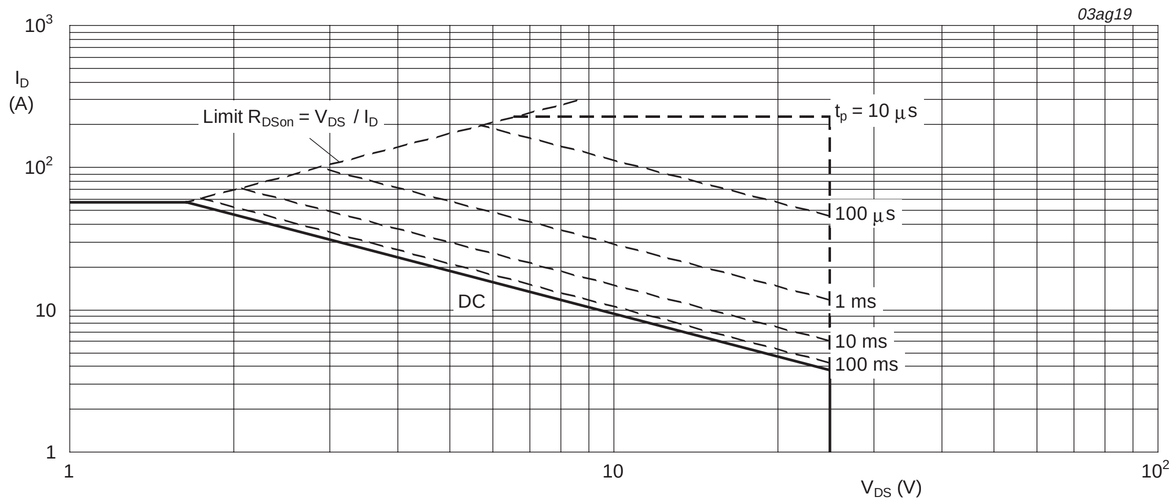
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 5 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in free air	-	60	-	K/W
	SOT533		-	70	-	K/W

5.1 Transient thermal impedance

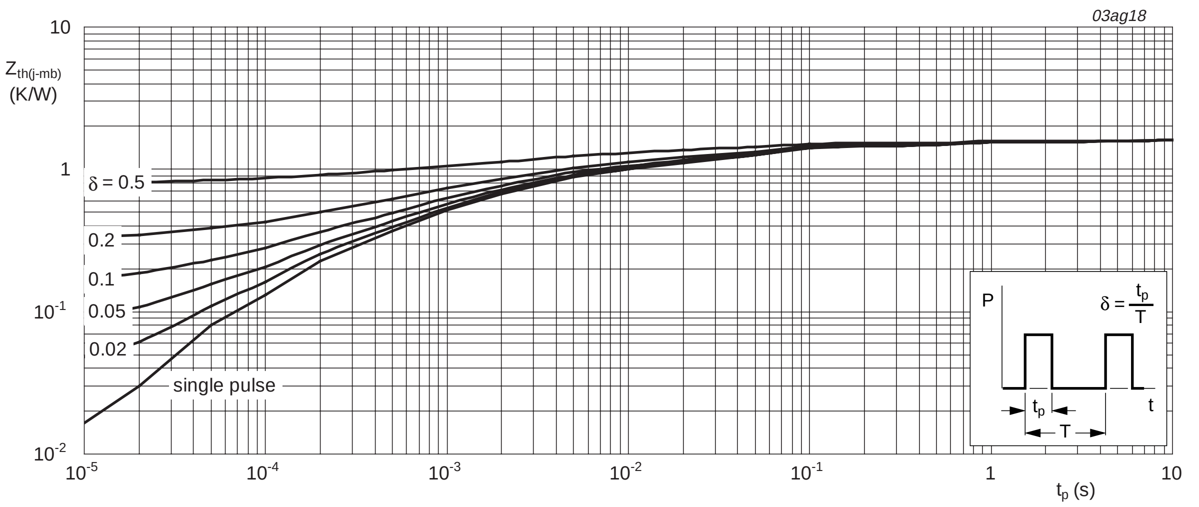


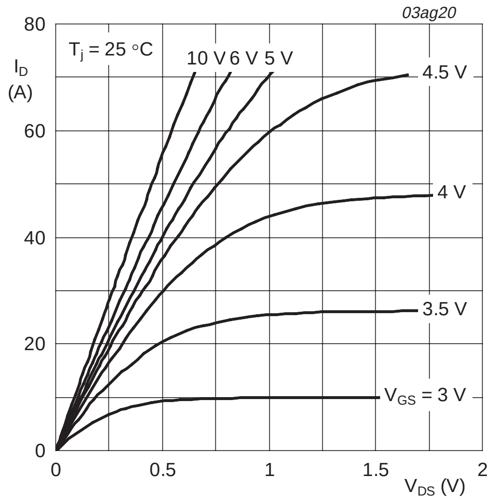
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

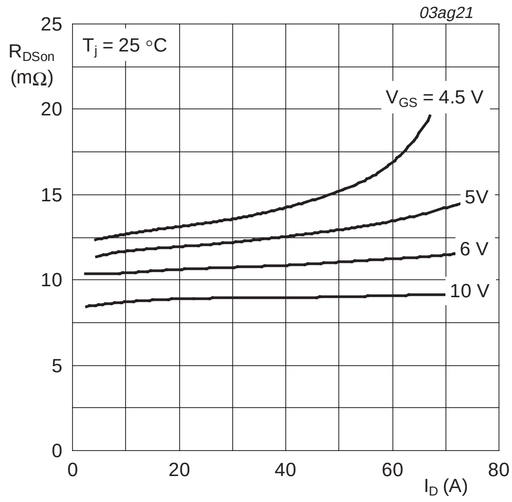
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	25	-	-	V
		T_j = −55 °C	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = −55 °C	-	-	2.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 25 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; Figure 6 and 8				
		T_j = 25 °C	-	9.1	10.5	mΩ
		T_j = 175 °C	-	16.4	18.9	mΩ
		V_{GS} = 5 V; I_D = 25 A; Figure 6 and 8	-	11.2	13.6	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 50 A; V_{DS} = 15 V; V_{GS} = 5 V; Figure 11	-	12	-	nC
Q_{gs}	gate-source charge		-	4.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 13	-	860	-	pF
C_{oss}	output capacitance		-	330	-	pF
C_{rss}	reverse transfer capacitance		-	145	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 5 V; R_G = 5.6 Ω	-	15	25	ns
t_r	rise time		-	90	135	ns
$t_{d(off)}$	turn-off delay time		-	25	40	ns
t_f	fall time		-	25	40	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 12	-	0.95	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = −100 A/µs; V_{GS} = 0 V; V_R = 25 V	-	32	-	ns
Q_r	recovered charge		-	20	-	nC



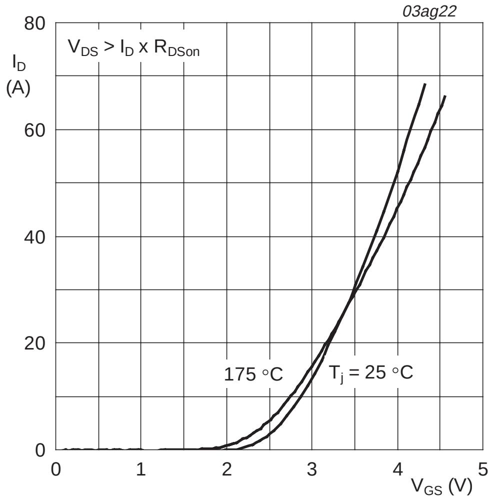
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



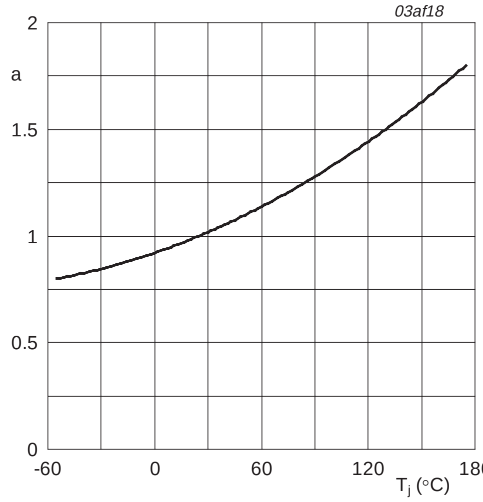
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



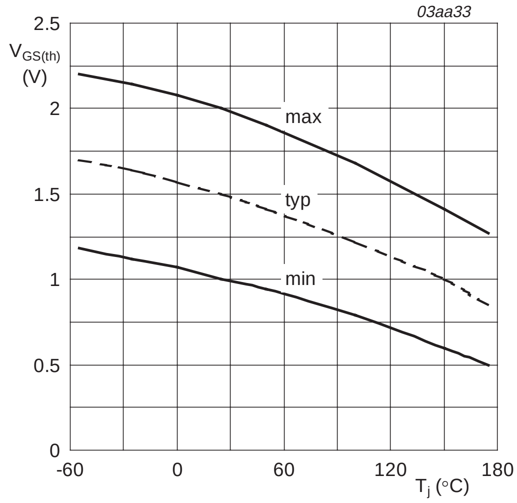
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



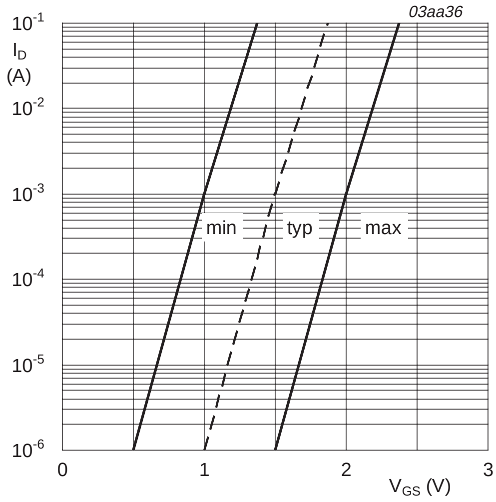
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



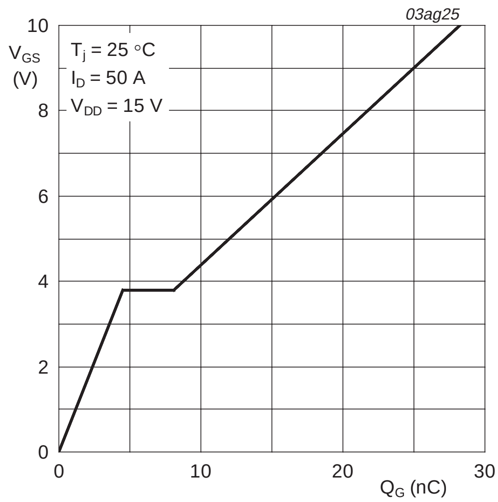
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



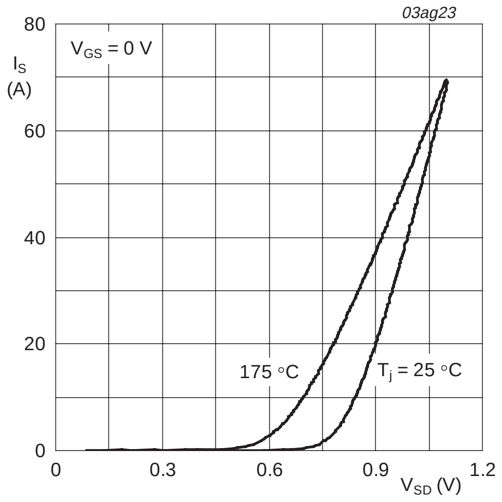
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



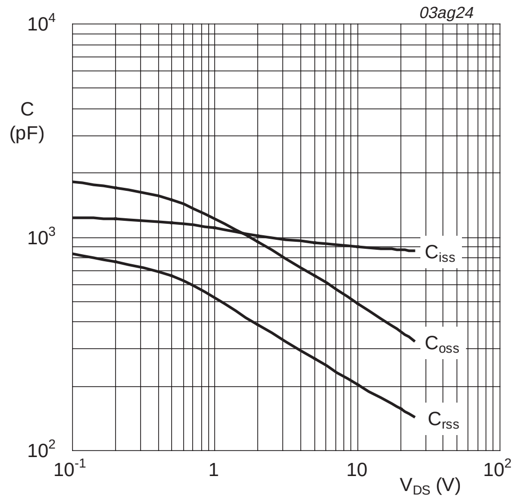
I_D = 50 A; V_{DS} = 15 V

Fig 11. Gate-source voltage as a function of gate charge; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

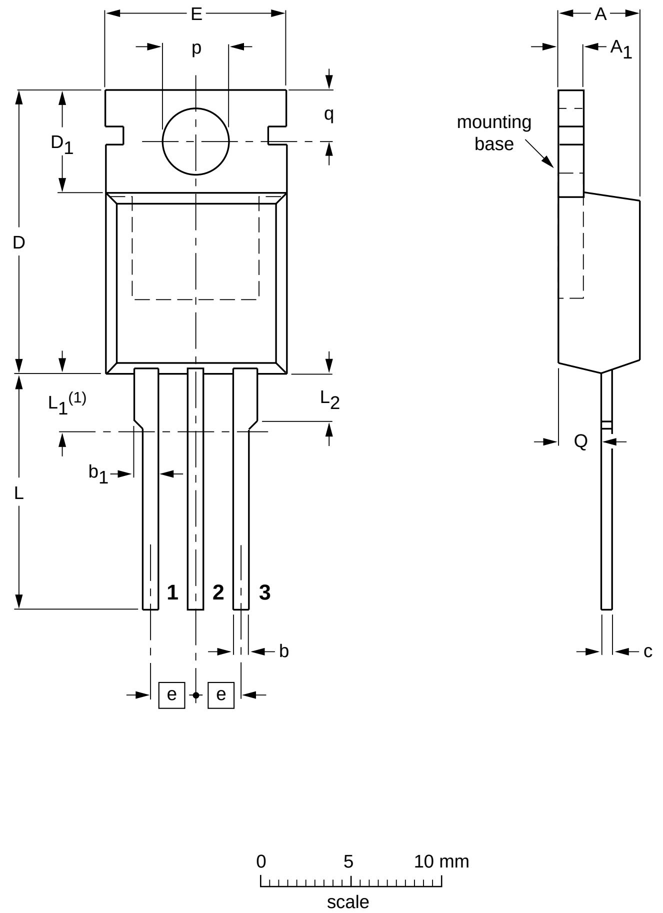


V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	$L_1^{(1)}$	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.6	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

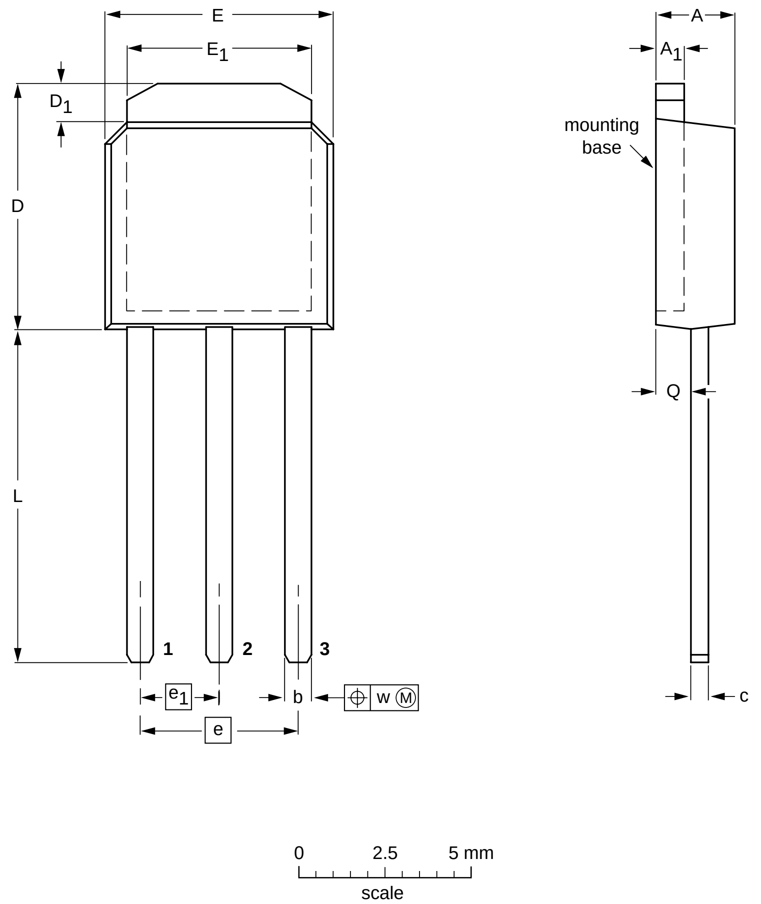
Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~01-02-16~~ 03-01-22

Fig 14. SOT78 (TO-220AB) package outline.

Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line) **SOT533**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	E	E_1	e	e_1	L	Q
mm	2.38 2.22	0.89 0.71	0.89 0.71	0.56 0.46	7.28 6.94	1.06 0.96	6.73 6.47	5.36 5.26	4.57	2.285	9.8 9.4	1.00 1.10

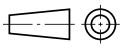
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT533		TO-251				99-02-18

Fig 15. SOT533 (I-PAK) package outline.

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Document number	Supersedes
PHP_PHU66NQ03LT_6	20040812	Product data sheet	-	9397 750 13428	PHP_PHB_PHD66NQ03LT_5
Modifications:	• Removal of PHB66NQ03LT (now in separate data sheet) • Removal of PHD66NQ03LT (now in separate data sheet) • Addition of PHU66NQ03LT. • Data sheet updated to latest standard.				
PHP_PHB_PHD66NQ03LT_5	20040415	Product data sheet	-	9397 750 13107	PHP_PHB_PHD66NQ03LT_4
PHP_PHB_PHD66NQ03LT_4	20020909	Product data sheet	-	9397 750 10158	PHP_PHB_PHD66NQ03LT_3
PHP_PHB_PHD66NQ03LT_3	20020312	Product data sheet	-	9397 750 09284	PHP_PHB_PHD66NQ03LT_2
PHP_PHB_PHD66NQ03LT_2	20011210	Product data sheet	-	9397 750 09119	PHP_PHB_PHD66NQ03LT_1
PHP_PHB_PHD66NQ03LT_1	20011012	Product data sheet	-	9397 750 08725	-

9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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14. Contents

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