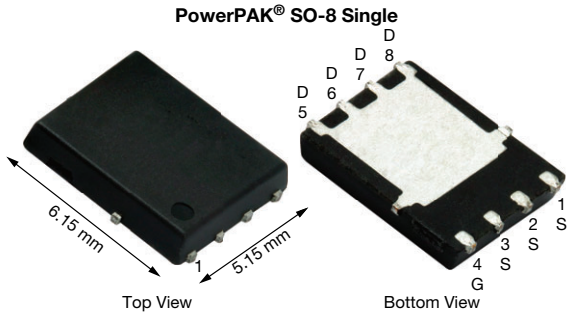
THE DATASHEET OF

SI7462DP-T1-E3

N-Channel 200 V (D-S) MOSFET



FEATURES

- TrenchFET® power MOSFETs
- New low thermal resistance PowerPAK® package with low 1.07 mm profile
- PWM optimized for fast switching

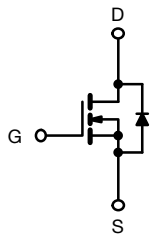
Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Primary side switch



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	200
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.130
$R_{DS(on)}$ max. (Ω) at V_{GS} = 6 V	0.142
Q_g typ. (nC)	20
I_D (A)	4.1
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free	Si7462DP-T1-E3
Lead (Pb)-free and halogen-free	Si7462DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	10 s	STEADY STATE	UNIT
Drain-source voltage		V_{DS}	200	200	V
Gate-source voltage		V_{GS}	± 20	± 20	
Continuous drain current (T_J = 150 °C) [a]	T_A = 25 °C	I_D	4.1	2.6	A
	T_A = 85 °C		3	1.9	
Pulsed drain current		I_{DM}	12	12	
Avalanche current	L = 0.1 mH	I_{AS}	6	6	
Single avalanche energy (duty cycle ≤ 1 %)		E_{AS}	1.8	1.8	mJ
Continuous source current (diode conduction) [a]		I_S	4	1.6	A
Maximum power dissipation [a]	T_A = 25 °C	P_D	4.8	1.9	W
	T_A = 85 °C		2.6	1	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [b, c]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a]	t ≤ 10 s	R_{thJA}	21	26	°C/W
	Steady state		55	65	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.7	2.1	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	-	4	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 85 °C	-	-	20	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	12	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.1 A	-	0.110	0.130	Ω
		V_{GS} = 6 V, I_D = 3.9 A	-	0.120	0.142	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 4.1 A	-	13	-	S
Diode forward voltage [a]	V_{SD}	I_S = 4 A, V_{GS} = 0 V	-	0.8	1.2	V
Dynamic [b]						
Total gate charge	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 4.1 A	-	20	30	nC
Gate-source charge	Q_{gs}		-	4.5	-	
Gate-drain charge	Q_{gd}		-	6.5	-	
Gate resistance	R_g		-	2	-	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 100 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 6 Ω	-	15	25	ns
Rise time	t_r		-	15	25	
Turn-off delay time	$t_{d(off)}$		-	40	60	
Fall time	t_f		-	20	30	
Source-drain reverse recovery time	t_{rr}	I_F = 4 A, di/dt = 100 A/µs	-	70	110	

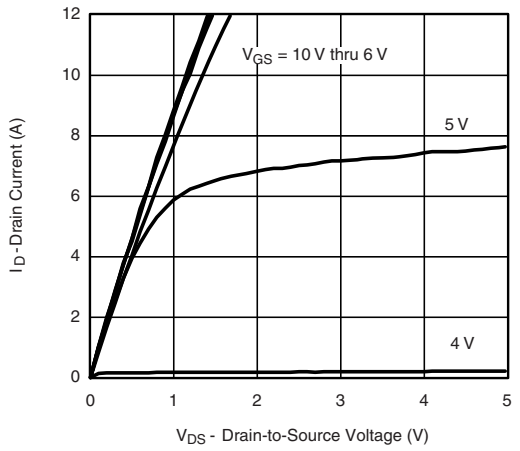
Notes

a. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2 %

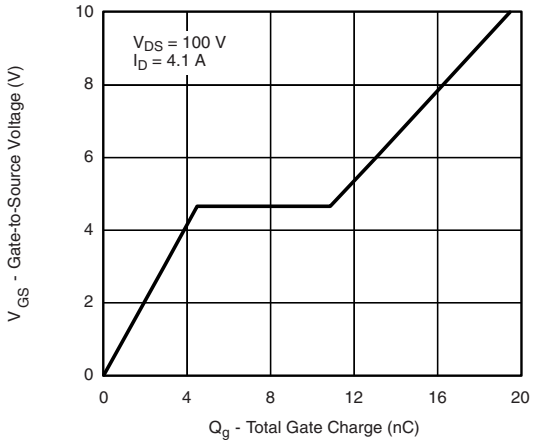
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

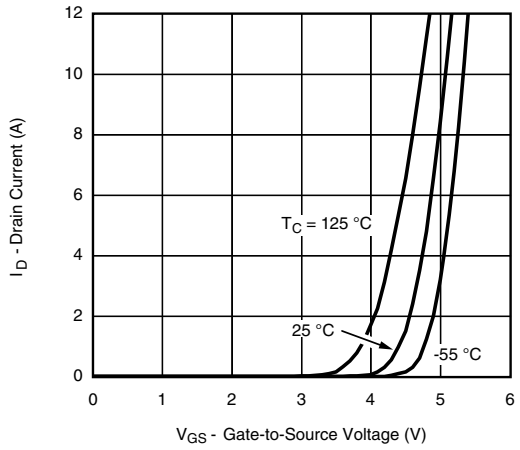
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



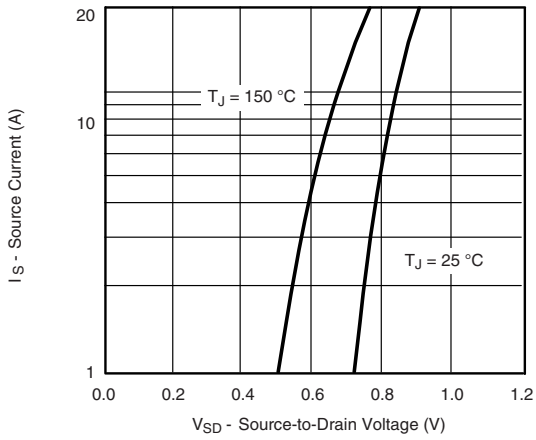
Output Characteristics



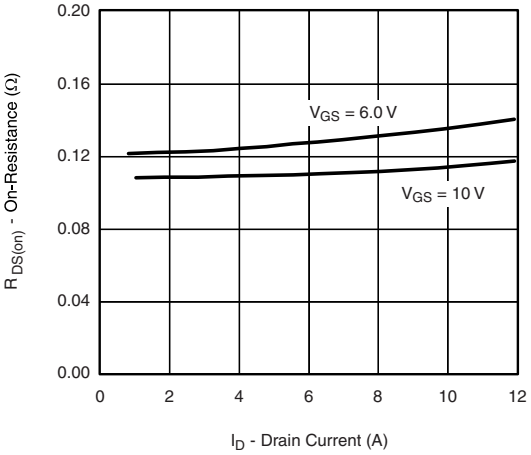
Gate Charge



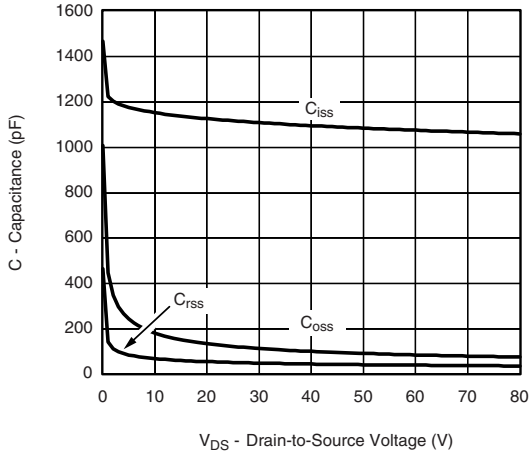
Transfer Characteristics



Source-Drain Diode Forward Voltage

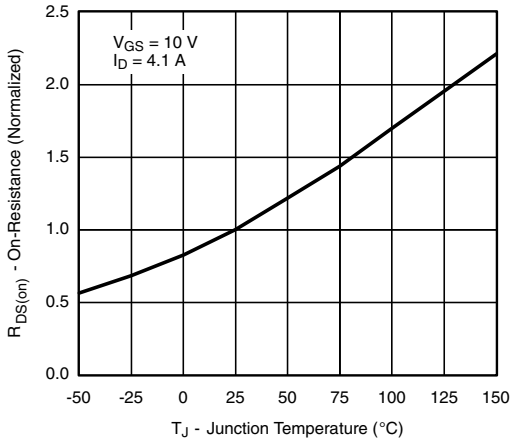


On-Resistance vs. Drain Current

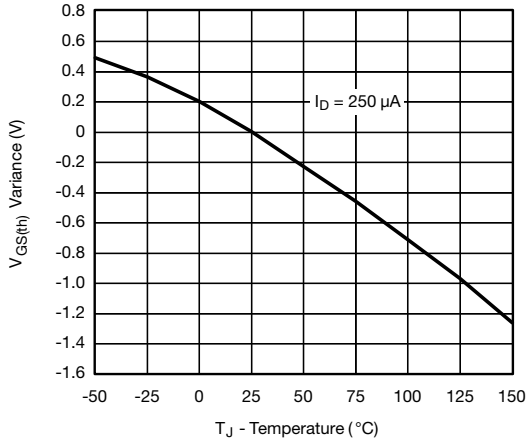


Capacitance

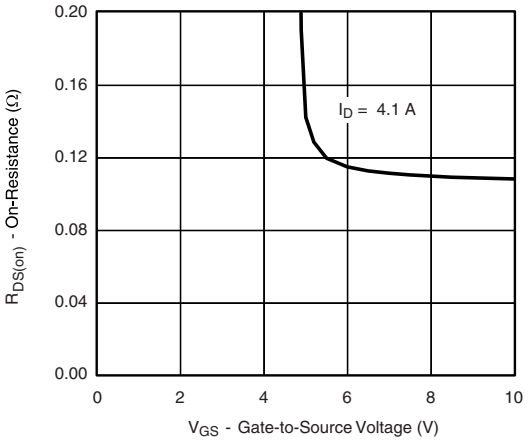
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



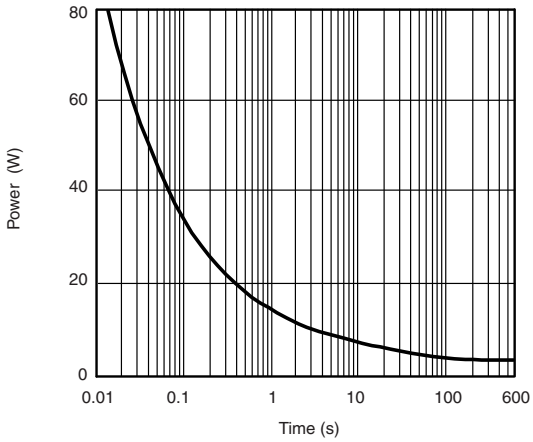
On-Resistance vs. Junction Temperature



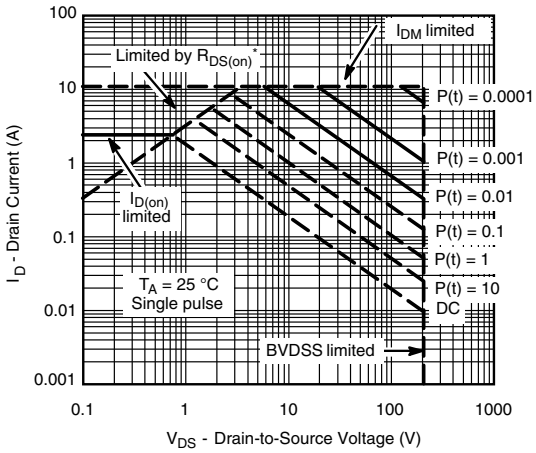
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

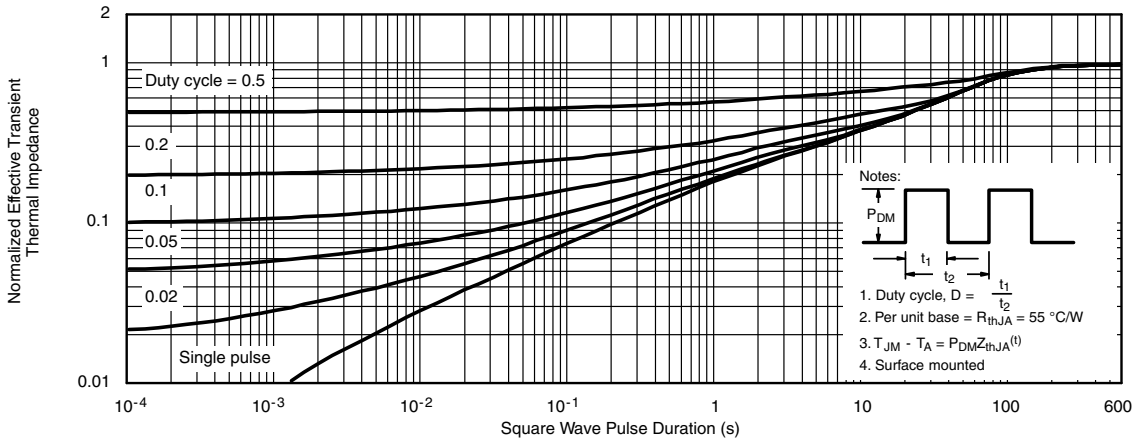


Single Pulse Power

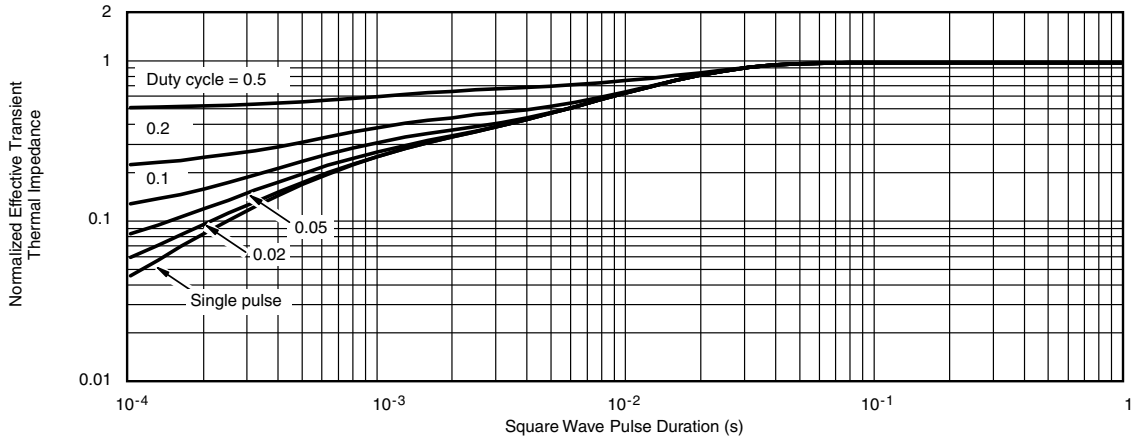


Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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