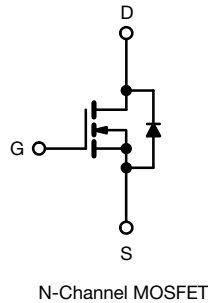
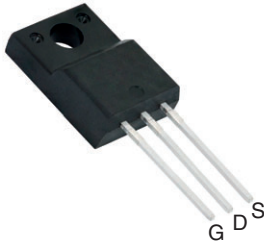


E Series Power MOSFET

Thin-Lead TO-220 FULLPAK


FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Consumer
 - Adaptors
 - Televisions
 - Game console
- Computing
 - Adaptors
 - ATX power supply

PRODUCT SUMMARY

| | | |
|---|-----------------|------|
| V_{DS} (V) at T_J max. | 650 | |
| $R_{DS(on)}$ max. (Ω) at 25 °C | $V_{GS} = 10$ V | 0.38 |
| Q_g max. (nC) | 58 | |
| Q_{gs} (nC) | 6 | |
| Q_{gd} (nC) | 13 | |
| Configuration | Single | |

ORDERING INFORMATION

| | |
|---------------------------------|--------------------------|
| Package | Thin-Lead TO-220 FULLPAK |
| Lead (Pb)-free | SiHA12N60E-E3 |
| Lead (Pb)-free and halogen-free | SiHA12N60E-GE3 |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|------------------|----------------|------|
| Drain-source voltage | V_{DS} | 600 | V |
| Gate-source voltage | V_{GS} | ± 30 | |
| Continuous drain current ($T_J = 150$ °C) ^e | V_{GS} at 10 V | $T_C = 25$ °C | 12 |
| | | $T_C = 100$ °C | 7.8 |
| Pulsed drain current ^a | I_{DM} | 27 | A |
| Linear derating factor | | 0.26 | |
| Single pulse avalanche energy ^b | E_{AS} | 117 | mJ |
| Maximum power dissipation | P_D | 33 | W |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C |
| Drain-source voltage slope | dV/dt | $T_J = 125$ °C | 70 |
| Reverse diode dV/dt ^d | | 5 | |
| Soldering recommendations (peak temperature) ^c | for 10 s | 300 | °C |
| Mounting torque | M3 screw | 0.6 | Nm |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 11.6$ mH, $R_g = 25$ Ω , $I_{AS} = 4.5$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature



| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient | R_{thJA} | - | 65 | °C/W |
| Maximum junction-to-case (drain) | R_{thJC} | - | 3.8 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|---|---|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 600 | - | - | V |
| V_{DS} temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$ | | - | 0.71 | - | V/°C |
| Gate-source threshold voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2 | - | 4 | V |
| Gate-source leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| | | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 1 | μA |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 10 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 6\text{ A}$ | - | 0.32 | 0.38 | Ω |
| Forward transconductance | g_{fs} | $V_{DS} = 40\text{ V}, I_D = 8\text{ A}$ | | - | 3.8 | - | S |
| Dynamic | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$ | | - | 937 | - | pF |
| Output capacitance | C_{oss} | | | - | 53 | - | |
| Reverse transfer capacitance | C_{rss} | | | - | 5 | - | |
| Effective output capacitance, energy related ^a | $C_{o(er)}$ | $V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$ | | - | 41 | - | pF |
| Effective output capacitance, time related ^b | $C_{o(tr)}$ | | | - | 136 | - | |
| Total gate charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 6\text{ A}, V_{DS} = 480\text{ V}$ | - | 29 | 58 | nC |
| Gate-source charge | Q_{gs} | | | - | 6 | - | |
| Gate-drain charge | Q_{gd} | | | - | 13 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 480\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 14 | 28 | ns |
| Rise time | t_r | | | - | 19 | 38 | |
| Turn-off delay time | $t_{d(off)}$ | | | - | 35 | 70 | |
| Fall time | t_f | | | - | 19 | 38 | |
| Gate input resistance | R_g | $f = 1\text{ MHz}, \text{ open drain}$ | | - | 1.1 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 12 | A |
| Pulsed diode forward current | I_{SM} | | | - | - | 48 | |
| Diode forward voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 6\text{ A}, V_{GS} = 0\text{ V}$ | | - | - | 1.2 | V |
| Reverse recovery time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 6\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$ | | - | 350 | - | ns |
| Reverse recovery charge | Q_{rr} | | | - | 4 | - | μC |
| Reverse recovery current | I_{RRM} | | | - | 19 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

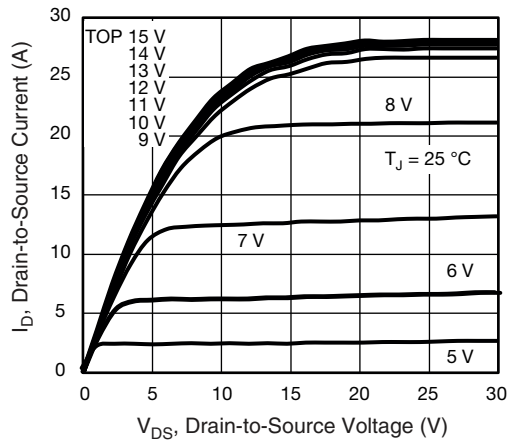


Fig. 1 - Typical Output Characteristics

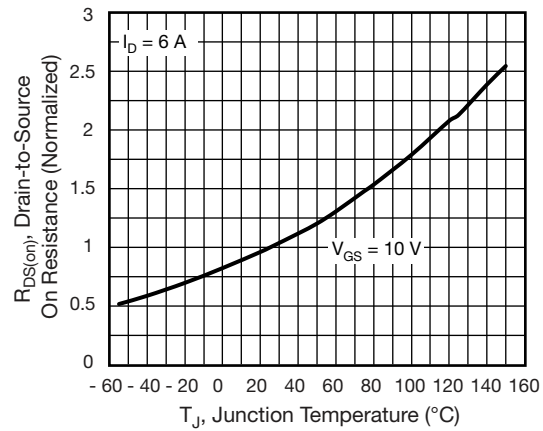


Fig. 4 - Normalized On-Resistance vs. Temperature

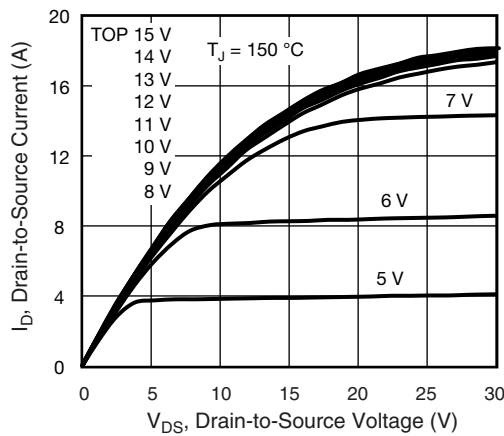


Fig. 2 - Typical Output Characteristics

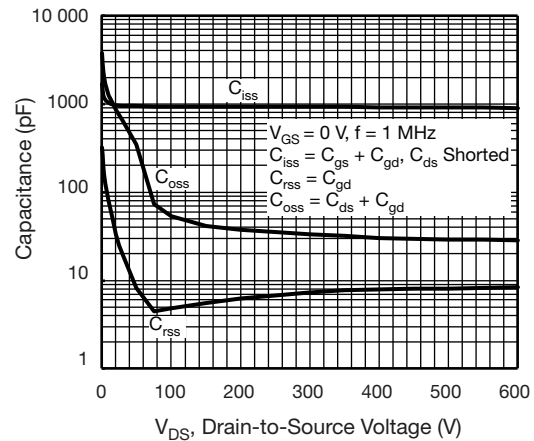


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

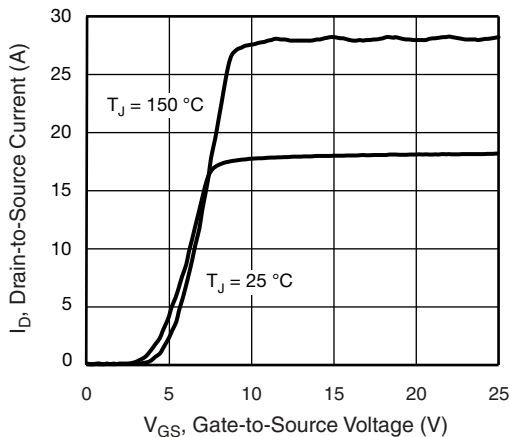


Fig. 3 - Typical Transfer Characteristics

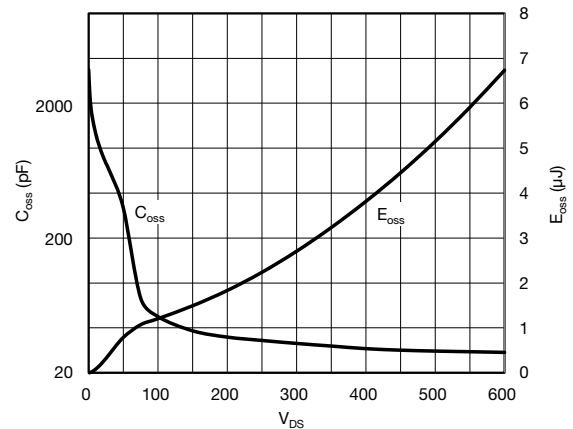


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

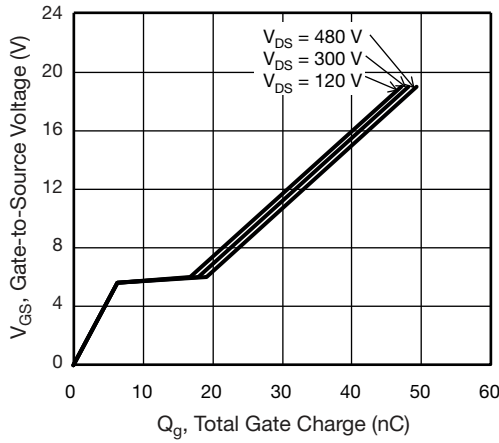


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

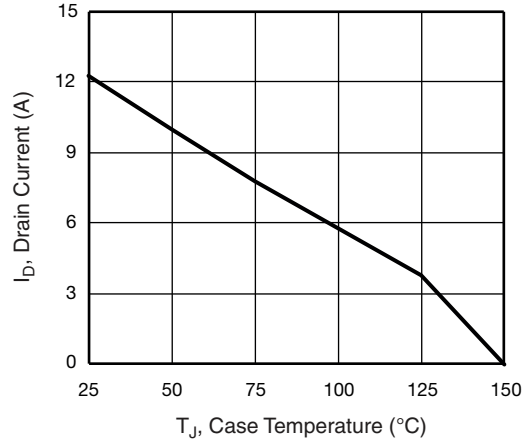


Fig. 10 - Maximum Drain Current vs. Case Temperature

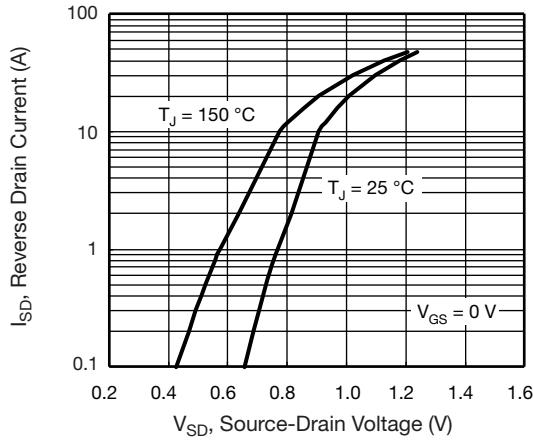


Fig. 8 - Typical Source-Drain Diode Forward Voltage

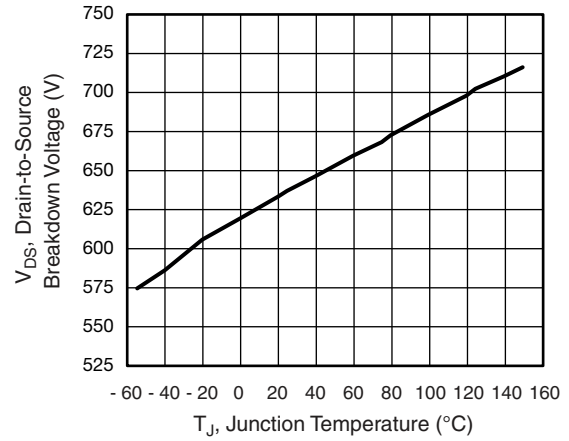


Fig. 11 - Temperature vs. Drain-to-Source Voltage

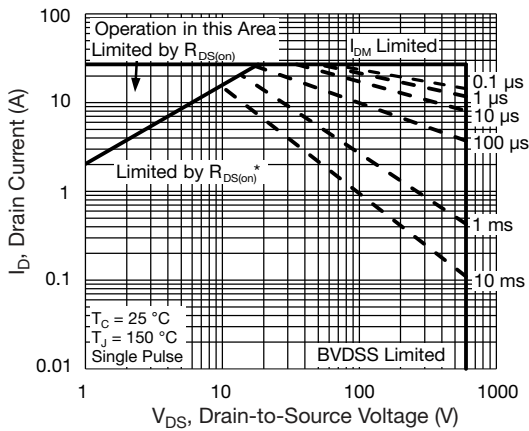


Fig. 9 - Maximum Safe Operating Area

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

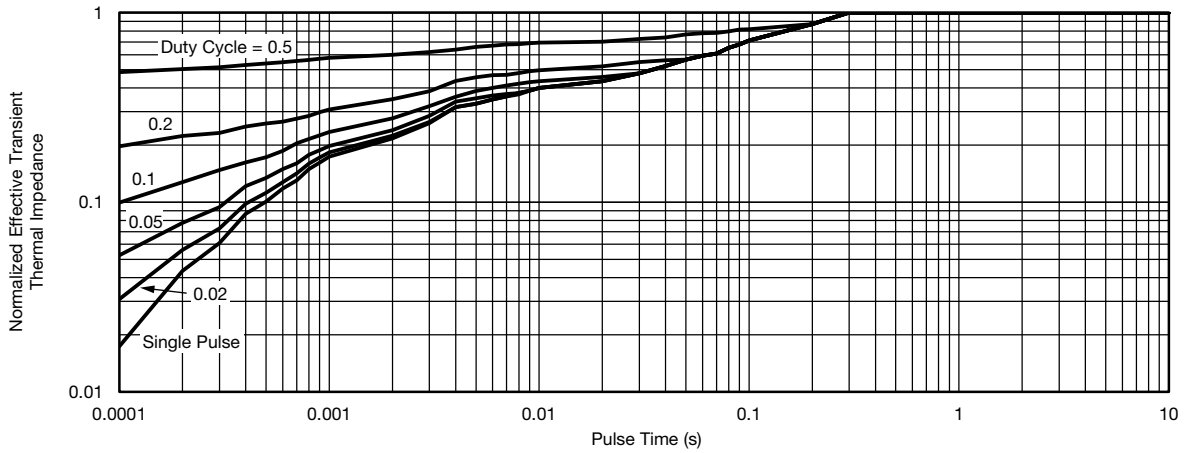


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

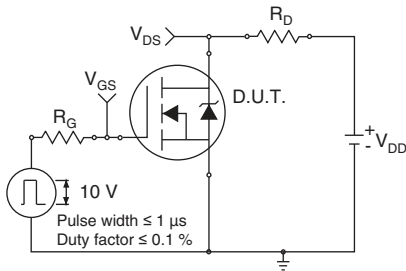


Fig. 13 - Switching Time Test Circuit

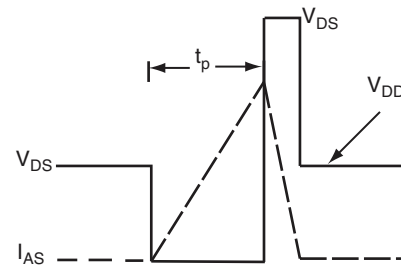


Fig. 16 - Unclamped Inductive Waveforms

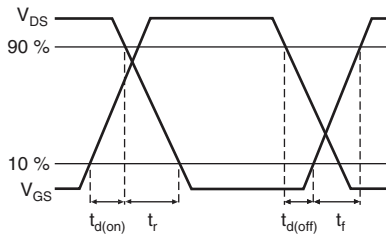


Fig. 14 - Switching Time Waveforms

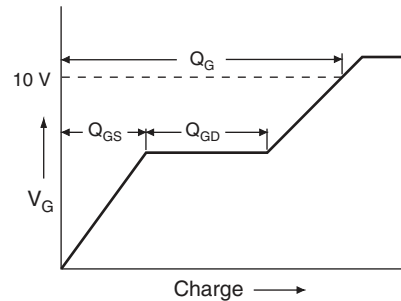


Fig. 17 - Basic Gate Charge Waveform

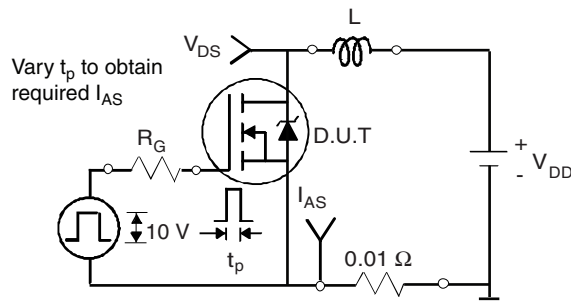


Fig. 15 - Unclamped Inductive Test Circuit

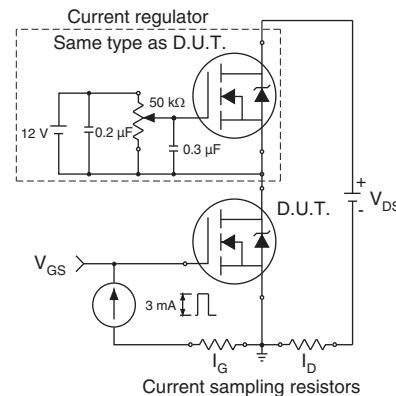
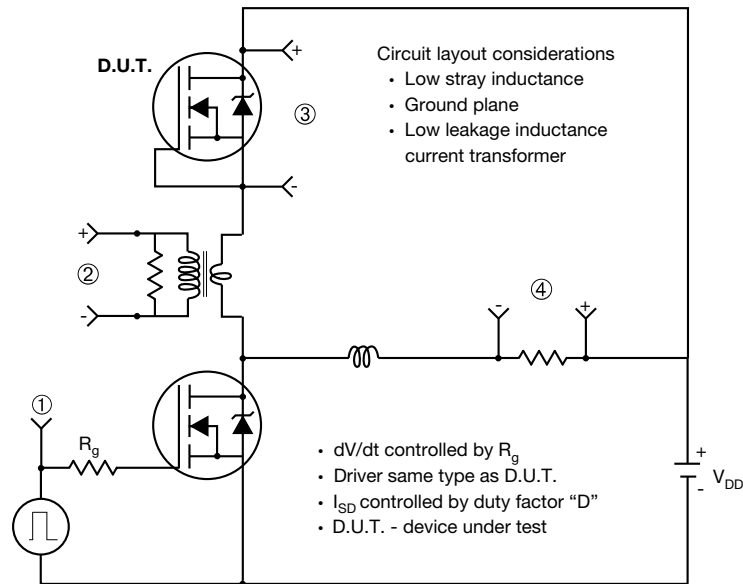


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

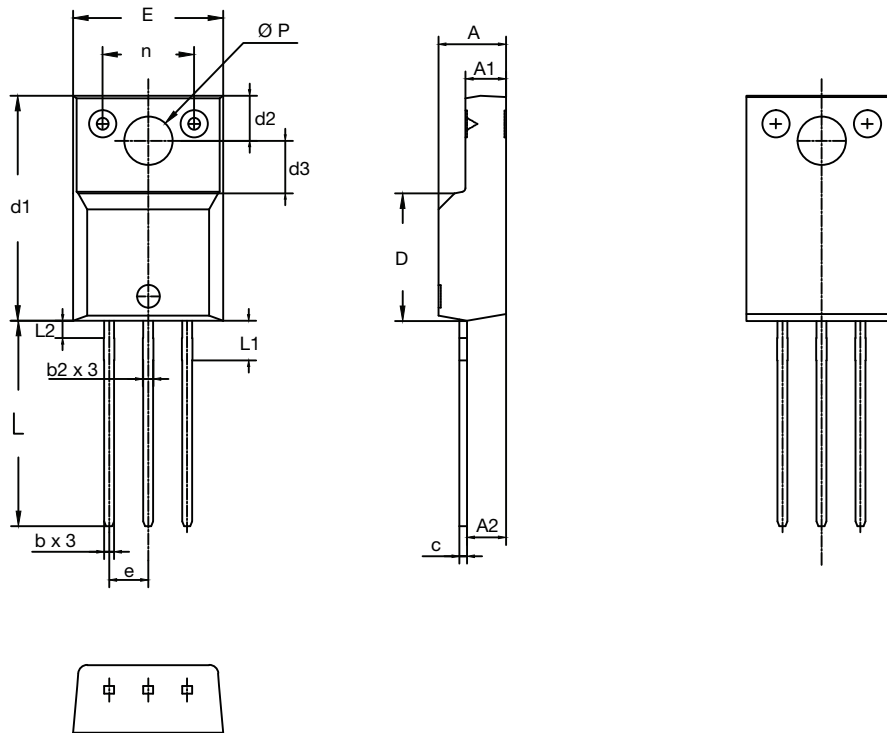
a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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TO-220 FULLPAK Thin Lead



| SYMBOL | DIMENSIONS | | | |
|--------|-------------|-------|--------|-------|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.30 | 4.70 | 0.169 | 0.185 |
| A1 | 2.50 | 2.90 | 0.098 | 0.114 |
| A2 | 2.50 | 2.70 | 0.098 | 0.106 |
| b | 0.60 | 0.80 | 0.024 | 0.031 |
| b2 | 0.60 | 0.90 | 0.024 | 0.035 |
| c | - | 0.60 | - | 0.024 |
| D | 8.30 | 8.70 | 0.327 | 0.342 |
| d1 | 14.70 | 15.30 | 0.579 | 0.602 |
| d2 | 2.90 | 3.10 | 0.114 | 0.122 |
| d3 | 3.40 | 3.60 | 0.134 | 0.142 |
| E | 9.70 | 10.30 | 0.382 | 0.406 |
| e | 2.50 | 2.70 | 0.098 | 0.106 |
| L | 13.40 | 13.80 | 0.528 | 0.543 |
| L1 | 2.50 | 2.80 | 0.098 | 0.110 |
| L2 | - | 1.20 | - | 0.047 |
| n | 6.05 | 6.15 | 0.238 | 0.242 |
| Ø P | 3.00 | 3.40 | 0.118 | 0.134 |

ECN: T16-0549-Rev. C, 12-Sep-16
 DWG: 6021



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