



**THE DATASHEET OF  
SIHP12N50C-E3**



## Power MOSFET

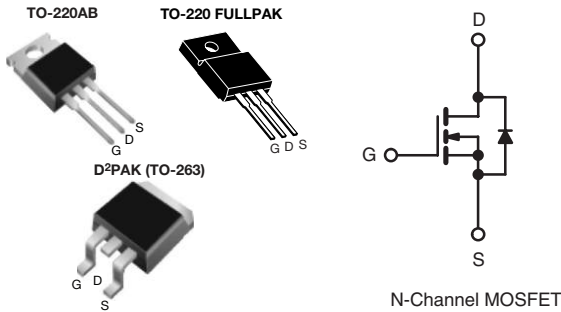
PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	560 V
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V   0.555
$Q_g$ (Max.) (nC)	48
$Q_{gs}$ (nC)	12
$Q_{gd}$ (nC)	15
Configuration	Single

### FEATURES

- Low Figure-of-Merit  $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- $T_{rr}/Q_{rr}$  Improved
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT



ORDERING INFORMATION			
Package	TO-220AB	D <sup>2</sup> PAK (TO-263)	TO-220 FULLPAK
Lead (Pb)-free	SiHP12N50C-E3	SiHB12N50C-E3	SiHF12N50C-E3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT		UNIT
		TO220-AB D <sup>2</sup> PAK (TO-263)	TO-220 FULLPAK	
Drain-Source Voltage	$V_{DS}$	500		V
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$V_{GS}$ at 10 V	$T_C = 25^\circ\text{C}$	12
			$T_C = 100^\circ\text{C}$	
Pulsed Drain Current <sup>c</sup>	$I_{DM}$	28		A
Linear Derating Factor		1.67	0.28	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	180		mJ
Maximum Power Dissipation	$P_D$	208	36	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s	300		

### Notes


- Limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25^\circ\text{C}$ ,  $L = 2.5$  mH,  $R_g = 25 \Omega$ ,  $I_{AS} = 12$  A.
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TO220-AB D <sup>2</sup> PAK (TO-263)	TO-220 FULLPAK	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	62	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.6	3.5	
Junction-to-Ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	40	-	

### Note

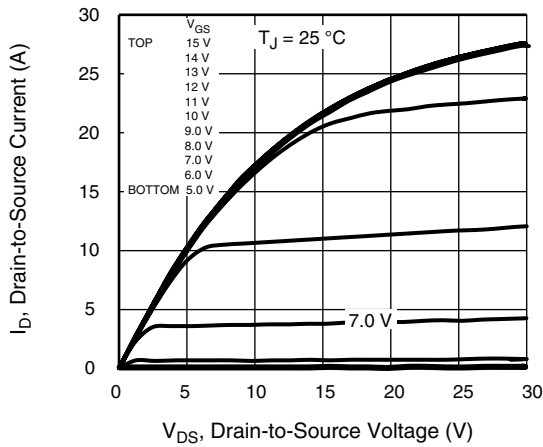
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A}$	-	0.46	0.555	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3\text{ A}$		-	3	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$		-	1375	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	165	-	
Reverse Transfer Capacitance	$C_{rss}$			-	17	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 400\text{ V}$	-	32	48	nC
Gate-Source Charge	$Q_{gs}$			-	12	-	
Gate-Drain Charge	$Q_{gd}$			-	15	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 10\text{ A}, R_g = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}$		-	18	-	ns
Rise Time	$t_r$			-	35	-	
Turn-Off Delay Time	$t_{d(off)}$			-	23	-	
Fall Time	$t_f$			-	6	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$		-	1.1	-	$\Omega$
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	12	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	28	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S, dI/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$		-	580	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	4.3	-	$\mu\text{C}$
Body Diode Reverse Recovery Current	$I_{RRM}$			-	13	-	A

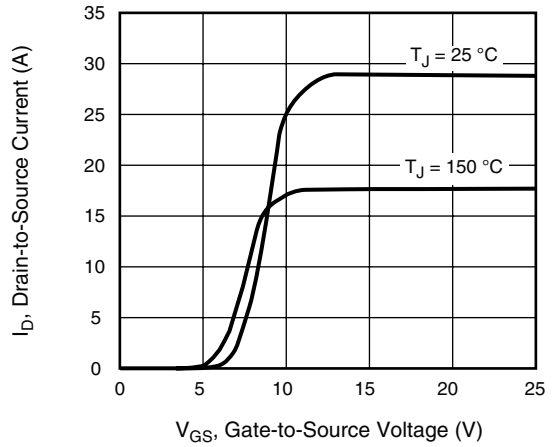
### Note

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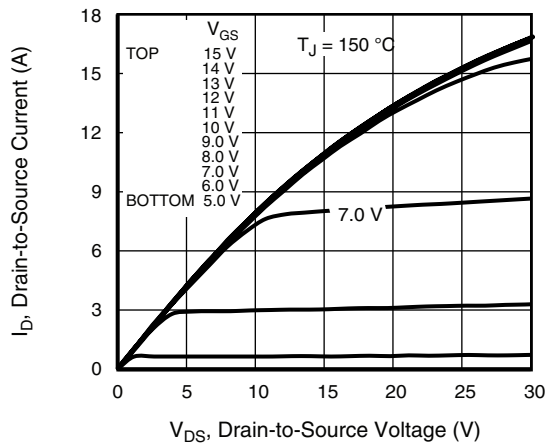
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



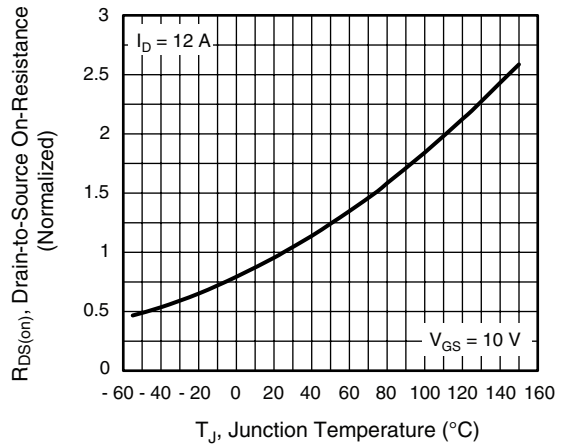
**Fig. 1 - Typical Output Characteristics (TO-220)**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics (TO-220)**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

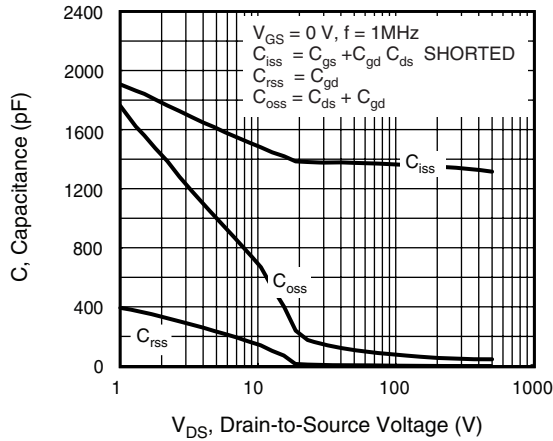


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

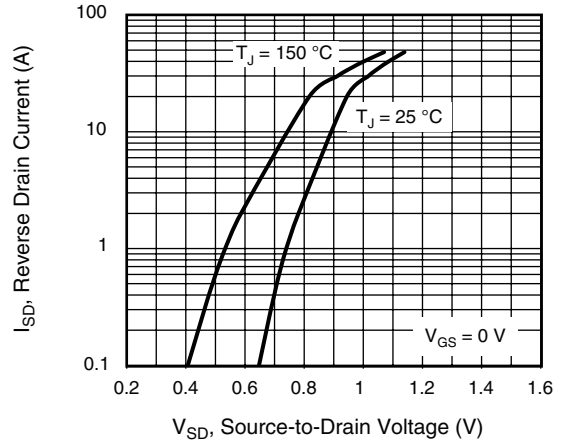


Fig. 7 - Typical Source-Drain Diode Forward Voltage

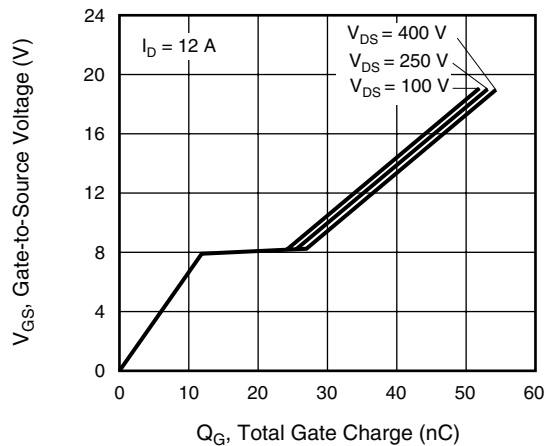


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

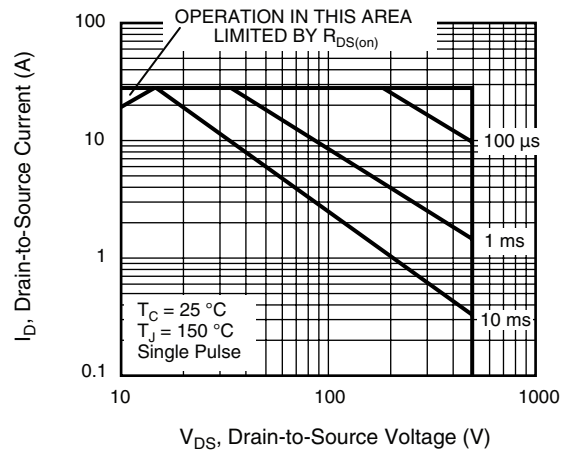


Fig. 8 - Maximum Safe Operating Area (TO-220AB, D2PAK)

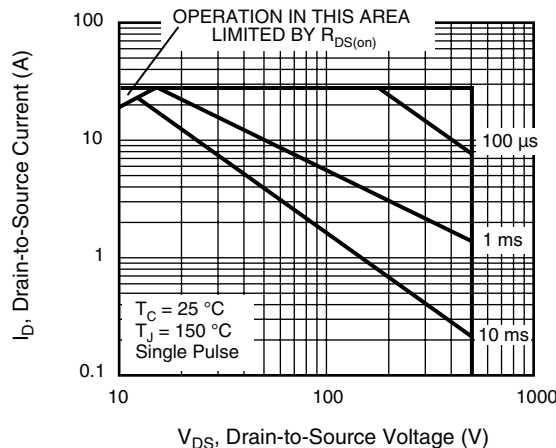
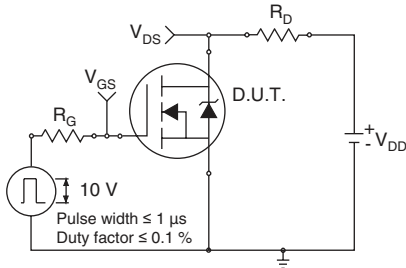
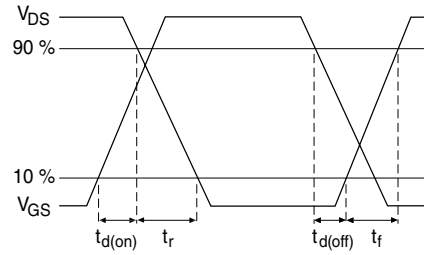


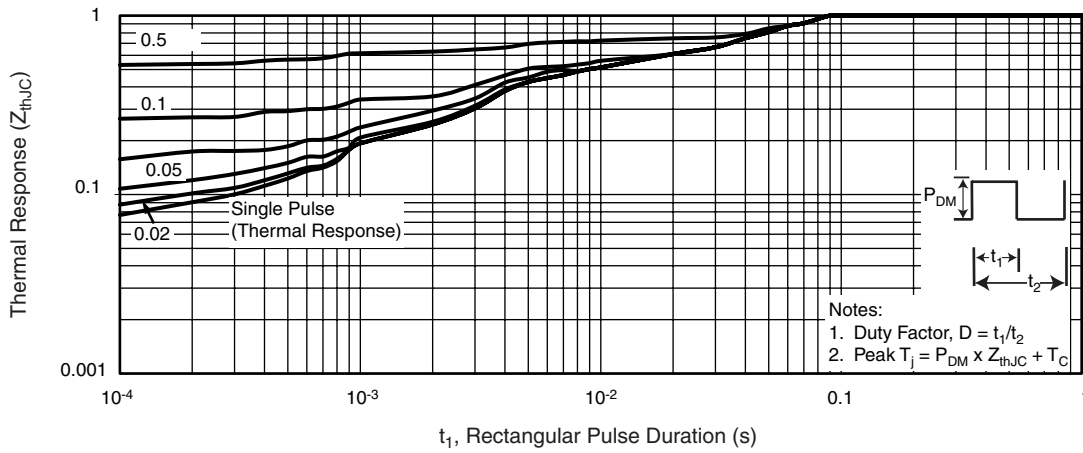
Fig. 9 - Maximum Safe Operating Area (TO-220 FULLPAK)



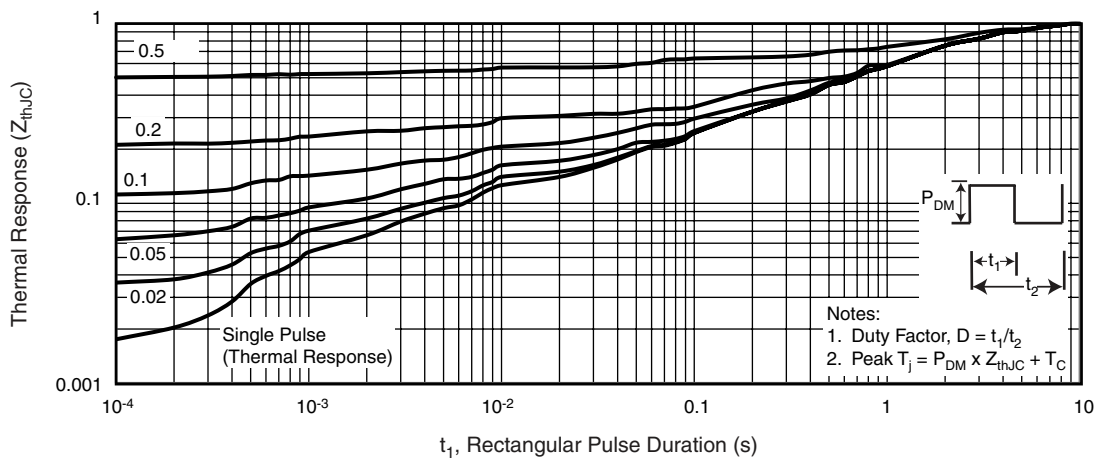
**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D<sup>2</sup>PAK)**



**Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220 FULLPAK)**

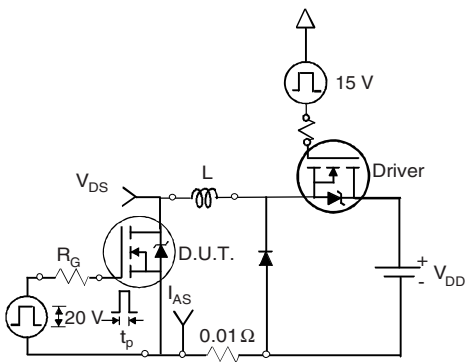


Fig. 13a - Unclamped Inductive Test Circuit

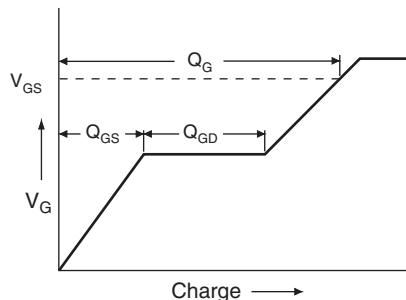


Fig. 14a - Basic Gate Charge Waveform

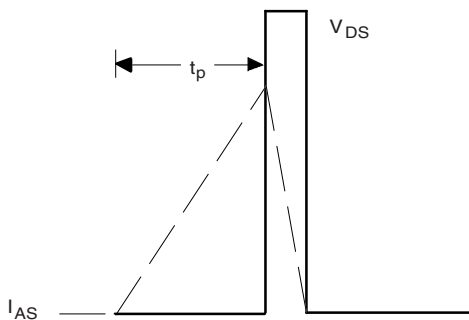


Fig. 13b - Unclamped Inductive Waveforms

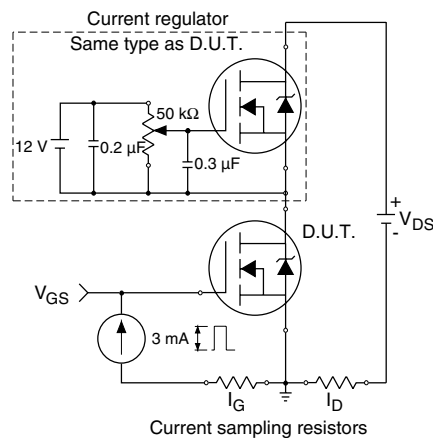
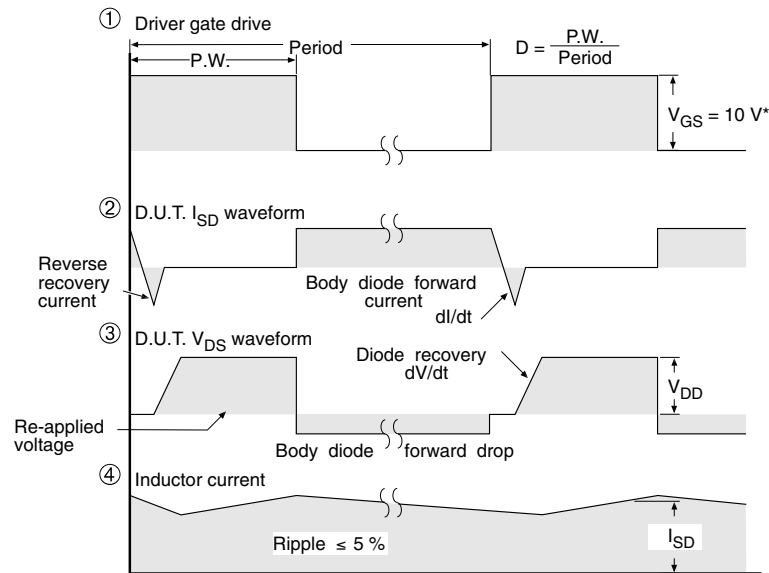
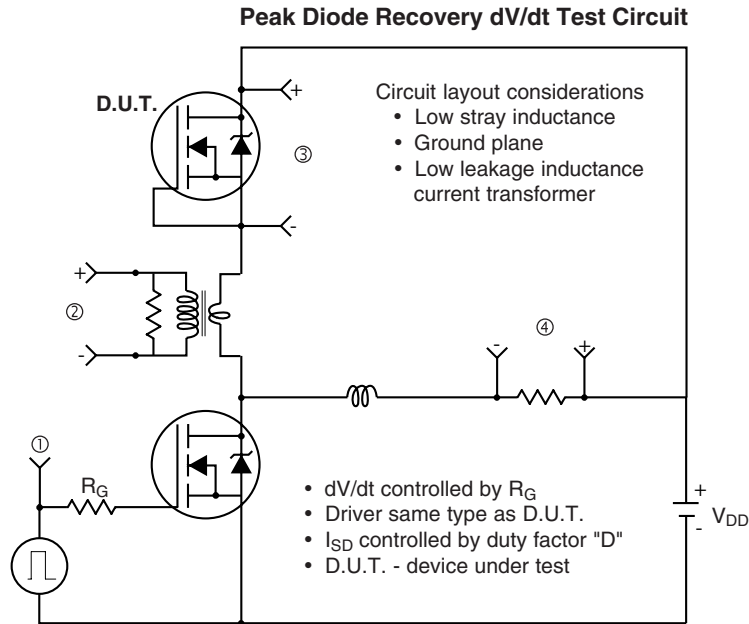


Fig. 14b - Gate Charge Test Circuit

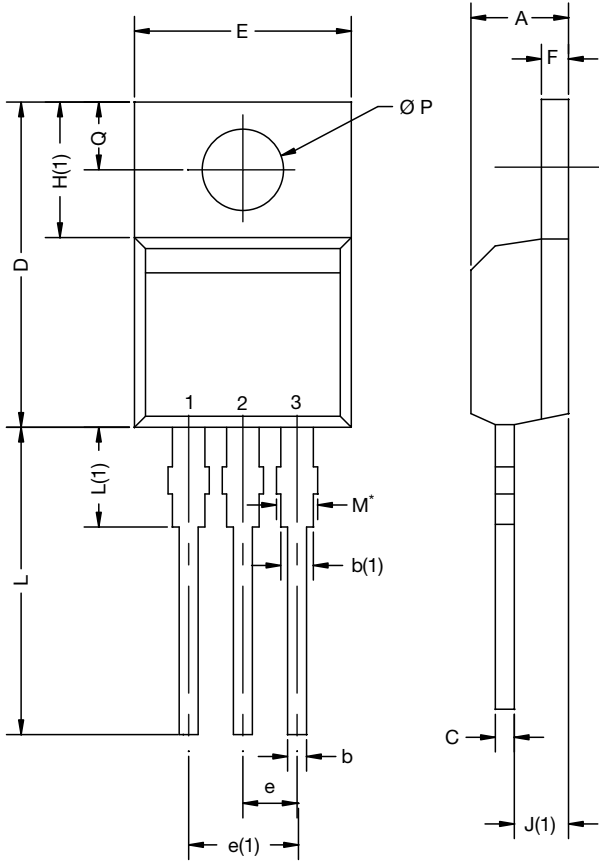


\*  $V_{GS} = 5 V$  for logic level devices

Fig. 15 - For N-Channel

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## TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- M\* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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