THE DATASHEET OF

MB95F316EPMC-G-SNE2

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MB95F314E/F314L/F316E/F316L/F318E/F318L
MB95F374E/F374L/F376E/F376L/F378E/F378L

New 8FX MB95310L/370L Series 8-bit Microcontrollers

MB95310L/370L is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock

- Selectable main clock source
  - Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz)
  - Main PLL clock (up to 16.25 MHz, maximum machine clock frequency: 16.25 MHz)
- Selectable subclock source
  - Sub-OSC clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

Timer

- 8/16-bit composite timer
- 8/16-bit PPG
- 16-bit reload timer
- Event counter
- Time-base timer
- Watch prescaler

UART-SIO

- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer
- Full duplex double buffer

I²C

Built-in wake-up function

External interrupt

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/10-bit A/D converter

8-bit or 10-bit resolution can be selected

LCD controller (LCDC)

- 40 SEG × 4 COM (MB95F314E/F314L/F316E/F316L/F318E/F318L)
- 32 SEG × 4 COM (MB95F374E/F374L/F376E/F376L/F378E/F378L)
- Internal divider resistor
- With blinking function

Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port

- MB95F314E/F314L/F316E/F316L/F318E/F318L (maximum no. of I/O ports: 71)
  General-purpose I/O ports (N-ch open drain): 3
  General-purpose I/O ports (CMOS I/O): 68
- MB95F374E/F374L/F376E/F376L/F378E/F378L (maximum no. of I/O ports: 55)
  General-purpose I/O ports (N-ch open drain): 3
  General-purpose I/O ports (CMOS I/O): 52

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Low-voltage detection reset circuit

- Built-in low-voltage detector
- Three configurable low-voltage detection levels for generating reset
- Five configurable low-voltage detection levels for generating interrupts

Clock supervisor counter

Built-in clock supervisor counter function

Programmable port input voltage level

CMOS input level / hysteresis input level

Dual operation Flash memory

The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

Protects the content of the Flash memory

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1. Product Line-up

■ MB95310L Series

Parameter \ Part number	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	Yes			No		
Reset input	Dedicated					
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 71 • CMOS I/O : 68 • N-ch open drain : 3					
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	2 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	4 channels					
	8-bit or 10-bit resolution can be selected.					

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Part number / Parameter	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
LCD controller (LCDC)	• COM output: 4 (Max) • SEG output: 40 (Max) • LCD drive power supply (bias) pin: 4 (Max) • 40 SEG × 4 COM: 160 pixels can be displayed					
	• Duty LCD mode • Operate in LCD standby mode • Blinking function • Internal divider resistor for LCD drive					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel” • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-80P-M37					

■ MB95370L Series

Part number / Parameter	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	Yes			No		
Reset input	Dedicated					
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max): 55 • CMOS I/O: 52 • N-ch open drain: 3					
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	2 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	4 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					

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Part number / Parameter	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
LCD controller (LCDC)	• COM output: 4 (Max) • SEG output: 32 (Max) • LCD drive power supply (bias) pin: 3 (Max) • 32 SEG × 4 COM: 128 pixels can be displayed					
	• Duty LCD mode • Operate in LCD standby mode • Blinking function • Internal divider resistor for LCD drive					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel“ • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-64P-M38 FPT-64P-M39					

2. Oscillation Stabilization Wait Time

The main CR clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{10} - 2) / F_{CRH}$	Approx. 128 µs (when the main CR clock is 8 MHz)

The main PLL clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{14} - 2) / F_{CH}$	Approx. 14.1 ms (when the main PLL clock is 4 MHz)

3. Packages And Corresponding Products

Part number / Package	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
FPT-80P-M37	O					
FPT-64P-M38	X					
FPT-64P-M39	X					

Part number / Package	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
FPT-80P-M37	X					
FPT-64P-M38	O					
FPT-64P-M39	O					

O: Available

X: Unavailable

4. Differences Among Products And Notes On Product Selection

■ Current consumption
When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “Electrical Characteristics”.

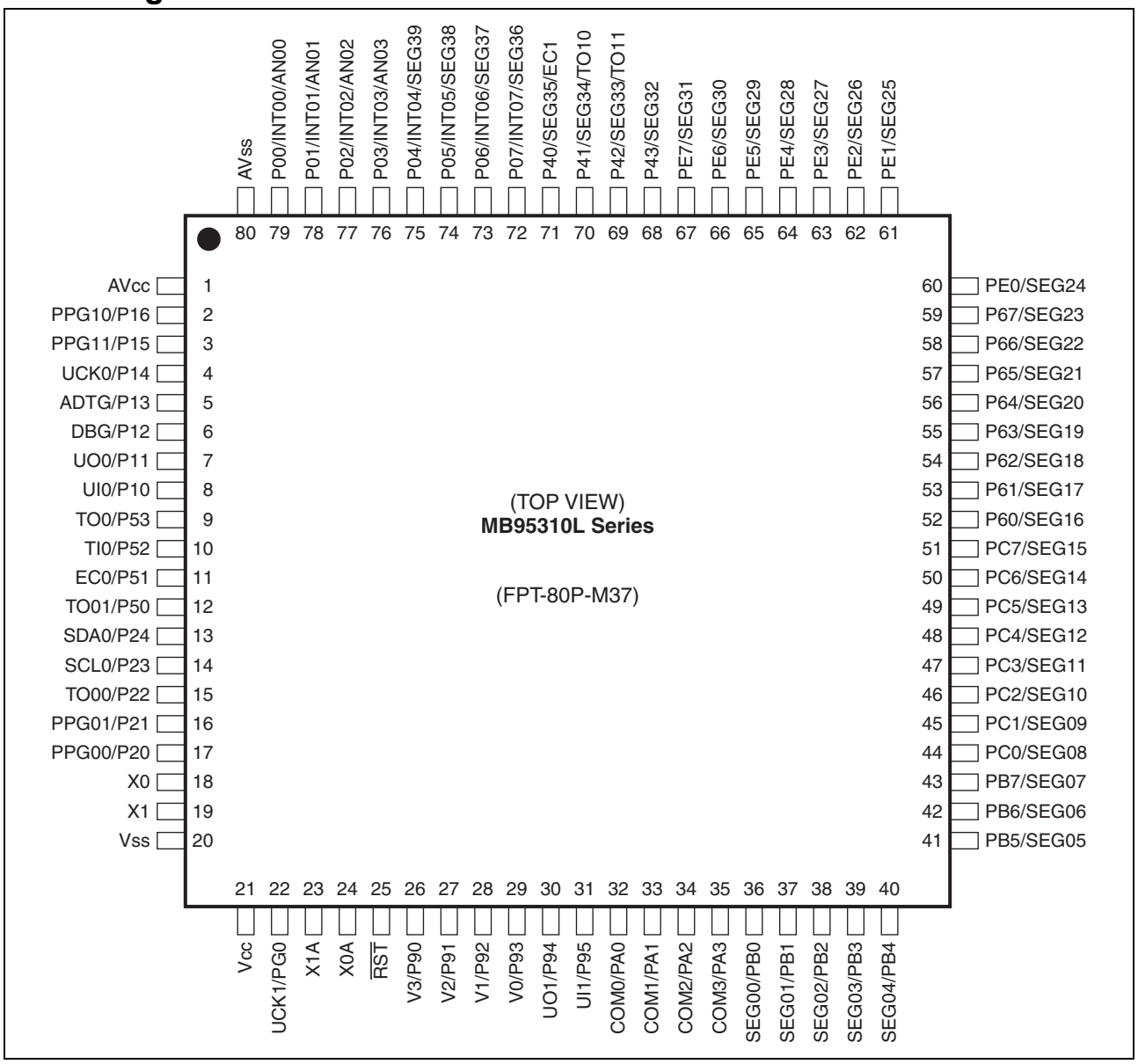
■ Package
For details of information on each package, see “Packages And Corresponding Products” and “Electrical Characteristics”.

■ Operating voltage
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “Electrical Characteristics”.

■ On-chip debug function
The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 31 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95310L/370L Series.

5. Pin Assignment



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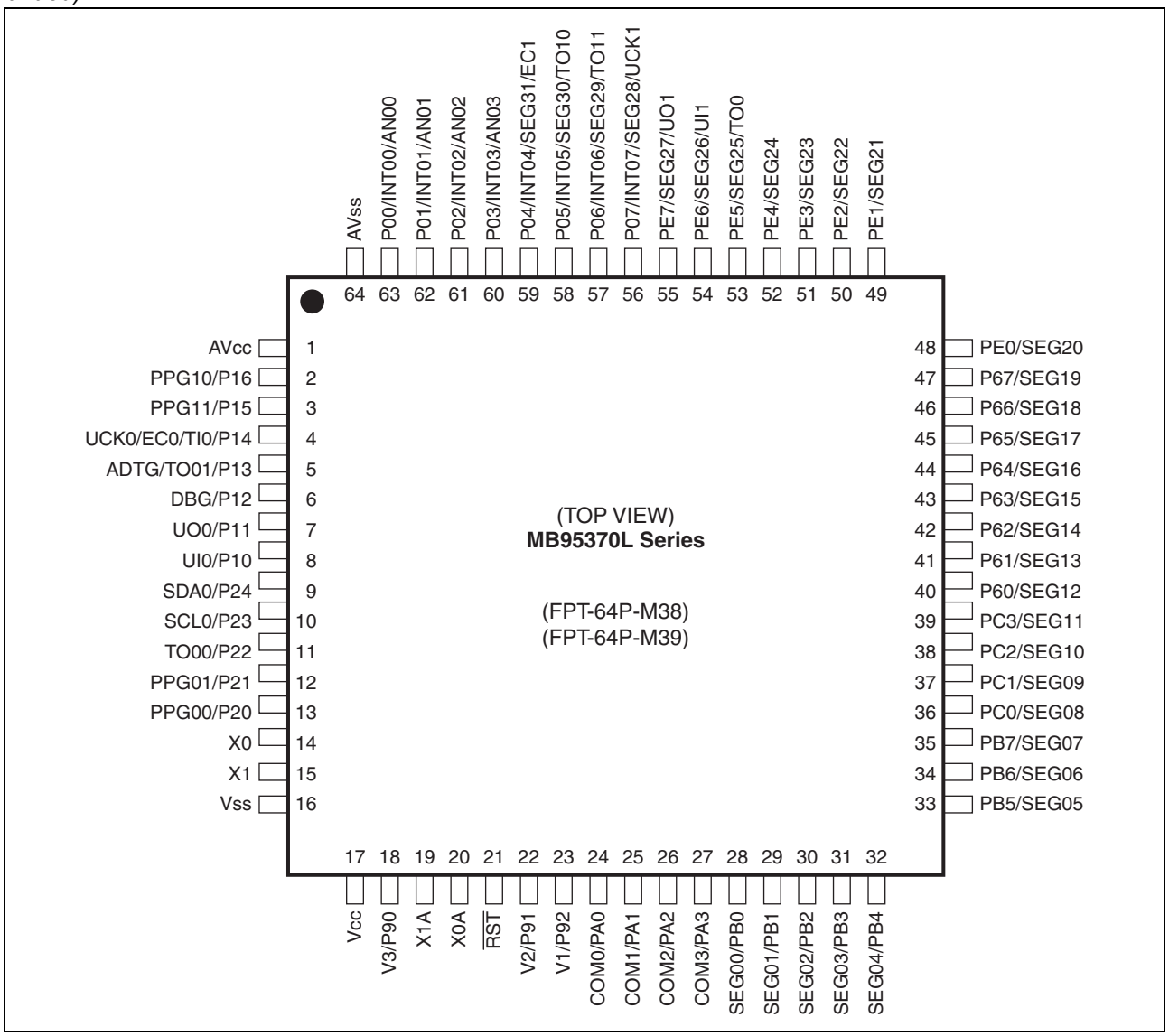
AVss
P00/INT00/AN00
P01/INT01/AN01
P02/INT02/AN02
P03/INT03/AN03
P04/INT04/SEG31/EC1
P05/INT05/SEG30/TO10
P06/INT06/SEG29/TO11
P07/INT07/SEG28/UCK1
PE7/SEG27/UO1
PE6/SEG26/UI1
PE5/SEG25/TO0
PE4/SEG24
PE3/SEG23
PE2/SEG22
PE1/SEG21
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
PPG10/P16 2
PPG11/P15 3
UCK0/EC0/TI0/P14 4
ADTG/TO01/P13 5
DBG/P12 6
UO0/P11 7
UI0/P10 8
SDA0/P24 9
SCL0/P23 10
TO00/P22 11
PPG01/P21 12
PPG00/P20 13
X0 14
X1 15
Vss 16
48 PE0/SEG20
47 P67/SEG19
46 P66/SEG18
45 P65/SEG17
44 P64/SEG16
43 P63/SEG15
42 P62/SEG14
41 P61/SEG13
40 P60/SEG12
39 PC3/SEG11
38 PC2/SEG10
37 PC1/SEG09
36 PC0/SEG08
35 PB7/SEG07
34 PB6/SEG06
33 PB5/SEG05
(TOP VIEW)
MB95370L Series
(FPT-64P-M38)
(FPT-64P-M39)
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Vcc
V3/P90
X1A
X0A
RST
V2/P91
V1/P92
COM0/PA0
COM1/PA1
COM2/PA2
COM3/PA3
SEG00/PB0
SEG01/PB1
SEG02/PB2
SEG03/PB3
SEG04/PB4

6. Pin Description (MB95310L Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P16	H	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
3	P15	H	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
4	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
5	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
6	P12	C	General-purpose I/O port
	DBG		DBG input pin
7	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
8	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
9	P53	H	General-purpose I/O port
	TO0		16-bit reload timer ch. 0 output pin
10	P52	H	General-purpose I/O port
	TI0		16-bit reload timer ch. 0 input pin The pin can also be used as the event counter input pin when the event counter function is used.
11	P51	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
12	P50	H	General-purpose I/O port
	TO01		8/16-bit composite timer ch. 0 output pin
13	P24	I	General-purpose I/O port
	SDA0		I^2C data I/O pin
14	P23	I	General-purpose I/O port
	SCL0		I^2C clock I/O pin
15	P22	H	General-purpose I/O port
	TO00		8/16-bit composite timer ch. 0 output pin
16	P21	H	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
17	P20	H	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
18	X0	A	Main clock oscillation pin
19	X1	A	Main clock oscillation pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
20	V_{SS}	—	Power supply pin (GND)
21	V_{CC}	—	Power supply pin
22	PG0	H	General-purpose I/O port
	UCK1		UART/SIO ch. 1 clock I/O pin
23	X1A	A	Subclock oscillation pin (32 kHz)
24	X0A	A	Subclock oscillation pin (32 kHz)
25	$\overline{RST}$	B	Reset pin
26	P90	R	General-purpose I/O port
	V3		LCDC drive power supply pin
27	P91	R	General-purpose I/O port
	V2		LCDC drive power supply pin
28	P92	R	General-purpose I/O port
	V1		LCDC drive power supply pin
29	P93	R	General-purpose I/O port
	V0		LCDC drive power supply pin
30	P94	H	General-purpose I/O port
	UO1		UART/SIO ch. 0 data output pin
31	P95	G	General-purpose I/O port
	UI1		UART/SIO ch. 0 data input pin
32	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
33	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
34	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
35	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
36	PB0	M	General-purpose I/O port
	SEG00		LCDC SEG output pin
37	PB1	M	General-purpose I/O port
	SEG01		LCDC SEG output pin
38	PB2	M	General-purpose I/O port
	SEG02		LCDC SEG output pin
39	PB3	M	General-purpose I/O port
	SEG03		LCDC SEG output pin
40	PB4	M	General-purpose I/O port
	SEG04		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
41	PB5	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
42	PB6	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
43	PB7	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
44	PC0	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
45	PC1	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
46	PC2	M	General-purpose I/O port
	SEG10		LCDC SEG output pin
47	PC3	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
48	PC4	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
49	PC5	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
50	PC6	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
51	PC7	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
52	P60	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
53	P61	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
54	P62	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
55	P63	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
56	P64	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
57	P65	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
58	P66	M	General-purpose I/O port
	SEG22		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
59	P67	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
60	PE0	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
61	PE1	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
62	PE2	M	General-purpose I/O port
	SEG26		LCDC SEG output pin
63	PE3	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
64	PE4	M	General-purpose I/O port
	SEG28		LCDC SEG output pin
65	PE5	M	General-purpose I/O port
	SEG29		LCDC SEG output pin
66	PE6	N	General-purpose I/O port
	SEG30		LCDC SEG output pin
67	PE7	M	General-purpose I/O port
	SEG31		LCDC SEG output pin
68	P43	M	General-purpose I/O port
	SEG32		LCDC SEG output pin
69	P42	M	General-purpose I/O port
	SEG33		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
70	P41	M	General-purpose I/O port
	SEG34		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
71	P40	M	General-purpose I/O port
	SEG35		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
72	P07	Q	General-purpose I/O port
	INT07		External interrupt input pin
	SEG36		LCDC SEG output pin
73	P06	Q	General-purpose I/O port
	INT06		External interrupt input pin
	SEG37		LCDC SEG output pin

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Pin no.	Pin name	I/O circuit type*	Function
74	P05	Q	General-purpose I/O port
	INT05		External interrupt input pin
	SEG38		LCDC SEG output pin
75	P04	Q	General-purpose I/O port
	INT04		External interrupt input pin
	SEG39		LCDC SEG output pin
76	P03	J	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
77	P02	J	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
78	P01	J	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
79	P00	J	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
80	AV_{ss}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see “I/O Circuit Type”.

7. Pin Description (MB95370L Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P16	H	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
3	P15	H	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
4	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
	EC0		8/16-bit composite timer ch. 0 clock input pin The pin can also be used as the event counter input pin when the event counter function is used.
	TI0		16-bit reload timer ch. 0 input pin
5	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
	TO01		8/16-bit composite timer ch. 0 output pin
6	P12	C	General-purpose I/O port
	DBG		DBG input pin
7	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
8	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
9	P24	I	General-purpose I/O port
	SDA0		I^2C data I/O pin
10	P23	I	General-purpose I/O port
	SCL0		I^2C clock I/O pin
11	P22	H	General-purpose I/O port
	TO00		8/16-bit composite timer ch. 0 output pin
12	P21	H	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
13	P20	H	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
14	X0	A	Main clock oscillation pin
15	X1	A	Main clock oscillation pin
16	V_{SS}	—	Power supply pin (GND)
17	V_{CC}	—	Power supply pin
18	P90	R	General-purpose I/O port
	V3		LCDC drive power supply pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
19	X1A	A	Subclock oscillation pin (32 kHz)
20	X0A		Subclock oscillation pin (32 kHz)
21	$\overline{RST}$	B	Reset pin
22	P91	R	General-purpose I/O port
	V2		LCDC drive power supply pin
23	P92	R	General-purpose I/O port
	V1		LCDC drive power supply pin
24	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
25	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
26	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
27	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
28	PB0	M	General-purpose I/O port
	SEG00		LCDC SEG output pin
29	PB1	M	General-purpose I/O port
	SEG01		LCDC SEG output pin
30	PB2	M	General-purpose I/O port
	SEG02		LCDC SEG output pin
31	PB3	M	General-purpose I/O port
	SEG03		LCDC SEG output pin
32	PB4	M	General-purpose I/O port
	SEG04		LCDC SEG output pin
33	PB5	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
34	PB6	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
35	PB7	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
36	PC0	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
37	PC1	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
38	PC2	M	General-purpose I/O port
	SEG10		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
39	PC3	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
40	P60	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
41	P61	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
42	P62	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
43	P63	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
44	P64	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
45	P65	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
46	P66	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
47	P67	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
48	PE0	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
49	PE1	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
50	PE2	M	General-purpose I/O port
	SEG22		LCDC SEG output pin
51	PE3	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
52	PE4	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
53	PE5	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
	TO0		16-bit reload timer ch. 0 output pin
54	PE6	N	General-purpose I/O port
	SEG26		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
55	PE7	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin

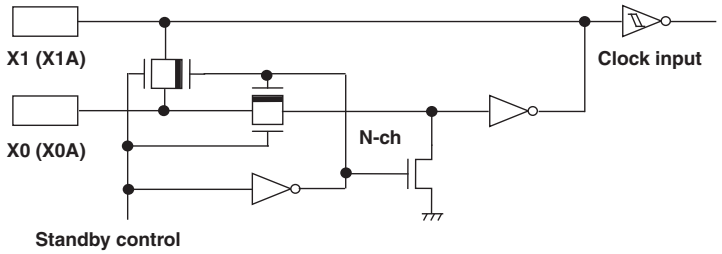
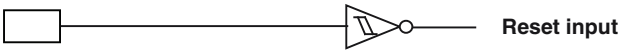
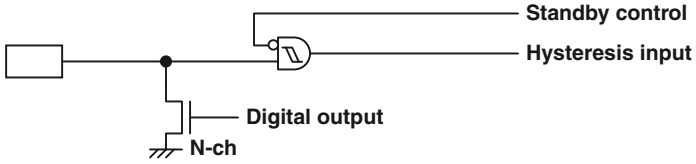
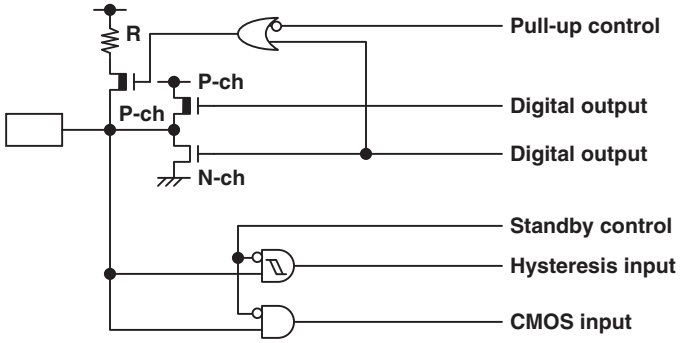
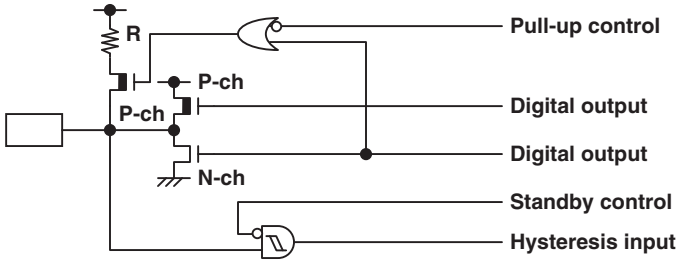
(Continued)

(Continued)

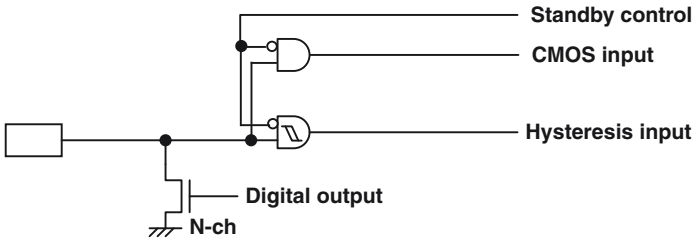
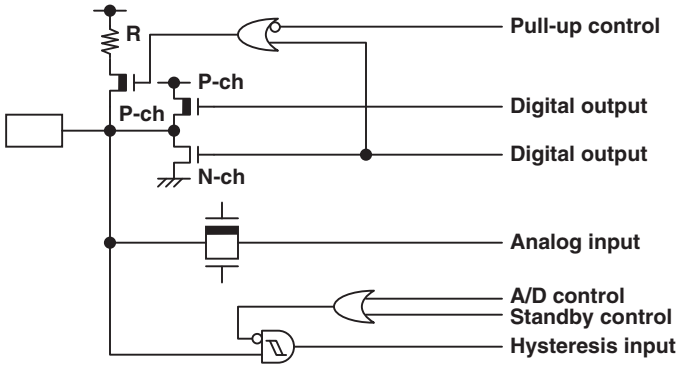
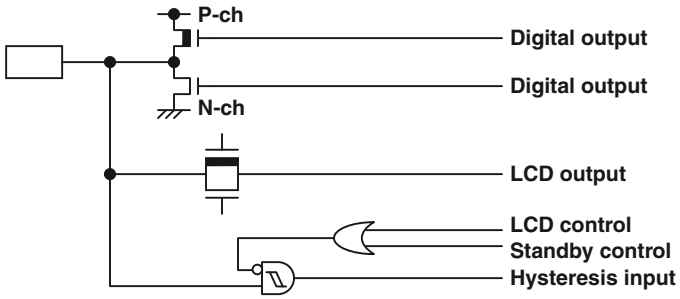
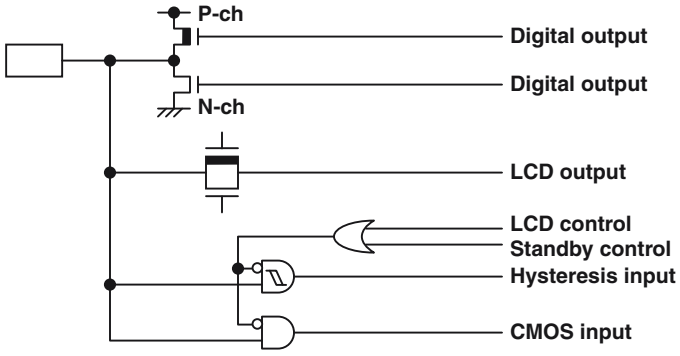
Pin no.	Pin name	I/O circuit type*	Function
56	P07	Q	General-purpose I/O port
	INT07		External interrupt input pin
	SEG28		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
57	P06	Q	General-purpose I/O port
	INT06		External interrupt input pin
	SEG29		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
58	P05	Q	General-purpose I/O port
	INT05		External interrupt input pin
	SEG30		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
59	P04	Q	General-purpose I/O port
	INT04		External interrupt input pin
	SEG31		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
60	P03	J	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
61	P02	J	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
62	P01	J	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
63	P00	J	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
64	AV_{ss}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see “I/O Circuit Type”.

8. I/O Circuit Type

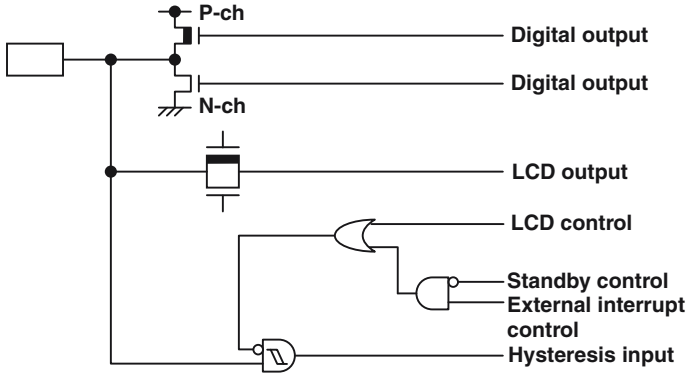
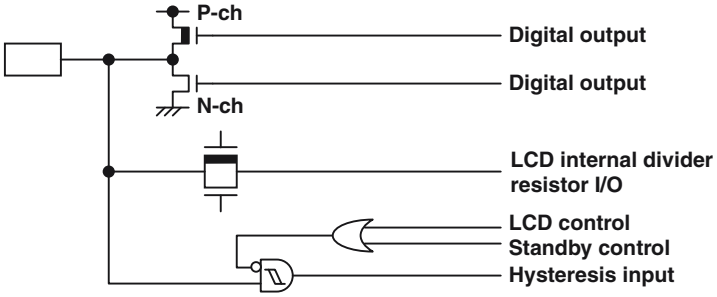
Type	Circuit	Remarks
A		■ Oscillation circuit ■ High-speed side Feedback resistance: approx. 1 MΩ ■ Low-speed side Feedback resistance: approx: 24 MΩ Dumping resistance: approx: 144 kΩ
B		Reset input
C		■ N-ch open drain output ■ Hysteresis input
G		■ CMOS output ■ Hysteresis input ■ CMOS input ■ Pull-up control available
H		■ CMOS output ■ Hysteresis input ■ Pull-up control available

(Continued)

Type	Circuit	Remarks
I		■ N-ch open drain output ■ CMOS input ■ Hysteresis input
J		■ CMOS output ■ Hysteresis input ■ Analog input ■ Pull-up control available
M		■ CMOS output ■ LCD output ■ Hysteresis input
N		■ CMOS output ■ LCD output ■ Hysteresis input ■ CMOS input

(Continued)

(Continued)

Type	Circuit	Remarks
Q		■ CMOS output ■ LCD output ■ Hysteresis input
R		■ CMOS output ■ LCD power supply ■ Hysteresis input

9. Notes On Device Handling

■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “18.1 Absolute Maximum Ratings” of “Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

10. Pin Connection

■ Treatment of unused input pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

■ Notes on handling the external clock pins while using the CR clock

Connect the X0 pin and the X0A pin to the V_{SS} pin and leave the X1 pin and the X1A pin unconnected.

■ Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

■ DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

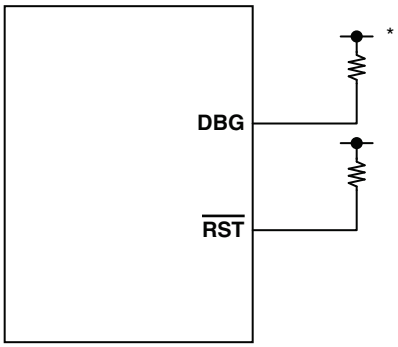
The DBG pin should not stay at “L” level after power-on until the reset output is released.

■ $\overline{RST}$ pin

Connect the $\overline{RST}$ pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{RST}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

- DBG/$\overline{\text{RST}}$ pins connection diagram

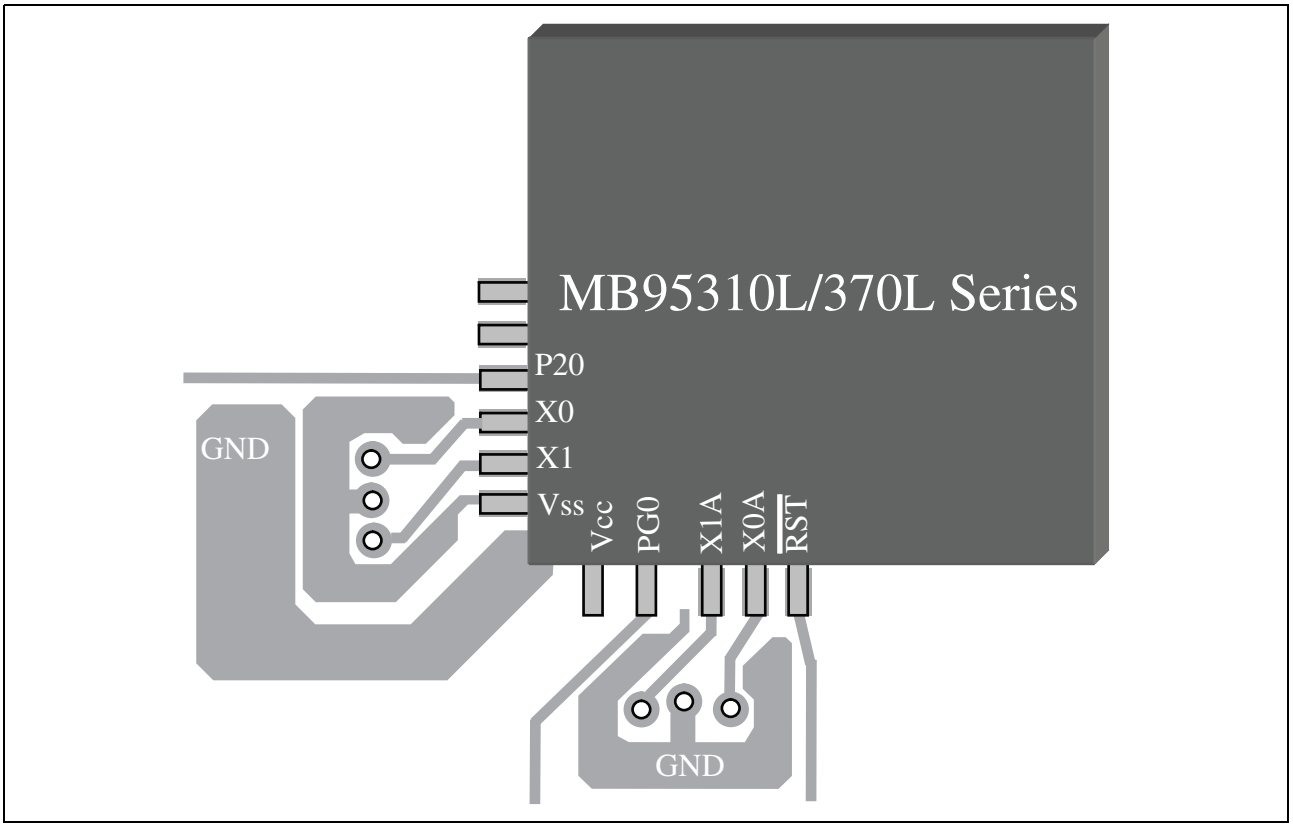


*: Since the DBG input pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

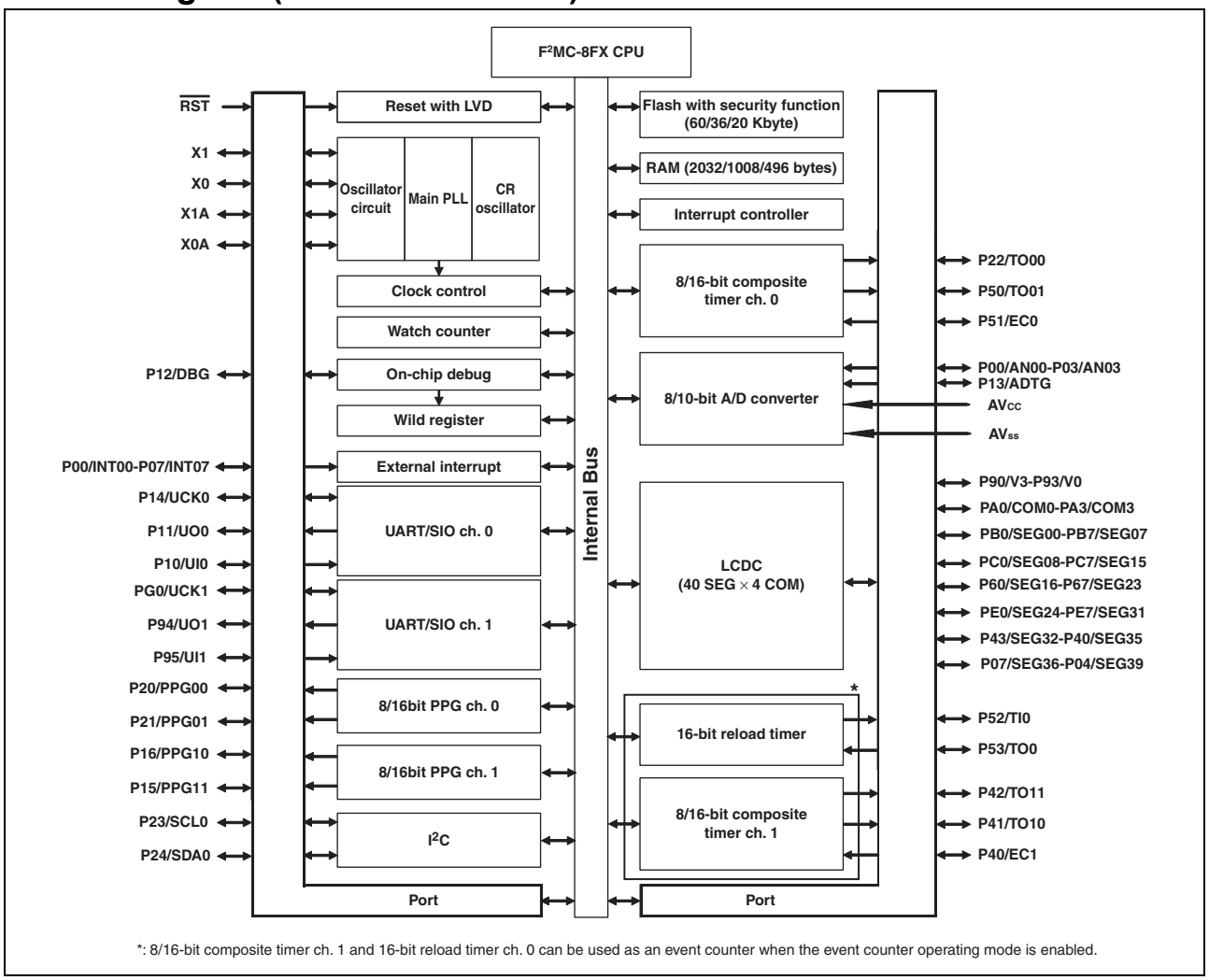
11. Recommended Layout

■ GND wire should be placed around X0, X1, X0A and X1A

The recommended layout method illustrated in following diagram aims to avoid noise coupled between the oscillator pins and GPIO, which may cause the main oscillator or the sub oscillator to malfunction.

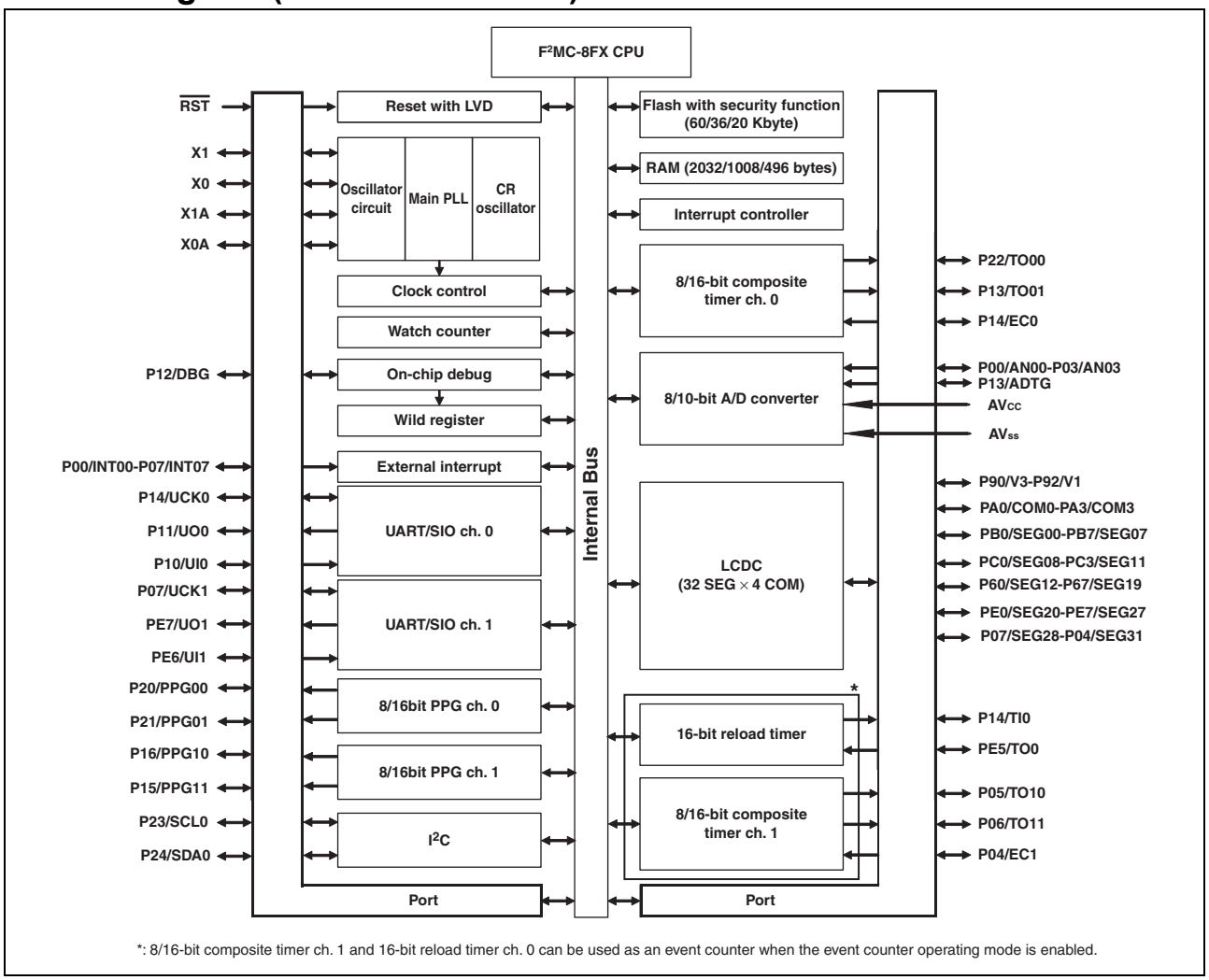


12. Block Diagram (MB95310L Series)



*: 8/16-bit composite timer ch. 1 and 16-bit reload timer ch. 0 can be used as an event counter when the event counter operating mode is enabled.

13. Block Diagram (MB95370L Series)



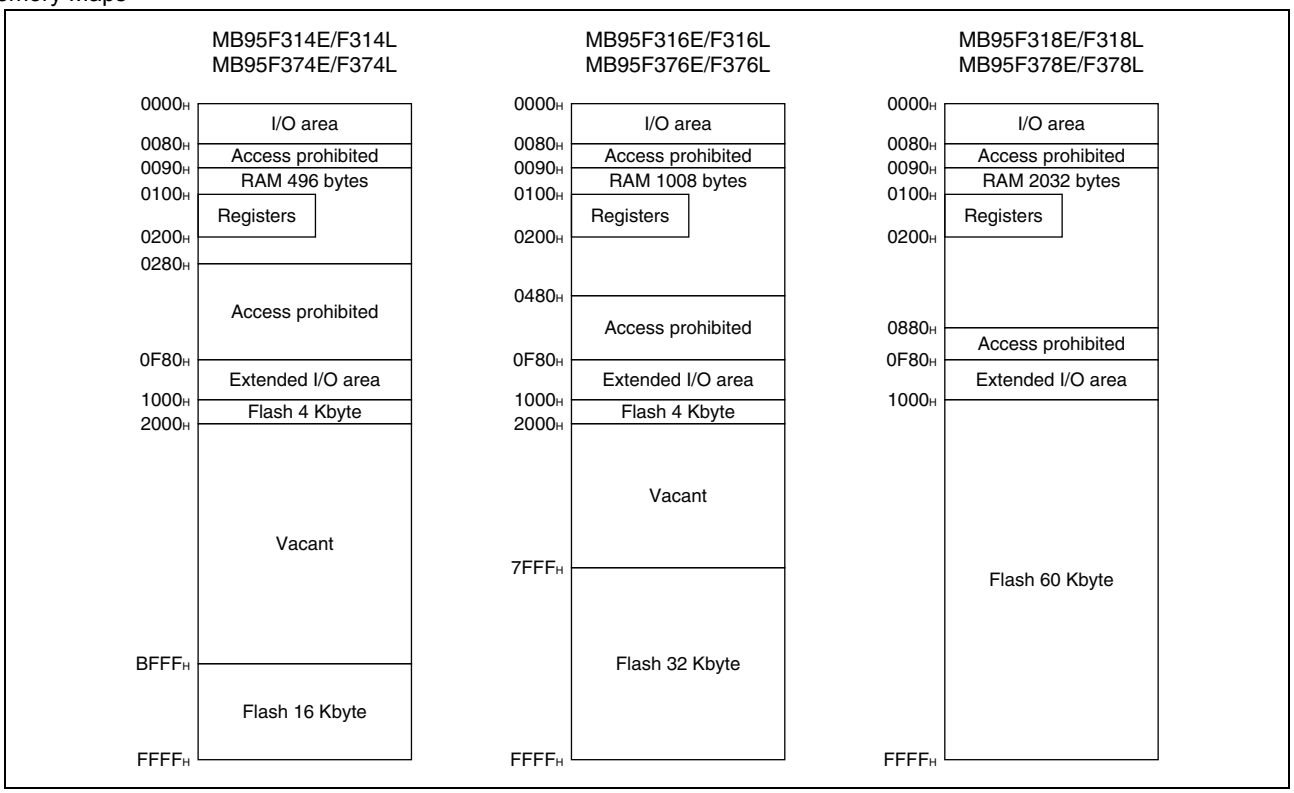
*: 8/16-bit composite timer ch. 1 and 16-bit reload timer ch. 0 can be used as an event counter when the event counter operating mode is enabled.

14. CPU Core

■ Memory Space

The memory space of the MB95310L/370L Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95310L/370L Series are shown below.

■ Memory Maps


MB95F314E/F314L
MB95F374E/F374L
0000H
I/O area
0080H
Access prohibited
0090H
RAM 496 bytes
0100H
Registers
0200H
0280H
Access prohibited
0F80H
Extended I/O area
1000H
Flash 4 Kbyte
2000H
Vacant
BFFFH
Flash 16 Kbyte
FFFFH
MB95F316E/F316L
MB95F376E/F376L
0000H
I/O area
0080H
Access prohibited
0090H
RAM 1008 bytes
0100H
Registers
0200H
0480H
Access prohibited
0F80H
Extended I/O area
1000H
Flash 4 Kbyte
2000H
Vacant
7FFFH
Flash 32 Kbyte
FFFFH
MB95F318E/F318L
MB95F378E/F378L
0000H
I/O area
0080H
Access prohibited
0090H
RAM 2032 bytes
0100H
Registers
0200H
0880H
Access prohibited
0F80H
Extended I/O area
1000H
Flash 60 Kbyte
FFFFH

15. I/O Map (MB95310L Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$XXXXXX11_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$	PDR2	Port 2 data register	R/W	00000000_B
$000F_H$	DDR2	Port 2 direction register	R/W	00000000_B
0010_H, 0011_H	—	(Disabled)	—	—
0012_H	PDR4	Port 4 data register	R/W	00000000_B
0013_H	DDR4	Port 4 direction register	R/W	00000000_B
0014_H	PDR5	Port 5 data register	R/W	00000000_B
0015_H	DDR5	Port 5 direction register	R/W	00000000_B
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to $001B_H$	—	(Disabled)	—	—
$001C_H$	PDR9	Port 9 data register	R/W	00000000_B
$001D_H$	DDR9	Port 9 direction register	R/W	00000000_B
$001E_H$	PDRA	Port A data register	R/W	00000000_B
$001F_H$	DDRA	Port A direction register	R/W	00000000_B
0020_H	PDRB	Port B data register	R/W	00000000_B
0021_H	DDRB	Port B direction register	R/W	00000000_B
0022_H	PDRC	Port C data register	R/W	00000000_B
0023_H	DDRC	Port C direction register	R/W	00000000_B
0024_H, 0025_H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0026_H	PDRE	Port E data register	R/W	00000000_B
0027_H	DDRE	Port E direction register	R/W	00000000_B
0028_H, 0029_H	—	(Disabled)	—	—
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$	PUL2	Port 2 pull-up register	R/W	00000000_B
$002F_H$, 0030_H	—	(Disabled)	—	—
0031_H	PUL5	Port 5 pull-up register	R/W	00000000_B
0032_H, 0033_H	—	(Disabled)	—	—
0034_H	PUL9	Port 9 pull-up register	R/W	00000000_B
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG01 control register ch. 0	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG00 control register ch. 0	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG11 control register ch. 1	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG10 control register ch. 1	R/W	00000000_B
$003E_H$	TMCSRH	16-bit reload timer control status register upper ch. 0	R/W	00000000_B
$003F_H$	TMCSRL	16-bit reload timer control status register lower ch. 0	R/W	00000000_B
0040_H to 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$, $004D_H$	—	(Disabled)	—	—
$004E_H$	LVDR	LVD reset voltage selection ID register	R/W	00000000_B
$004F_H$	LVDC	LVD control register	R/W	$X000000X_B$
0050_H to 0055_H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0056_H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status register ch. 0	R/W	00000001_B
0059_H	TDR0	UART/SIO output data register ch. 0	R/W	00000000_B
$005A_H$	RDR0	UART/SIO input data register ch. 0	R	00000000_B
$005B_H$	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	00000000_B
$005C_H$	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	00100000_B
$005D_H$	SSR1	UART/SIO serial status register ch. 1	R/W	00000001_B
$005E_H$	TDR1	UART/SIO output data register ch. 1	R/W	00000000_B
$005F_H$	RDR1	UART/SIO input data register ch. 1	R	00000000_B
0060_H	IBCR00	I^2C bus control register 0	R/W	00000001_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBCR0	I^2C bus status register	R	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	WCSR	Watch counter status register	R/W	00000000_B
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$	PPS01	8/16-bit PPG01 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9D_H$	PPS00	8/16-bit PPG00 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9E_H$	PDS01	8/16-bit PPG01 duty setting buffer register ch. 0	R/W	11111111_B
$0F9F_H$	PDS00	8/16-bit PPG00 duty setting buffer register ch. 0	R/W	11111111_B
$0FA0_H$	PPS11	8/16-bit PPG11 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA1_H$	PPS10	8/16-bit PPG10 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA2_H$	PDS11	8/16-bit PPG11 duty setting buffer register ch. 1	R/W	11111111_B
$0FA3_H$	PDS10	8/16-bit PPG10 duty setting buffer register ch. 1	R/W	11111111_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FA4_H$	PPGS	8/16-bit PPG start register	R/W	00000000_B
$0FA5_H$	REVC	8/16-bit PPG output inversion register	R/W	00000000_B
$0FA6_H$	TMRH0	16-bit reload timer timer register upper	R/W	00000000_B
	TMRLRH0	16-bit reload timer reload register upper	R/W	00000000_B
$0FA7_H$	TMRL0	16-bit reload timer timer register lower	R/W	00000000_B
	TMRLRL0	16-bit reload timer reload register lower	R/W	00000000_B
$0FA8_H$ to $0FBD_H$	—	(Disabled)	—	—
$0FBE_H$	PSSR0	UART/SIO dedicated baud rate generator prescaler selecting register ch. 0	R/W	00000000_B
$0FBF_H$	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000_B
$0FC0_H$	PSSR1	UART/SIO dedicated baud rate generator prescaler selecting register ch. 1	R/W	00000000_B
$0FC1_H$	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	00000000_B
$0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (lower)	R/W	00000000_B
$0FC4_H$	LCDCC	LCDC control register	R/W	00010000_B
$0FC5_H$	LCDCE1	LCDC enable register 1	R/W	00110000_B
$0FC6_H$	LCDCE2	LCDC enable register 2	R/W	00000000_B
$0FC7_H$	LCDCE3	LCDC enable register 3	R/W	00000000_B
$0FC8_H$	LCDCE4	LCDC enable register 4	R/W	00000000_B
$0FC9_H$	LCDCE5	LCDC enable register 5	R/W	00000000_B
$0FCA_H$	LCDCE6	LCDC enable register 6	R/W	00000000_B
$0FCB_H$	LCDCB1	LCDC blinking setting register 1	R/W	00000000_B
$0FCC_H$	LCDCB2	LCDC blinking setting register 2	R/W	00000000_B
$0FCD_H$ to $0FE0_H$	LCDRAM	LCDC display RAM	R/W	00000000_B
$0FE1_H$	—	(Disabled)	—	—
$0FE2_H$	EVCR	Event counter control register	R/W	00000000_B
$0FE3_H$	WCDR	Watch counter data register	R/W	00111111_B
$0FE4_H$	CRTH	Main CR clock trimming register (upper)	R/W	$0XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (lower)	R/W	$00XXXXXX_B$
$0FE6_H$ to $0FE8_H$	—	(Disabled)	—	—
$0FE9_H$	CMCR	Clock monitoring control register	R/W	$XX000000_B$
$0FEA_H$	CMDR	Clock monitoring data register	R	00000000_B

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FEB_H$	WDTH	Watchdog timer selection ID register (upper)	R	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (lower)	R	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$	WICR	Interrupt pin control register	R/W	01000000_B
$0FF0_H$ to $0FFF_H$	—	(Disabled)	—	—

■ R/W access symbols

R/W : Readable / Writable

R : Read only

■ Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

16. I/O Map (MB95370L Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$XXXXXX11_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$	PDR2	Port 2 data register	R/W	00000000_B
$000F_H$	DDR2	Port 2 direction register	R/W	00000000_B
0010_H to 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to $001B_H$	—	(Disabled)	—	—
$001C_H$	PDR9	Port 9 data register	R/W	00000000_B
$001D_H$	DDR9	Port 9 direction register	R/W	00000000_B
$001E_H$	PDRA	Port A data register	R/W	00000000_B
$001F_H$	DDRA	Port A direction register	R/W	00000000_B
0020_H	PDRB	Port B data register	R/W	00000000_B
0021_H	DDRB	Port B direction register	R/W	00000000_B
0022_H	PDRC	Port C data register	R/W	00000000_B
0023_H	DDRC	Port C direction register	R/W	00000000_B
0024_H, 0025_H	—	(Disabled)	—	—
0026_H	PDRE	Port E data register	R/W	00000000_B
0027_H	DDRE	Port E direction register	R/W	00000000_B
0028_H to $002B_H$	—	(Disabled)	—	—
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$	PUL2	Port 2 pull-up register	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$002F_H$ to 0033_H	—	(Disabled)	—	—
0034_H	PUL9	Port 9 pull-up register	R/W	00000000_B
0035_H	—	(Disabled)	—	—
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG01 control register ch. 0	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG00 control register ch. 0	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG11 control register ch. 1	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG10 control register ch. 1	R/W	00000000_B
$003E_H$	TMCSRH	16-bit reload timer control status register upper ch. 0	R/W	00000000_B
$003F_H$	TMCSRL	16-bit reload timer control status register lower ch. 0	R/W	00000000_B
0040_H to 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$, $004D_H$	—	(Disabled)	—	—
$004E_H$	LVDR	LVD reset voltage selection ID register	R/W	00000000_B
$004F_H$	LVDC	LVD control register	R/W	$X000000X_B$
0050_H to 0055_H	—	(Disabled)	—	—
0056_H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status register ch. 0	R/W	00000001_B
0059_H	TDR0	UART/SIO output data register ch. 0	R/W	00000000_B
$005A_H$	RDR0	UART/SIO input data register ch. 0	R	00000000_B
$005B_H$	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	00000000_B
$005C_H$	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	00100000_B
$005D_H$	SSR1	UART/SIO serial status register ch. 1	R/W	00000001_B
$005E_H$	TDR1	UART/SIO output data register ch. 1	R/W	00000000_B
$005F_H$	RDR1	UART/SIO input data register ch. 1	R	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0060_H	IBCR00	I^2C bus control register 0	R/W	00000001_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBCR0	I^2C bus status register	R	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	WCSR	Watch counter status register	R/W	00000000_B
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$	PPS01	8/16-bit PPG01 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9D_H$	PPS00	8/16-bit PPG00 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9E_H$	PDS01	8/16-bit PPG01 duty setting buffer register ch. 0	R/W	11111111_B
$0F9F_H$	PDS00	8/16-bit PPG00 duty setting buffer register ch. 0	R/W	11111111_B
$0FA0_H$	PPS11	8/16-bit PPG11 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA1_H$	PPS10	8/16-bit PPG10 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA2_H$	PDS11	8/16-bit PPG11 duty setting buffer register ch. 1	R/W	11111111_B
$0FA3_H$	PDS10	8/16-bit PPG10 duty setting buffer register ch. 1	R/W	11111111_B
$0FA4_H$	PPGS	8/16-bit PPG start register	R/W	00000000_B
$0FA5_H$	REVC	8/16-bit PPG output inversion register	R/W	00000000_B
$0FA6_H$	TMRH0	16-bit reload timer timer register upper	R/W	00000000_B
	TMRLRH0	16-bit reload timer reload register upper	R/W	00000000_B
$0FA7_H$	TMRL0	16-bit reload timer timer register lower	R/W	00000000_B
	TMRLRL0	16-bit reload timer reload register lower	R/W	00000000_B
$0FA8_H$ to $0FBD_H$	—	(Disabled)	—	—
$0FBE_H$	PSSR0	UART/SIO dedicated baud rate generator prescaler selecting register ch. 0	R/W	00000000_B
$0FBF_H$	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000_B
$0FC0_H$	PSSR1	UART/SIO dedicated baud rate generator prescaler selecting register ch. 1	R/W	00000000_B
$0FC1_H$	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	00000000_B
$0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (lower)	R/W	00000000_B
$0FC4_H$	LCDCC	LCDC control register	R/W	00010000_B

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(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FC5_H$	LCDCE1	LCDC enable register 1	R/W	00110000_B
$0FC6_H$	LCDCE2	LCDC enable register 2	R/W	00000000_B
$0FC7_H$	LCDCE3	LCDC enable register 3	R/W	00000000_B
$0FC8_H$	LCDCE4	LCDC enable register 4	R/W	00000000_B
$0FC9_H$	LCDCE5	LCDC enable register 5	R/W	00000000_B
$0FCA_H$	—	(Disabled)	—	—
$0FCB_H$	LCDCB1	LCDC blinking setting register 1	R/W	00000000_B
$0FCC_H$	LCDCB2	LCDC blinking setting register 2	R/W	00000000_B
$0FCD_H$ to $0FDC_H$	LCDRAM	LCDC display RAM	R/W	00000000_B
$0FDD_H$ to $0FE1_H$	—	(Disabled)	—	—
$0FE2_H$	EVCR	Event counter control register	R/W	00000000_B
$0FE3_H$	WCDR	Watch counter data register	R/W	00111111_B
$0FE4_H$	CRTH	Main CR clock trimming register (upper)	R/W	$0XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (lower)	R/W	$00XXXXXX_B$
$0FE6_H$ to $0FE8_H$	—	(Disabled)	—	—
$0FE9_H$	CMCR	Clock monitoring control register	R/W	$XX000000_B$
$0FEA_H$	CMDR	Clock monitoring data register	R	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (upper)	R	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (lower)	R	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$	WICR	Interrupt pin control register	R/W	01000000_B
$0FF0_H$ to $0FFF_H$	—	(Disabled)	—	—

■ R/W access symbols

R/W : Readable / Writable

R : Read only

■ Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

17. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 4					
External interrupt ch. 1	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 5					
External interrupt ch. 2	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
External interrupt ch. 7					
UART/SIO ch. 0	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
Low-voltage detection reset circuit					
8/16-bit composite timer ch. 0 (lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
—	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
—	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
UART/SIO ch. 1					
8/16-bit PPG ch. 1 (upper)	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
16-bit reload timer ch. 0	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
I^2C	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
Watch counter					
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}, AV_{CC}	V_{SS} − 0.3	V_{SS} + 4.0	V	*2
Power supply voltage for LCD	V0 to V3	V_{SS} − 0.3	V_{SS} + 4.0	V	Products with LCD internal division resistance*3
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	P23,P24*4
		V_{SS} − 0.3	V_{SS} + 4.0	V	Other than P23,P24*4
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 4.0	V	*4
Maximum clamp current	I_{CLAMP}	−2.0	+2.0	mA	Applicable to specific pins*5
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*5
“L” level maximum output current	I_{OL}	—	15	mA	Applicable to specific pins*5
“L” level average current	I_{OLAV}	—	4	mA	Applicable to specific pins*5 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	-15	mA	Applicable to specific pins*5
“H” level average current	I_{OHAV}	—	-4	mA	Applicable to specific pins*5 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	-100	mA	
“H” level total average output current	ΣI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: Apply equal potential to V_{CC} and AV_{CC}.

*3: V0 to V3 should not exceed V_{CC} + 0.3 V.

*4: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

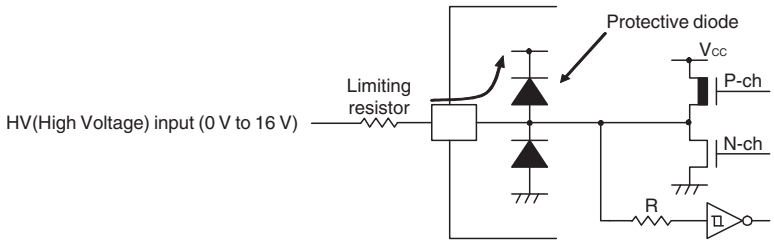
(Continued)

(Continued)

*5: Applicable to the following pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PE0 to PE7, PG0

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistance should be set so that when the HV (High Voltage) signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, and thus affects other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit

  • Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

18.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}, AV_{CC}	1.8*1*2*3	3.6	V	In normal operation, T_A = -10°C to +85°C	Other than on-chip debug mode
		2.0	3.6		In normal operation, T_A = -40°C to +85°C	
		1.5	3.6		Hold condition in stop mode	
		3.10*3	3.6		T_A = +5°C to +35°C	On-chip debug mode
		1.5	3.6		Hold condition in stop mode	
Operating temperature	T_A	–40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is initially 2.03 V when the low-voltage detection reset is used.

*3: The threshold voltage can be set to be 2.03 V, 2.55 V, 3.10 V by software.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

18.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*5	Max		
"H" level input voltage	V_{IHI1}	P10, P95*1, PE6*2	*3	0.7 V_{CC}	—	V_{CC} + 0.3	V	When selecting CMOS input level
	V_{IHI2}	P23, P24	*3	0.7 V_{CC}	—	V_{SS} + 5.5	V	
	V_{IHS1}	P00 to P07, P10 to P16, P20 to P22, P40 to P43*1, P50 to P53*1, P60 to P67, P90 to P92, P93 to P95*1, PA0 to PA3, PB0 to PB7, PC0 to PC3, PC4 to PC7*1, PE0 to PE7, PG0*1	*3	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS2}	P23, P24	*3	0.8 V_{CC}	—	V_{SS} + 5.5	V	
	V_{IHM}	$\overline{RST}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P10, P23, P24, P95*1, PE6*2	*3	V_{SS} – 0.3	—	0.3 V_{CC}	V	When selecting CMOS input level
	V_{ILS}	P00 to P07, P10 to P16, P20 to P24, P40 to P43*1, P50 to P53*1, P60 to P67, P90 to P92, P93 to P95*1, PA0 to PA3, PB0 to PB7, PC0 to PC3, PC4 to PC7*1, PE0 to PE7, PG0*1	*3	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	$\overline{RST}$	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
"H" level output voltage	V_{OH}	Output pin other than P12, P23, P24	I_{OH} = 4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	Output pin other than $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	

(Continued)

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*5	Max		
Input leakage current (Hi-Z output leakage current)	I_{LI}	Ports other than P12, P23, P24	0.0 V<V_I<V_{CC}	−5	—	+5	µA	When pull-up resistance is disabled
Open-drain output leakage voltage	I_{LIOD}	P12, P23, P24	0.0 V<V_I<V_{SS} + 5.5 V	—	—	5	µA	
Pull-up resistance	R_{PULL}	P00 to P03, P10, P11, P13 to P16, P20 to P22, P50 to P53*1, P94, P95*1, PG0*1	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*4	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	16.5	27.7	mA	Except during Flash memory programming and erasing
				—	38.1	44.9	mA	During Flash memory programming and erasing
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	9	15.9	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	22.6	37.9	µA	

(Continued)

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*5	Max		
Power supply current*4	I_{CCLS}	V_{CC} (External clock operation)	F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	11.2	16.5	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	6.7	9	µA	
	I_{CCMPLL}		F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	10.1	19.2	mA	
			F_{CH} = 6.4 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	16.2	30.7	mA	
	I_{CCMCR}		F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	7.9	13.2	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25°C	—	77.8	138.5	µA	
	I_{CTS}		F_{CH} = 32 MHz Time-base timer mode T_A = +25°C	—	4.3	7.4	mA	
	I_{CCH}		Substop mode T_A = +25°C	—	1	5	µA	
	I_A	AV_{CC}	Current consumption for A/D conversion at 16 MHz	—	0.8	1.9	mA	
	I_{AH}		Current consumption for stopping A/D conversion at 16 MHz	—	1	5	µA	

(Continued)

(Continued)

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*5	Max		
Power supply current*4	I_{LVD}	V_{CC}	Current consumption for the low-voltage detection reset circuit	—	6	9.8	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	
LCD internal division resistance	R_{LCD}	—	Between V3 and V_{SS}	—	300	—	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 3.6 V	—	—	5	kΩ	
SEG00 to SEG39 output impedance	R_{VSEG}	SEG00 to SEG39		—	—	7	kΩ	
LCD leakage current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG00 to SEG39	—	−1	—	+1	µA	

*1: It is for MB95310L Series.

*2: It is for MB95370L Series.

*3: The input level can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*4:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “18.4 AC Characteristics: Clock Timing” for F_{CH} and F_{CL}.
- See “18.4 AC Characteristics: 18.4.2 Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

*5: V_{CC} = 3.0 V, T_A = +25°C

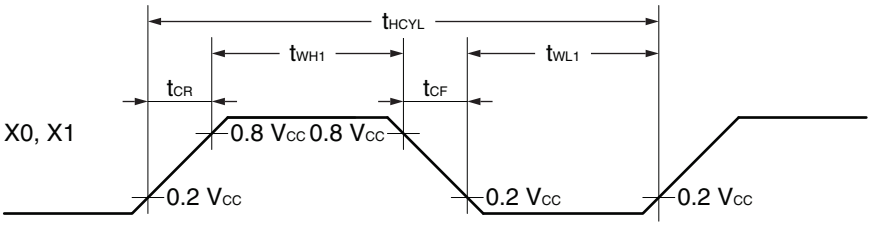
18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

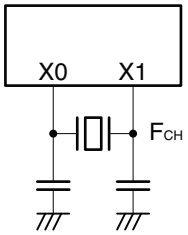
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When the main oscillation circuit is used
				1.00	—	32.50	MHz	When the main external clock is used
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.5	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F_{CRH}	—		12.25	12.5	12.75	MHz	Operating conditions: • The main CR clock is used. • T_A = −10°C to +85°C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
		—		12.1875	12.5	12.8125	MHz	Operating conditions: • The main CR clock is used. • T_A = −40°C to −10°C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—		50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
				30.8	—	1000	ns	When the external clock is used
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	—	61.5	—	—	ns	When using external clock and the duty ratio is about 30% to 70%
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A	X1: open	—	—	5	ns	When the external clock is used
CR oscillation start time	t_{CRHWK}	—	—	—	—	150	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

- Input waveform generated when an external clock (main clock) is used

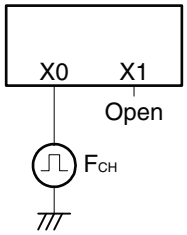


- Figure of main clock input port external connection

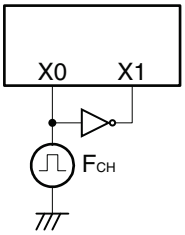
When a crystal oscillator or a ceramic oscillator is used



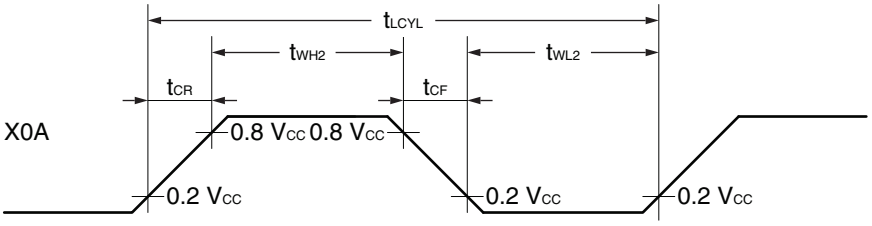
When the external clock is used (X1 is open)



When the external clock is used

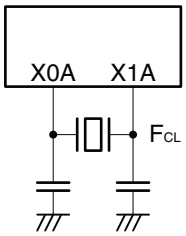


- Input waveform generated when an external clock (subclock) is used

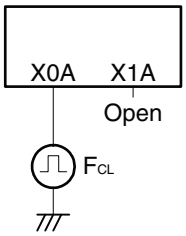


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



18.4.2 Source Clock/Machine Clock

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main oscillation clock is used Min: F_{CH} = 8.125 MHz, multiplied by the PLL multiplier of 2 Max: F_{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 12.5 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.50	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F_{SP} = 12.5 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.393 kHz, no division Max: F_{SPL} = 16.393 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (select from 2, 2.5, 4 multiplication)
- Main CR clock divided by 2
- Subclock divided by 2
- Sub-CR clock divided by 2

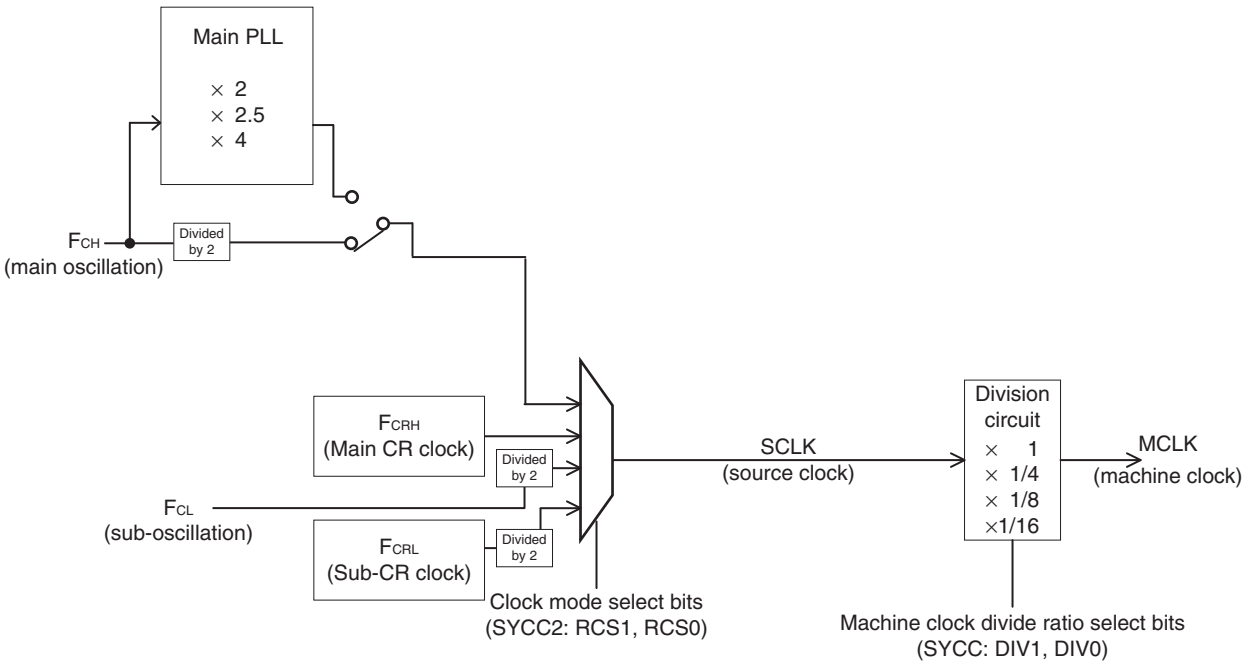
(Continued)

(Continued)

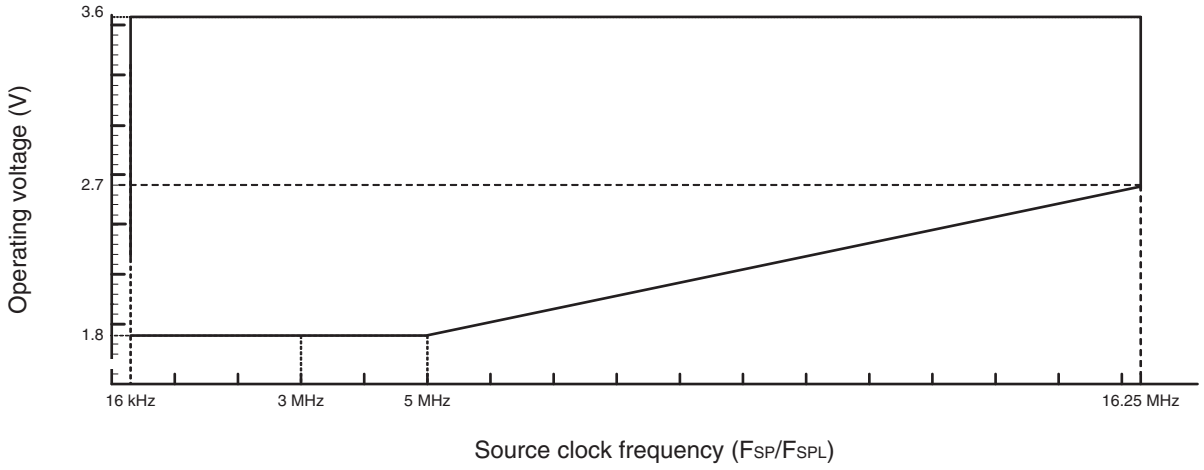
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

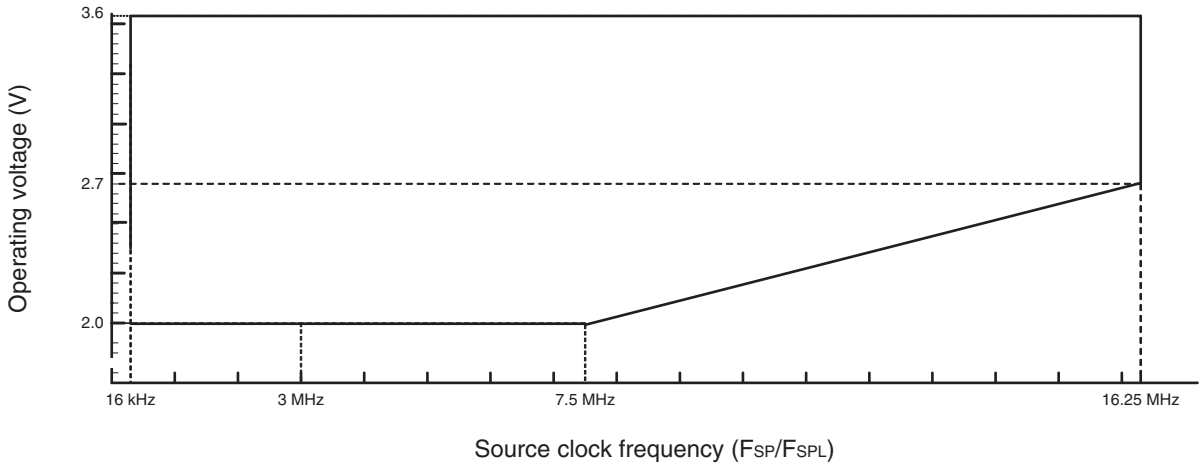
• Schematic diagram of the clock generation block



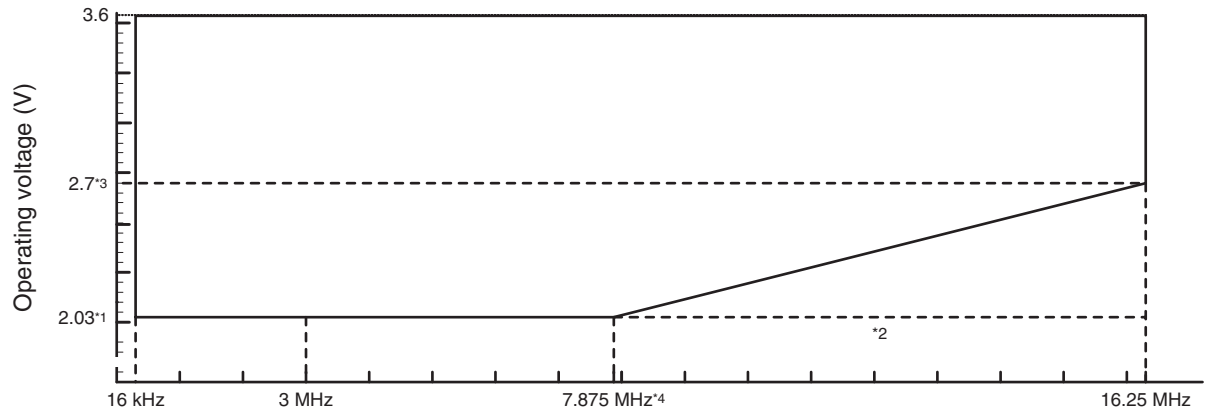
- Operating voltage - Operating frequency (When T_A = −10°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (When T_A = +5°C to +35°C)
  With the on-chip debug function



*1: This is the default LVD reset clear threshold: 1.93 V ± 0.10 V. It can also be set to 2.40 V ± 0.15 V or 2.95 V ± 0.15 V.

*2: If the LVD reset clear threshold is set to 2.95 V ± 0.15 V, the slope from 10 MHz to 16.25 MHz should be a horizontal line.

*3: The operating voltage becomes 3.1 V if the LVD reset clear threshold is set to 2.95 V ± 0.15 V.

*4: The source clock frequency becomes 14.375 MHz if the LVD reset clear threshold is set to 2.40 V ± 0.15 V.

18.4.3 External Reset

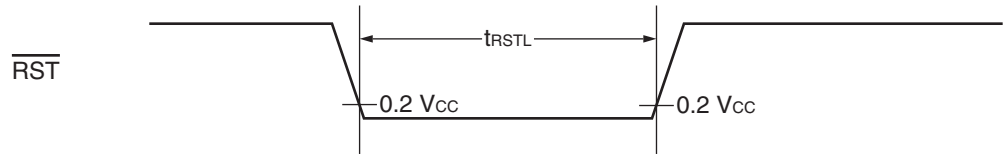
(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

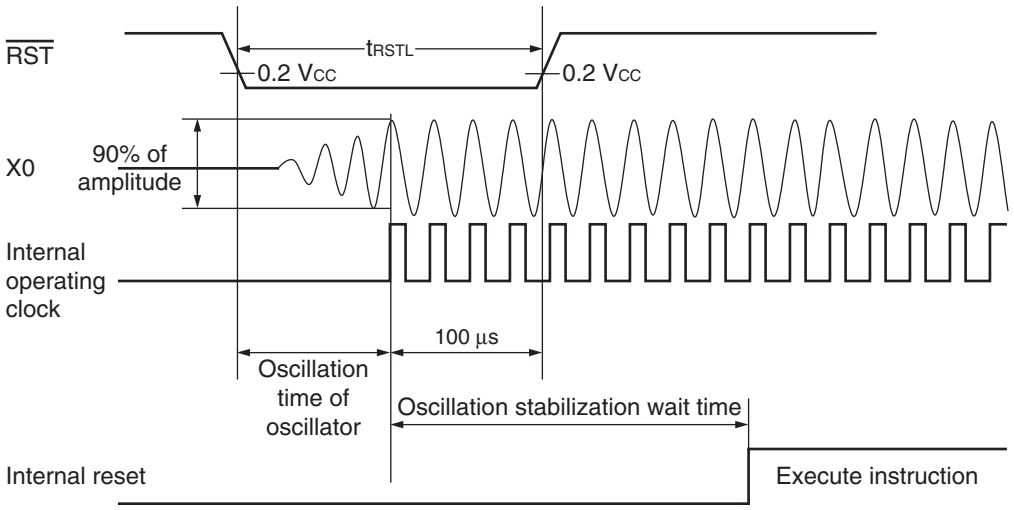
*1: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



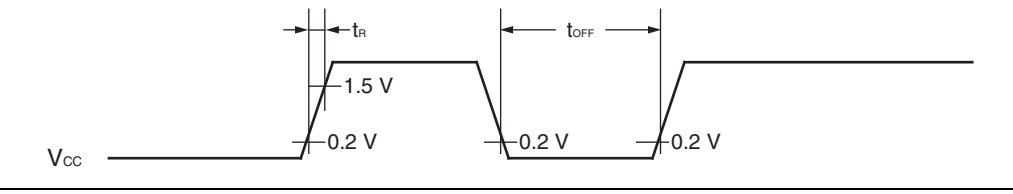
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



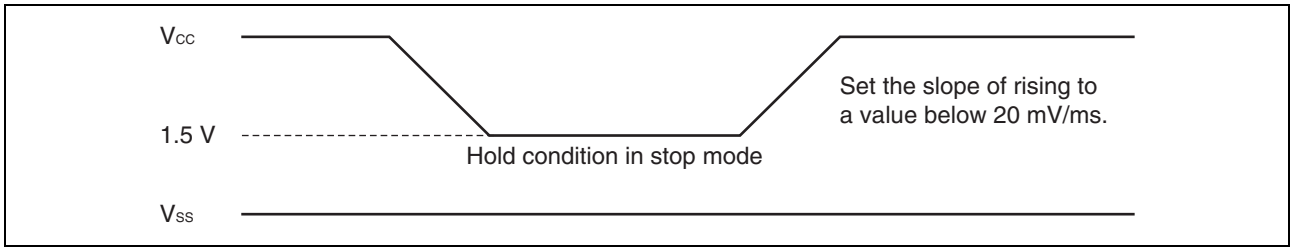
18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 20 mV/ms as shown below.

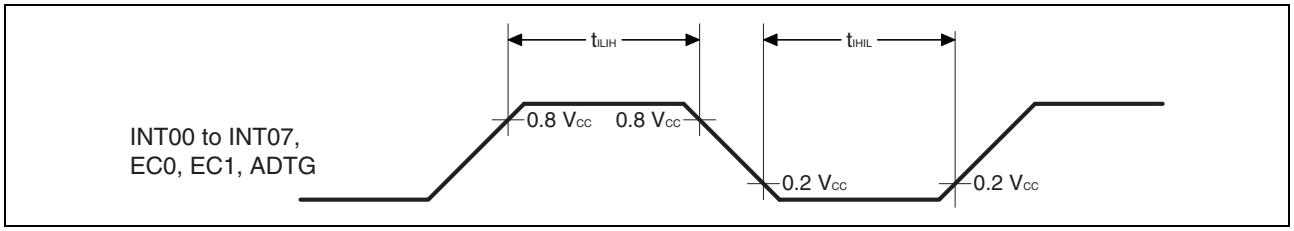


18.4.5 Peripheral Input Timing

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



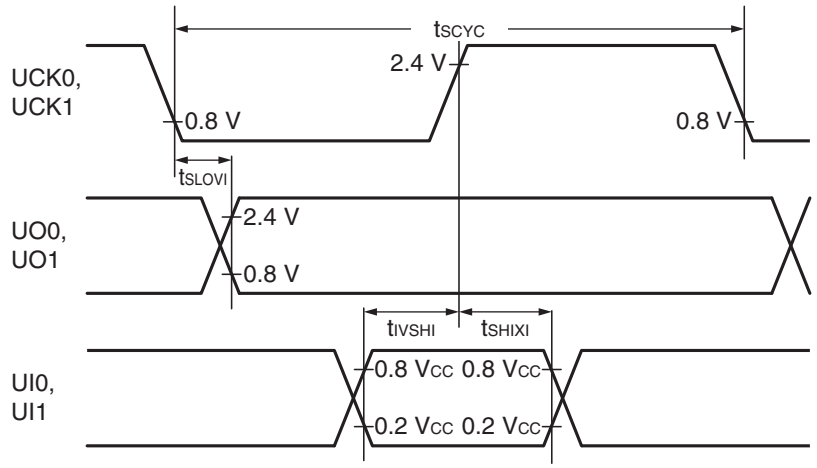
18.4.6 UART/SIO, Serial I/O Timing

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

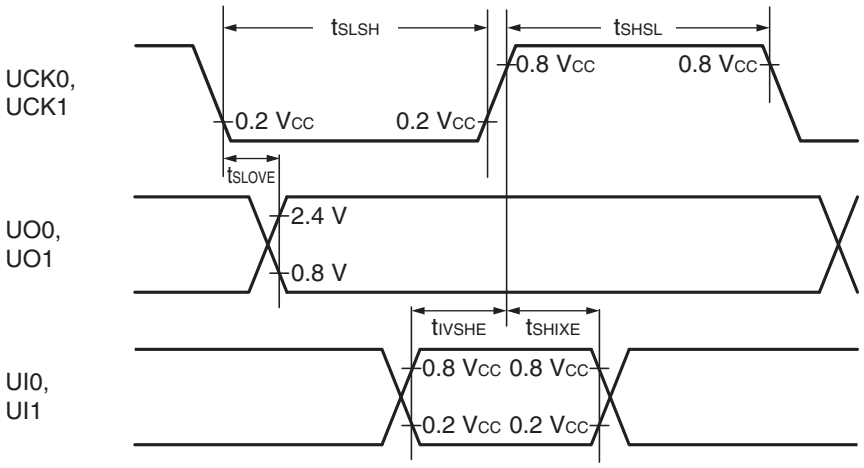
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0, UCK1	Internal clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
UCK ↓→ UO time	t_{SLOVI}	UCK0, UCK1, UO0, UO1		−190	+190	ns
Valid UI → UCK ↑	t_{IVSHI}	UCK0, UCK1, UI0, UI1		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIXI}	UCK0, UCK1, UI0, UI1		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0, UCK1	External clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0, UCK1		4 t_{MCLK}*	—	ns
UCK ↓→ UO time	t_{SLOVE}	UCK0, UCK1, UO0, UO1		—	190	ns
Valid UI → UCK ↑	t_{IVSHE}	UCK0, UCK1, UI0, UI1		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIXE}	UCK0, UCK1, UI0, UI1		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



18.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V, T_A = −40°C to +85°C)

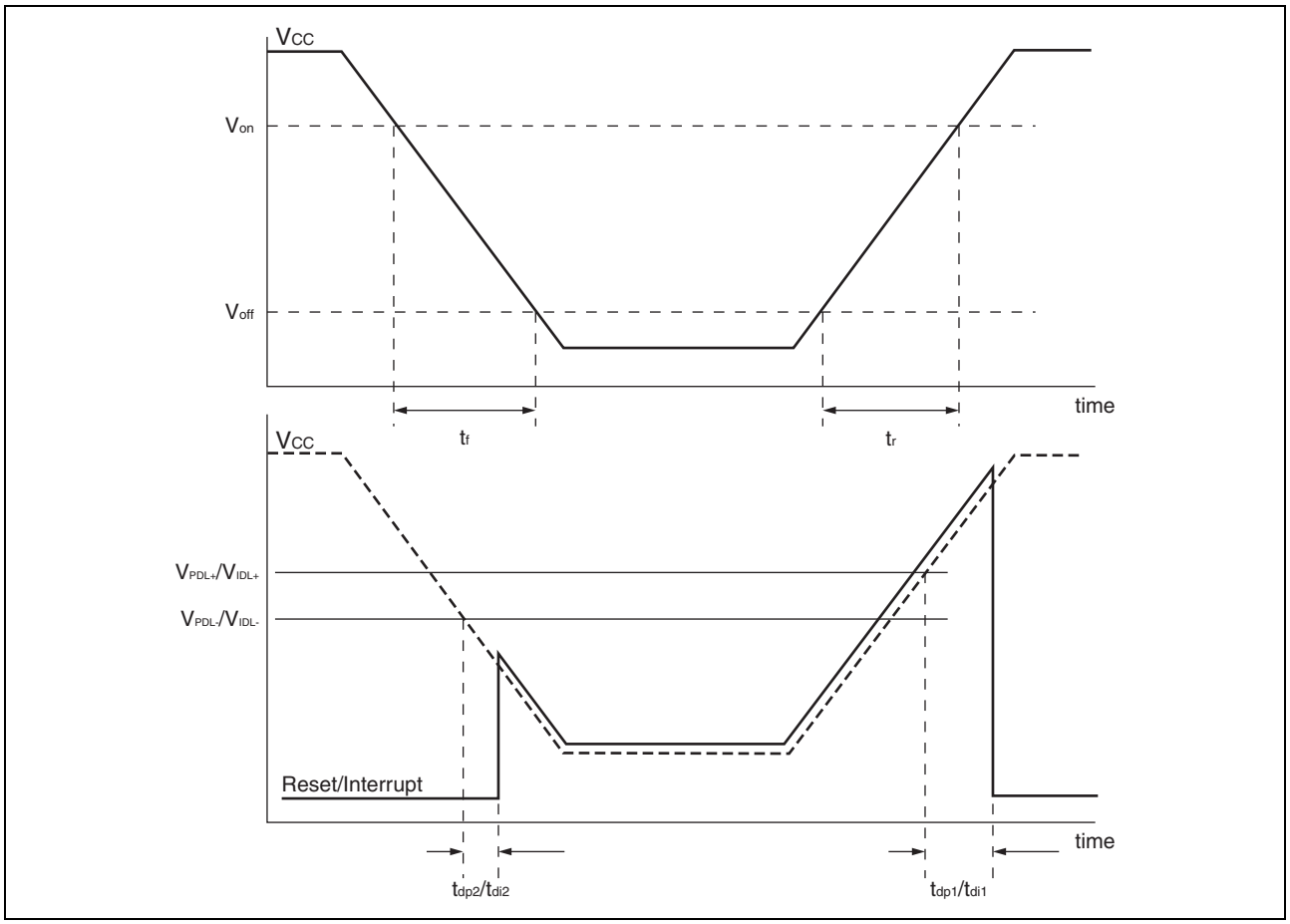
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power release voltage 0	V_{PDL0+}	1.83	1.93	2.03	V	At power supply rise
Power detection voltage 0	V_{PDL0-}	1.80	1.90	2.00	V	At power supply fall
Power release voltage 1	V_{PDL1+}	2.25	2.40	2.55	V	At power supply rise
Power detection voltage 1	V_{PDL1-}	2.20	2.35	2.50	V	At power supply fall
Power release voltage 2	V_{PDL2+}	2.80	2.95	3.10	V	At power supply rise
Power detection voltage 2	V_{PDL2-}	2.70	2.85	3.00	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.03	2.18	2.33	V	At power supply rise
Interrupt detection voltage 0	V_{IDL0-}	2.00	2.15	2.30	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.25	2.40	2.55	V	At power supply rise
Interrupt detection voltage 1	V_{IDL1-}	2.20	2.35	2.50	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.46	2.61	2.76	V	At power supply rise
Interrupt detection voltage 2	V_{IDL2-}	2.40	2.55	2.70	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	2.67	2.82	2.97	V	At power supply rise
Interrupt detection voltage 3	V_{IDL3-}	2.60	2.75	2.90	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	2.90	3.10	3.30	V	At power supply rise
Interrupt detection voltage 4	V_{IDL4-}	2.80	3.00	3.20	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.8	V	
Power supply end voltage	V_{on}	3.3	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})
Power supply voltage change time (at power supply fall)	t_f	3000	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{PDL-}/V_{IDL-})

(Continued)

(Continued)

(V_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power reset release delay time	t_{dp1}	10	—	300	µs	
Power reset detection delay time	t_{dp2}	—	—	150	µs	
Interrupt reset release delay time	t_{di1}	10	—	200	µs	
Interrupt reset detection delay time	t_{di2}	—	—	150	µs	



18.4.8 I²C Timing

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0, SDA0		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCL0		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCL0		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0, SDA0		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL0, SDA0		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL0, SDA0		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0, SDA0		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL0, SDA0		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL0 and SDA0 lines, and C the load capacitor of the SCL0 and SDA0 lines.

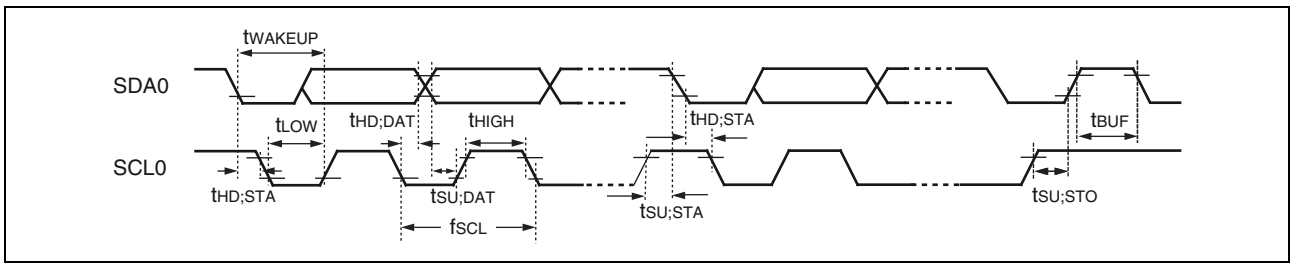
*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.

(Continued)

(Continued)

Note: The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA0 and SCL0 if the rating of the input data set-up time cannot be satisfied.



(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm / 2)\ t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0		$(nm / 2)t_{MCLK} - 20$	$(nm / 2)t_{MCLK} + 20$	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL0, SDA0		$(-1 + nm / 2)\ t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL0, SDA0		$(1 + nm / 2)\ t_{MCLK} - 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL0, SDA0		$(1 + nm / 2)t_{MCLK} - 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL0, SDA0		$(2\ nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SDA0		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0, SDA0		$(-2 + nm / 2)t_{MCLK} - 20$	$(-1 + nm / 2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.

(Continued)

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0	R = 1.7 kΩ, C = 50 pF*1	(nm / 2)t_{MCLK} − 20	(1 + nm / 2)t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL¬. Maximum value is applied to interrupt at 8th SCL¬.
SCL clock “L” width	t_{LOW}	SCL0		4 t_{MCLK} − 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL0		4 t_{MCLK} − 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL0, SDA0		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Stop condition detection	$t_{SU;STO}$	SCL0, SDA0		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL0, SDA0		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL0, SDA0		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0, SDA0		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0, SDA0		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0, SDA0		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0, SDA0		t_{MCLK} − 20	—	ns	At reception
SDA¬∅ SCLf (at wakeup function)	t_{WAKEUP}	SCL0, SDA0		Oscillation stabilization wait time + 2 t_{MCLK} − 20	—	ns	

(Continued)

(Continued)

*1: R represents the pull-up resistor of the SCL0 and SDA0 lines, and C the load capacitor of the SCL0 and SDA0 lines.

*2:
- See “(2) Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8): 0.9 MHz < $t_{MCLK} \leq$ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4): 0.9 MHz < $t_{MCLK} \leq$ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8): 0.9 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22): 0.9 MHz < $t_{MCLK} \leq$ 10 MHz
  (m, n) = (8, 22): 0.9 MHz < $t_{MCLK} \leq$ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8): 3.3 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 22), (5, 4): 3.3 MHz < $t_{MCLK} \leq$ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4): 3.3 MHz < $t_{MCLK} \leq$ 10 MHz
  (m, n) = (5, 8): 3.3 MHz < $t_{MCLK} \leq$ 16.25 MHz

18.5 A/D Converter

18.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

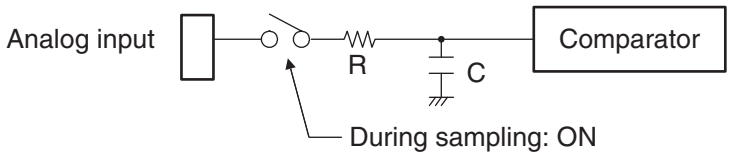
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	2.7 V ≤ V_{CC} ≤ 3.6 V
		AV_{SS} − 0.5 LSB	AV_{SS} + 1.5 LSB	AV_{SS} + 3.5 LSB	V	1.8 V ≤ V_{CC} < 2.7 V
Full-scale transition voltage	V_{FST}	AV_{CC} − 3.5 LSB	AV_{CC} − 1.5 LSB	AV_{CC} + 0.5 LSB	V	2.7 V ≤ V_{CC} ≤ 3.6 V
		AV_{CC} − 2.5 LSB	AV_{CC} − 0.5 LSB	AV_{CC} + 1.5 LSB	V	1.8 V ≤ V_{CC} < 2.7 V
Compare time	—	0.6	—	140	µs	2.7 V ≤ V_{CC} ≤ 3.6 V
		20	—	140	µs	1.8 V ≤ V_{CC} < 2.7 V
Sampling time	—	0.4	—	∞	µs	2.7 V ≤ V_{CC} ≤ 3.6 V, with external impedance < 1.8 kΩ
		30	—	∞	µs	1.8 V ≤ V_{CC} < 2.7 V, with external impedance < 14.8 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	

18.5.2 Notes on Using the A/D Converter

■ **External impedance of analog input and its sampling time**

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

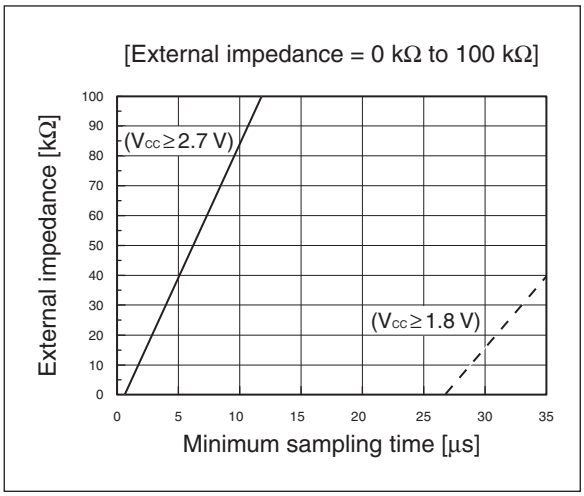
- Analog input equivalent circuit

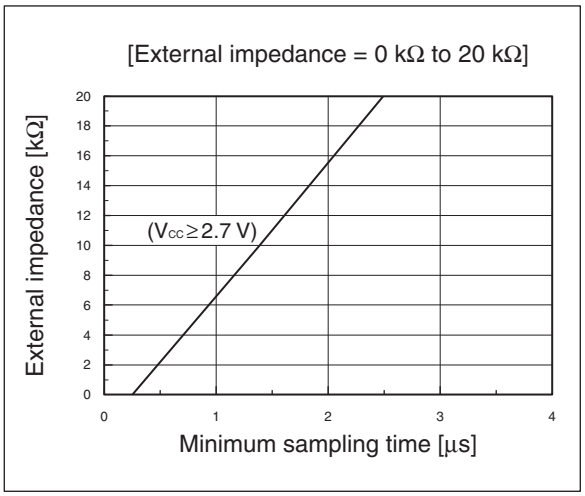


V_{CC}	R	C
2.7 V ≤ V_{CC} ≤ 3.6V	1.7 kΩ (Max)	14.5 pF (Max)
1.8 V ≤ V_{CC} < 2.7 V	8.4 kΩ (Max)	25.2 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time





■ **A/D conversion error**

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

18.5.3 Definitions of A/D Converter Terms

■ Resolution

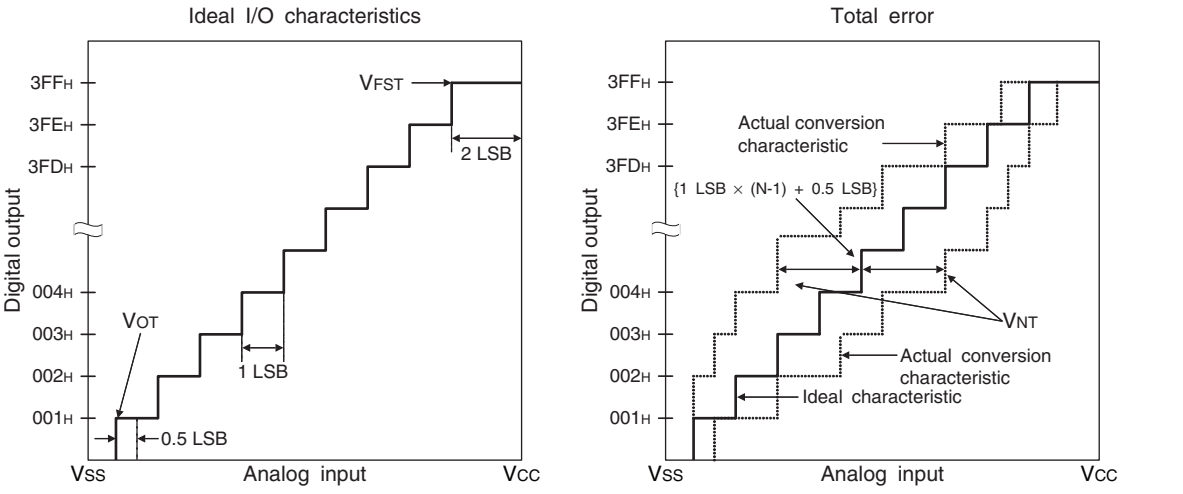
It indicates the level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.

■ Linearity error (unit: LSB)

It indicates how much an actual conversion value deviates from the straight line connecting

the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to
the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.

- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ LSB = \frac{V_{CC} - V_{SS}}{1024}\ (V)$$

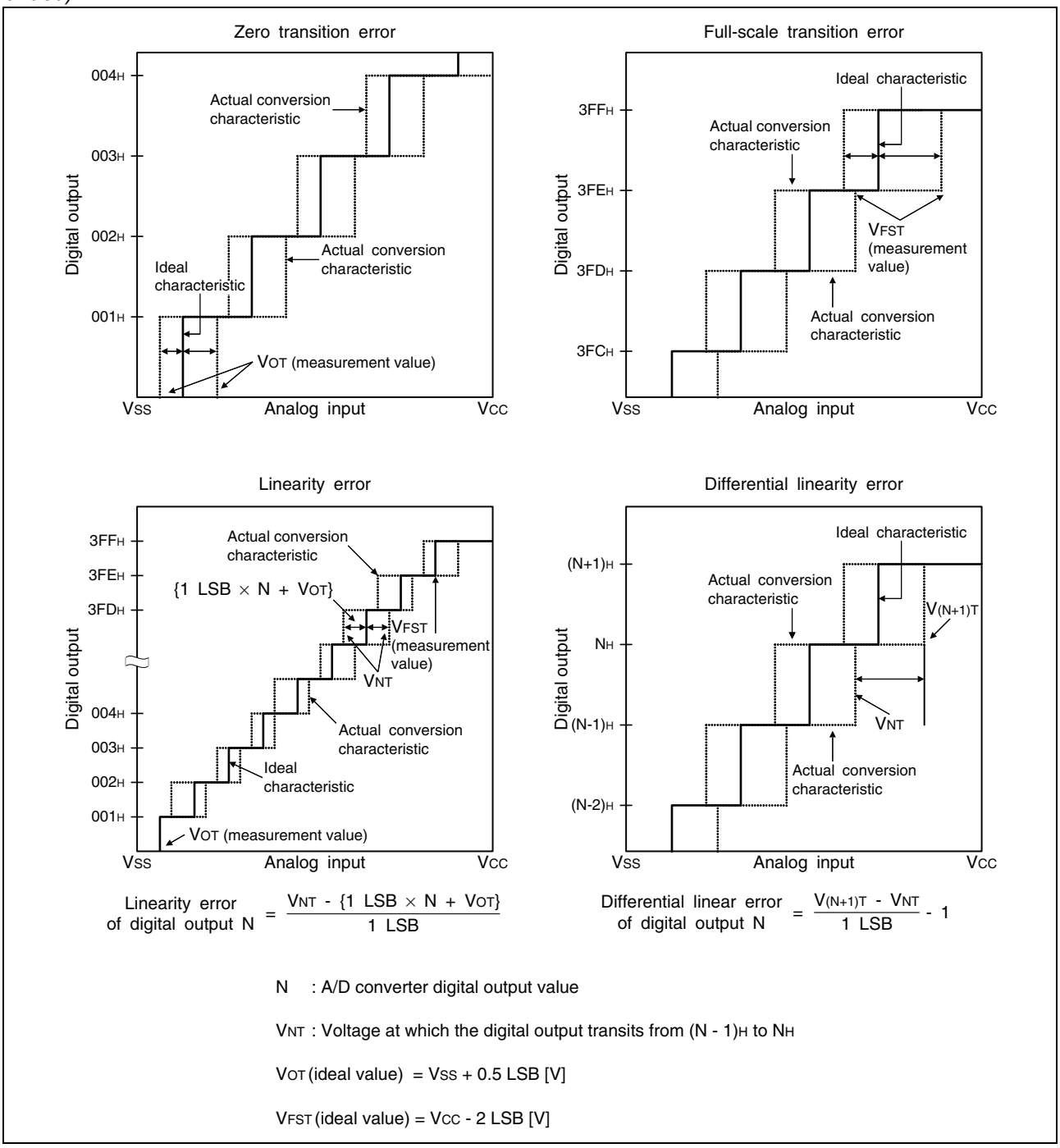
$$\text{Total error of digital output } N = \frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}\ [LSB]$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

18.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of programming 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of programming 00_H prior to erasure is excluded.
Byte programming time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	2.7	3.0	3.6	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 3.0 V, 100000 cycles

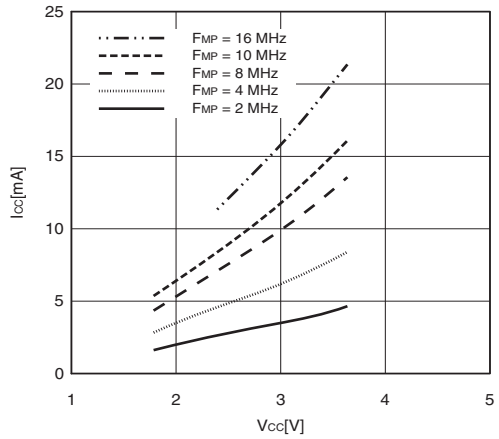
*2: T_A = +85°C, V_{CC} = 2.7 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

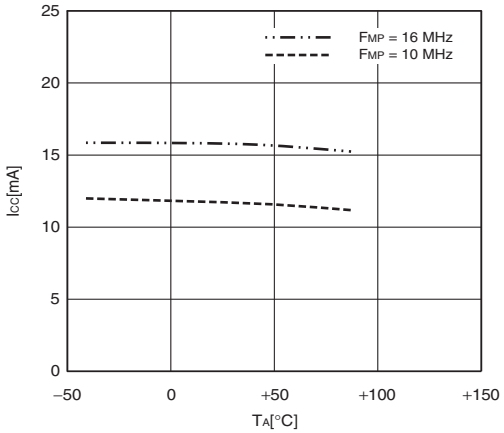
19. Sample Characteristics

- Power supply current temperature characteristics

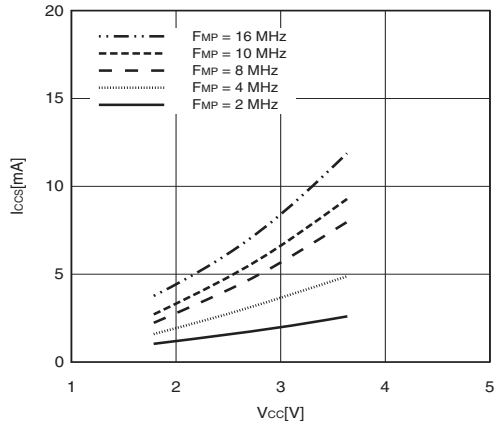
$I_{CC} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



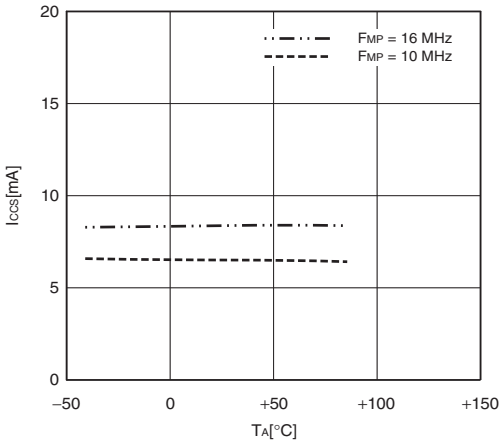
$I_{CC} - T_A$
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



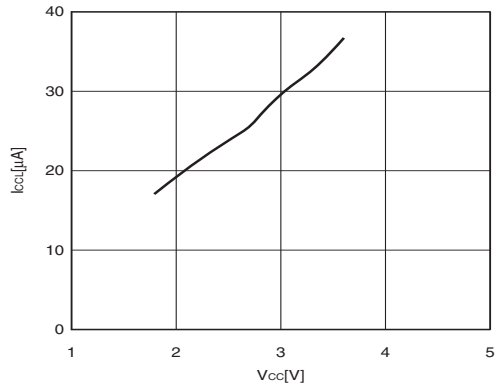
$I_{CCS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



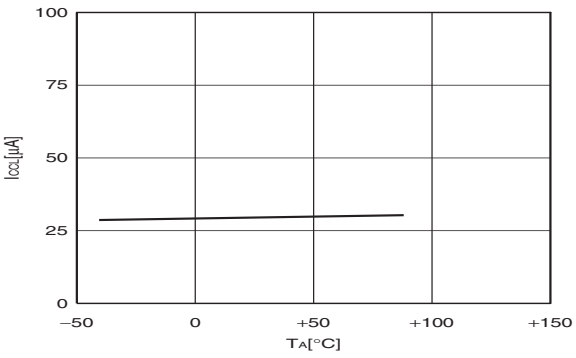
$I_{CCS} - T_A$
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



$I_{CCL} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

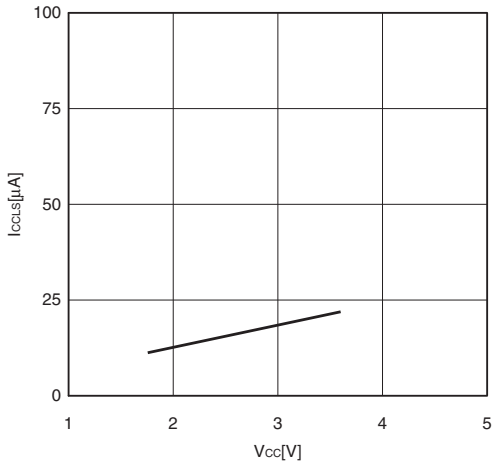


ICCL —TA
VCC = 3.0 V, FMPL = 16 kHz (divided by 2)
Subclock mode with the external clock operating

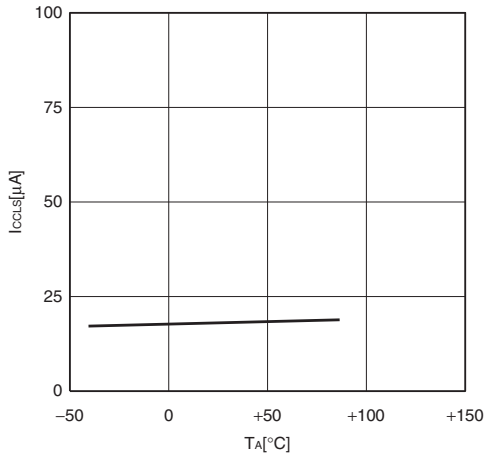


(Continued)

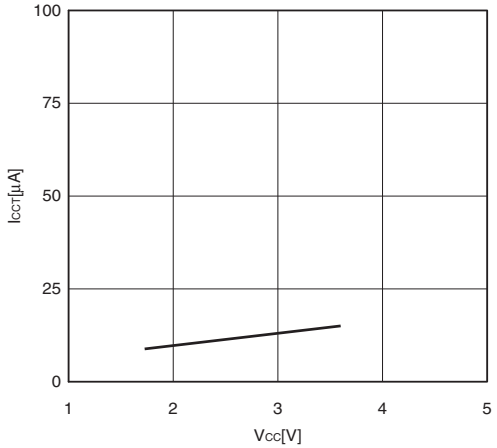
I_{CCLS} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



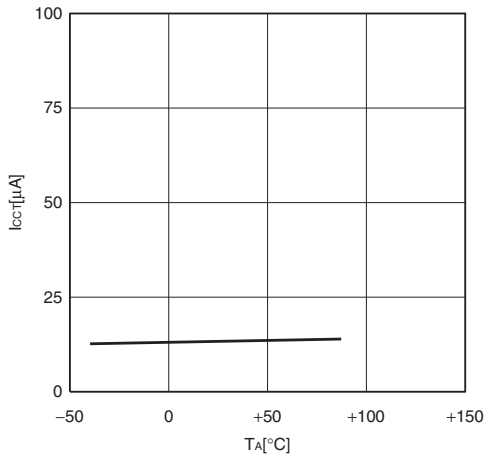
I_{CCLS} – T_A
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



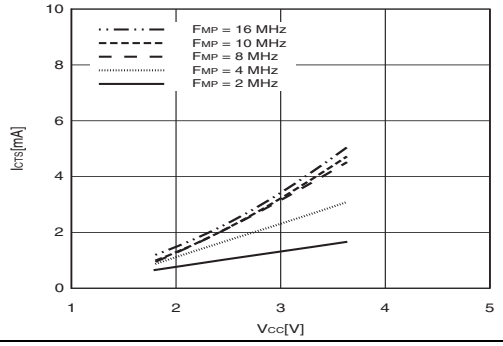
I_{CCT} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



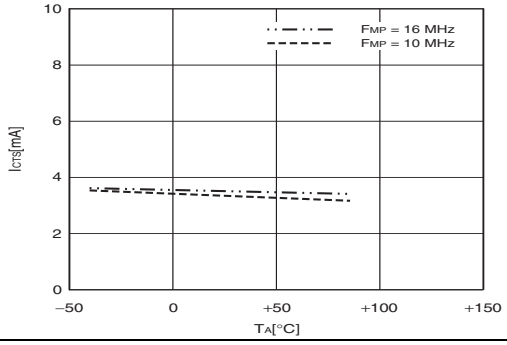
I_{CCT} – T_A
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



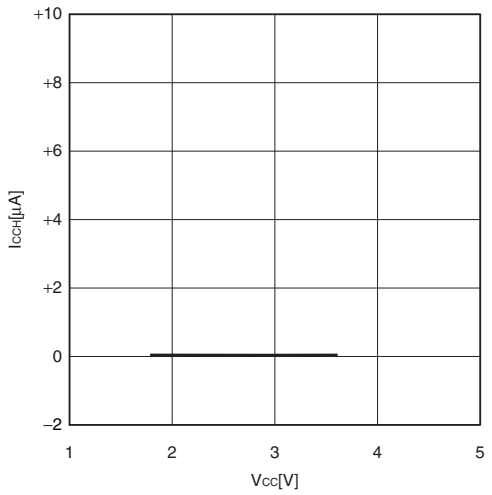
I_{CTS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



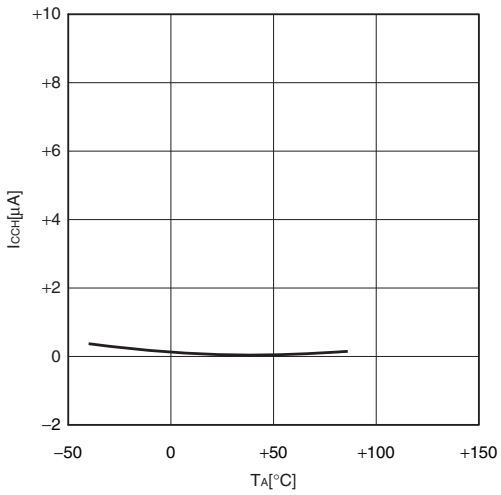
I_{CTS} – T_A
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



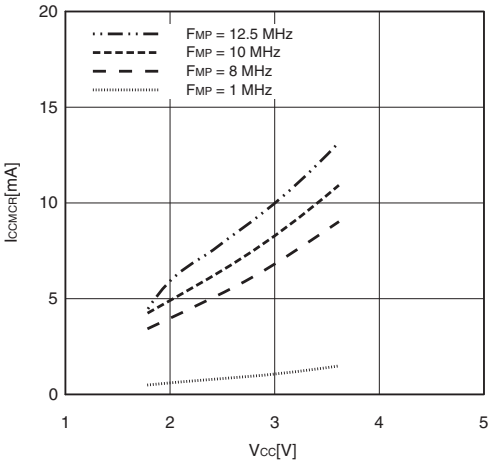
I_{CCH} – V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



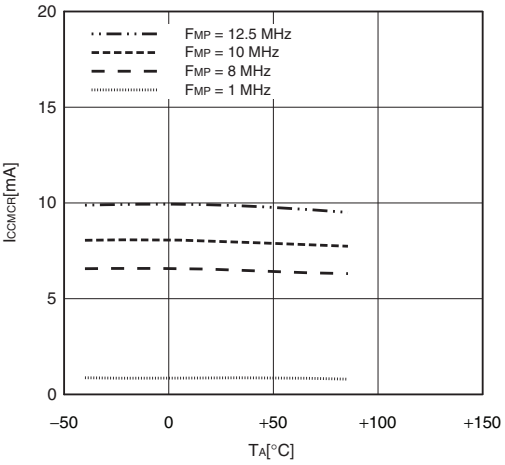
I_{CCH} – T_A
V_{CC} = 3.0 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



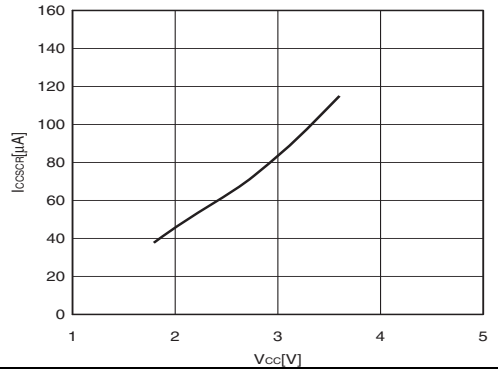
I_{CCMCR} – V_{CC}
T_A = +25°C, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



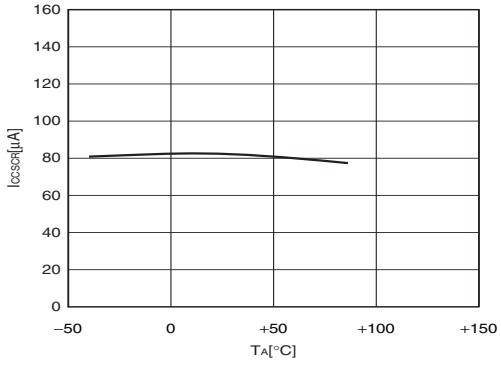
I_{CCMCR} – T_A
V_{CC} = 3.0 V, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



I_{CCSCR} – V_{CC}
T_A = +25°C, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

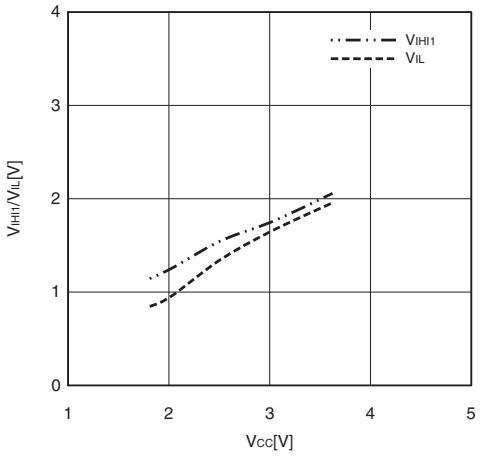


I_{CCSCR} – T_A
V_{CC} = 3.0 V, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

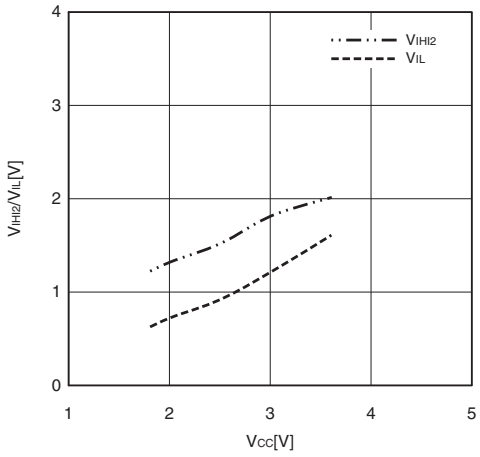


- Input voltage characteristics

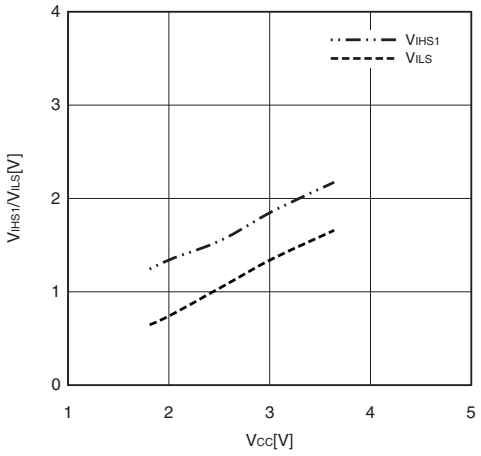
V_{IHI1} – V_{CC} and V_{IL} – V_{CC}
T_A = +25°C



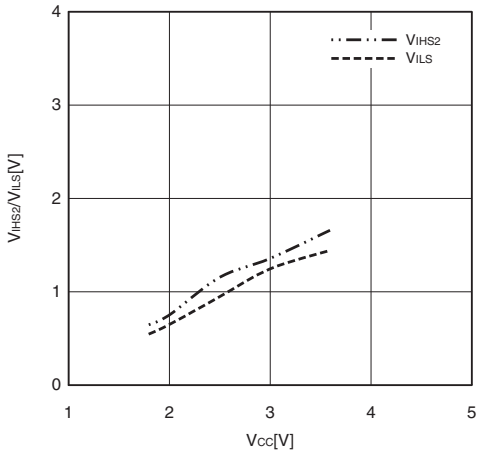
V_{IHI2} – V_{CC} and V_{IL} – V_{CC}
T_A = +25°C



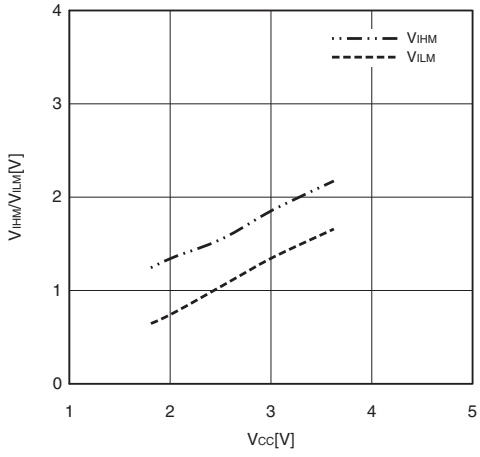
V_{IHS1} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C



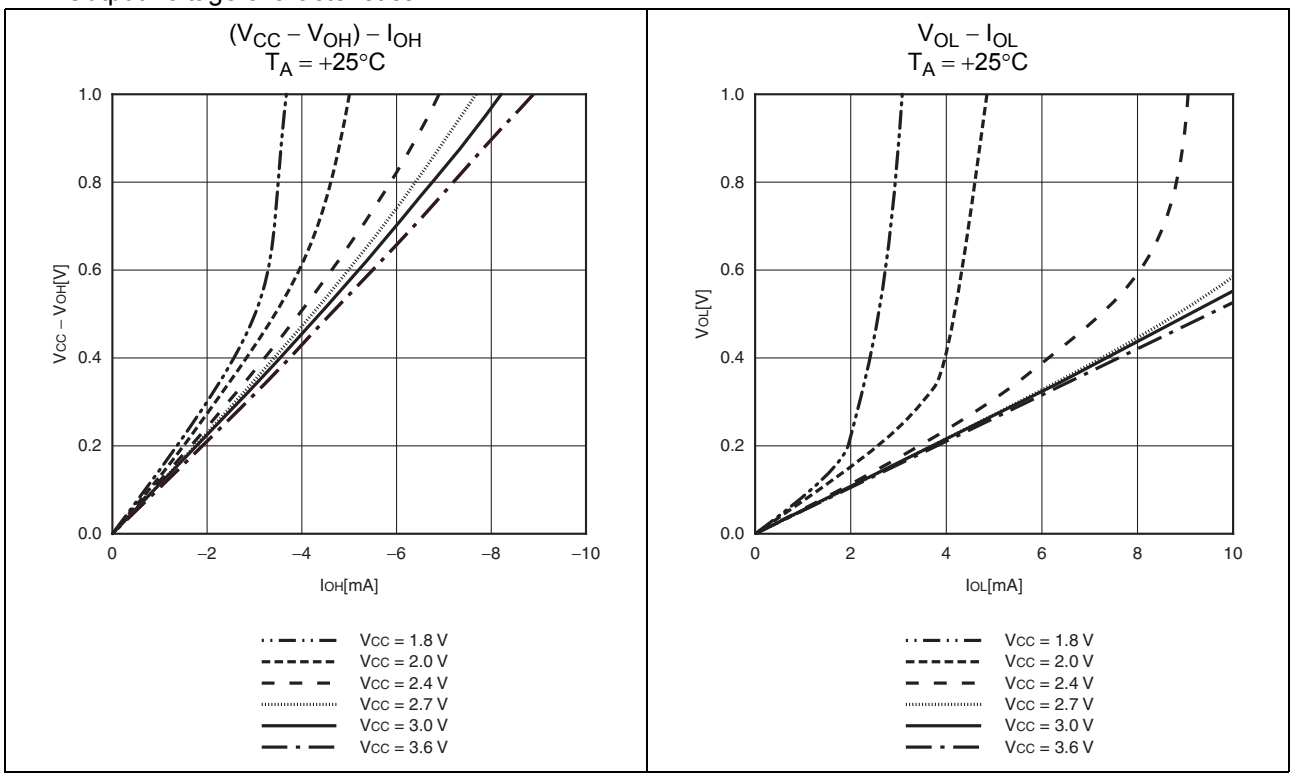
V_{IHS2} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C



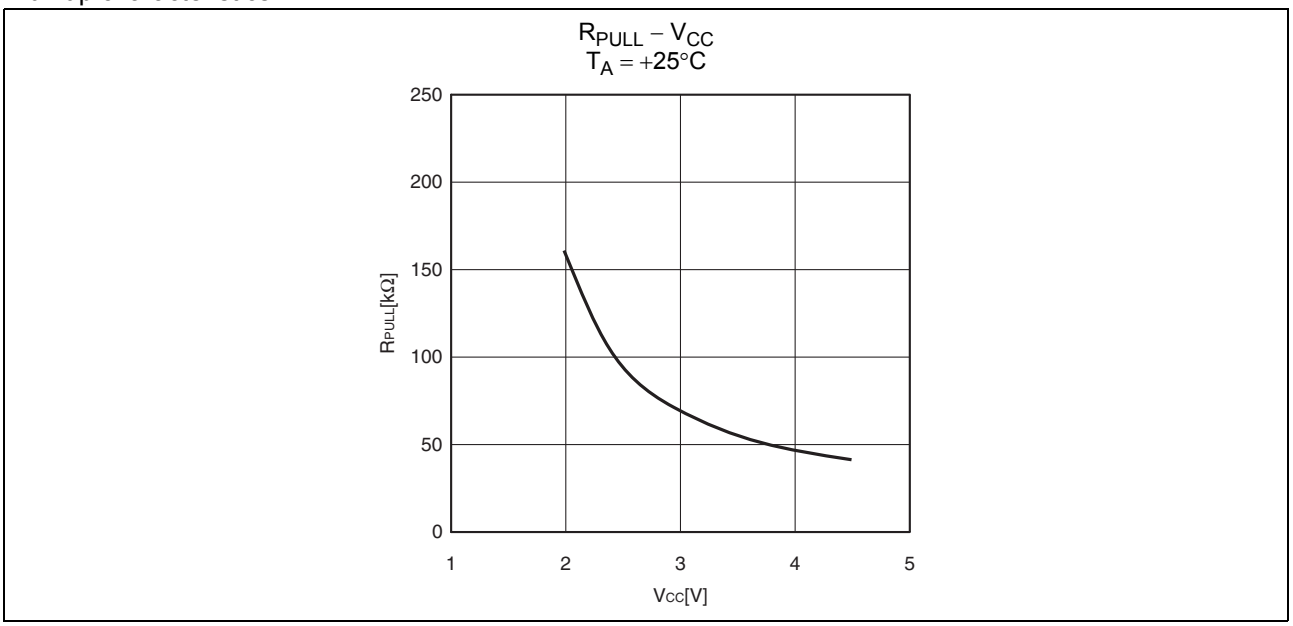
V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25°C



- Output voltage characteristics



- Pull-up characteristics



20. Mask Options

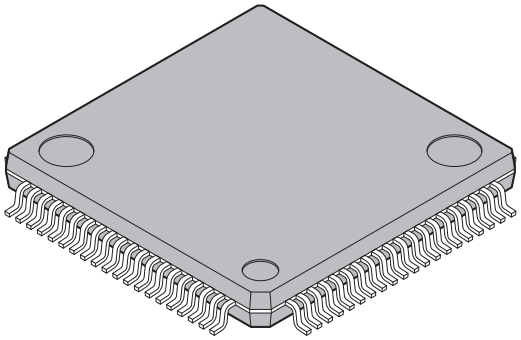
No.	Part Number	MB95F314E MB95F316E MB95F318E MB95F374E MB95F376E MB95F378E	MB95F314L MB95F316L MB95F318L MB95F374L MB95F376L MB95F378L
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	With low-voltage detection reset	Without low-voltage detection reset

21. Ordering Information

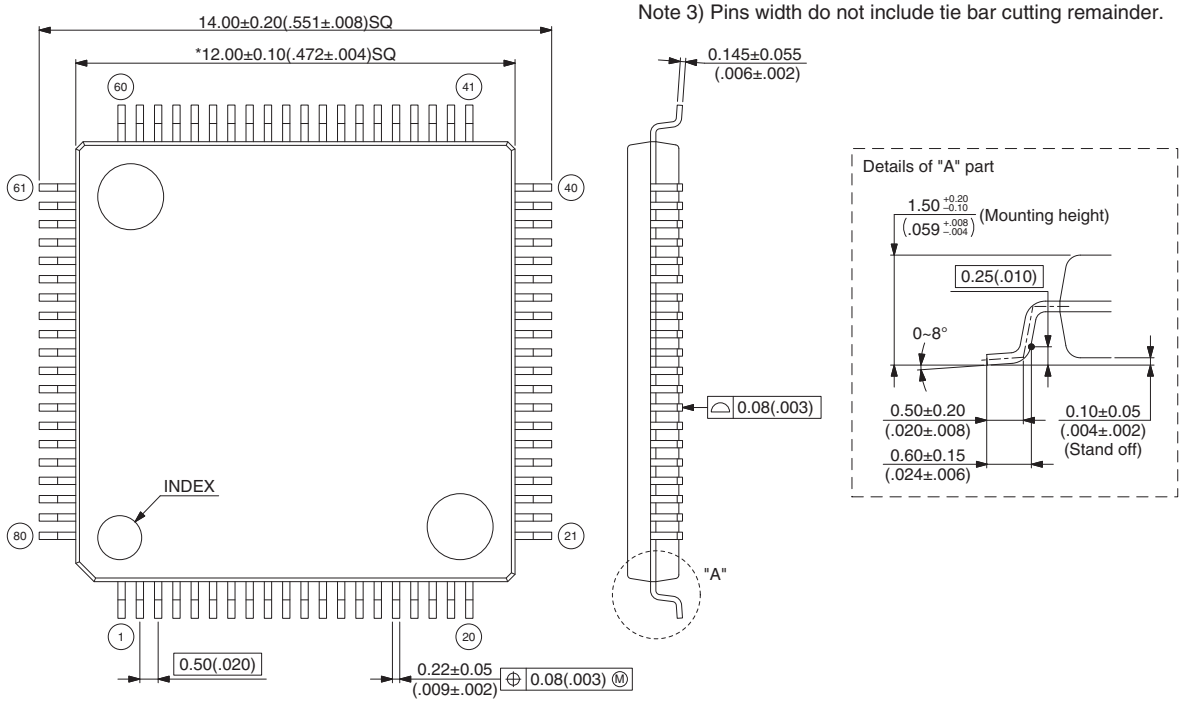
Part Number	Package
MB95F314EPMC-G-SNE2 MB95F314LPMC-G-SNE2 MB95F316EPMC-G-SNE2 MB95F316LPMC-G-SNE2 MB95F318EPMC-G-SNE2 MB95F318LPMC-G-SNE2	80-pin plastic LQFP (FPT-80P-M37)
MB95F374EPMC1-G-SNE2 MB95F374LPMC1-G-SNE2 MB95F376EPMC1-G-SNE2 MB95F376LPMC1-G-SNE2 MB95F378EPMC1-G-SNE2 MB95F378LPMC1-G-SNE2	64-pin plastic LQFP (FPT-64P-M38)

Part Number	Package
MB95F374EPMC2-G-SNE2 MB95F374LPMC2-G-SNE2 MB95F376EPMC2-G-SNE2 MB95F376LPMC2-G-SNE2 MB95F378EPMC2-G-SNE2 MB95F378LPMC2-G-SNE2	64-pin plastic LQFP (FPT-64P-M39)

22. Package Dimension

80-pin plastic LQFP		
 (FPT-80P-M37)	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g

80-pin plastic LQFP
(FPT-80P-M37)



Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

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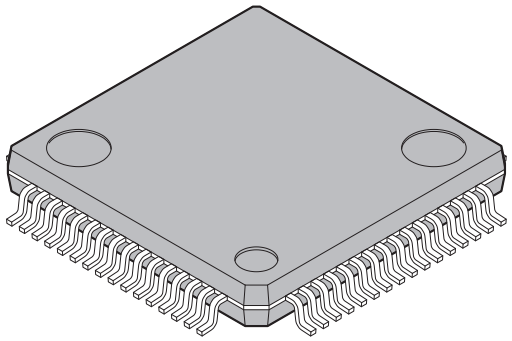
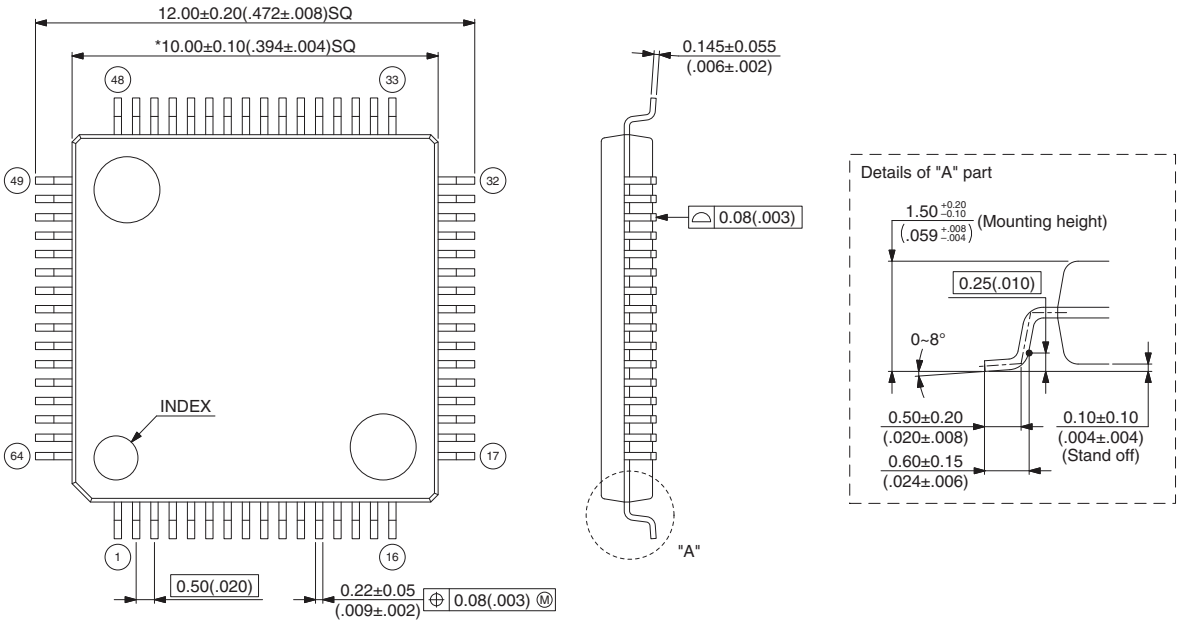
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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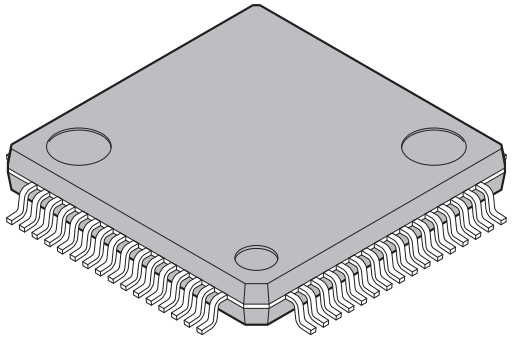
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

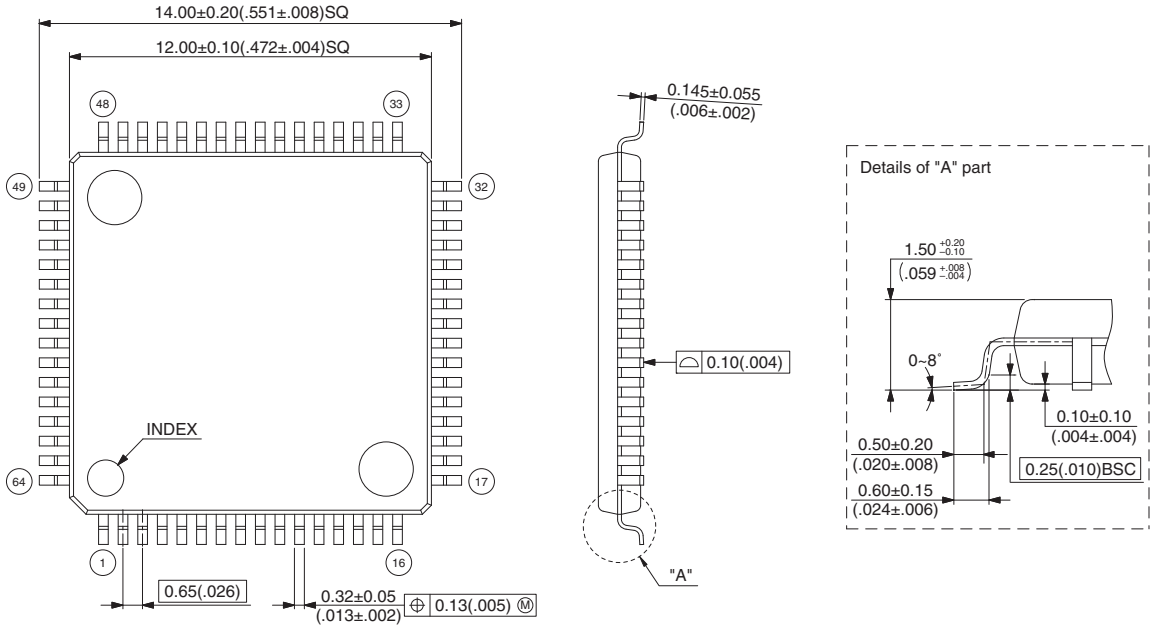
(Continued)

(Continued)

64-pin plastic LQFP		
 (FPT-64P-M39)	Lead pitch	0.65 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

23. Major Changes

Spansion Publication Number: DS07-12628-2E

Page	Section	Details
1	—	Changed the family name. F^2MC-8FX → New 8FX
1	Features	Changed the main CR clock oscillation frequency. 1/8/10 MHz ±3%, maximum machine clock frequency: 10 MHz → 1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz
23	Pin Connection	Added "• Notes on handling the external clock pins while using the CR clock".
46	Electrical Characteristics DC Characteristics	Changed the condition for the power supply current (I_{CCMCR}). F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode → F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode Changed the condition for the power supply current (I_{CCSCR}). F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub-CR clock mode (divided by 2) T_A = +25°C → Sub-CR clock mode (divided by 2) T_A = +25°C
47		Changed the condition for the power supply current (I_{CRH}). Current consumption for the main CR oscillator at 10 MHz → Current consumption for the main CR oscillator
48	Electrical Characteristics AC Characteristics Clock Timing	Changed the values of the clock frequency (F_{CRH}).
58	Electrical Characteristics AC Characteristics Low-voltage Detection	Deleted the following parameters: Power hysteresis width 0, Power hysteresis width 1, Power hysteresis width 2, Interrupt hysteresis width 0, Interrupt hysteresis width 1, Interrupt hysteresis width 2, Interrupt hysteresis width 3, Interrupt hysteresis width 4
59		Deleted V_{PHYS}/V_{IHYS} from the diagram.
64	Electrical Characteristics AC Characteristics I^2C Timing	Changed the settings related to the machine clock shown in *2.
70 to 75	Sample Characteristics	Added "■ SAMPLE CHARACTERISTICS".

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB95F314E/F314L/F316E/F316L/F318E/F318L, MB95F374E/F374L/F376E/F376L/F378E/F378L, New 8FX MB95310L/370L Series 8-bit Microcontrollers Document Number: 002-07519				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/13/2010	Migrated to Cypress and assigned document number 002-07519. No change to document contents or format.
*A	5180514	AKIH	04/05/2016	Updated to Cypress template
*B	5861651	YSAT	08/24/2017	Adapted new Cypress logo

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