



**THE DATASHEET OF  
LP2988IM-3.3/NOPB**



# LP2987/LP2988 Micropower, 200 mA Ultra Low-Dropout Voltage Regulator with Programmable Power-On Reset Delay; Low Noise Version Available (LP2988)

Check for Samples: [LP2987](#), [LP2988](#)

## FEATURES

- Ultra Low Dropout Voltage
- Power-ON Reset Delay Requires Only One Component
- Bypass Pin for Reduced Output Noise (LP2988)
- Specified Continuous Output Current 200 mA
- Specified Peak Output Current > 250 mA
- SOIC-8 and VSSOP-8 Surface Mount Packages
- <2  $\mu\text{A}$  Quiescent Current when Shutdown
- Low Ground Pin Current at All Loads
- 0.5% Output Voltage Accuracy ("A" Grade)
- Wide Supply Voltage Range (16V Max)
- Overtemperature/overcurrent Protection
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Junction Temperature Range

## APPLICATIONS

- Cellular Phone
- Palmtop/Laptop Computer
- Camcorder, Personal Stereo, Camera

## DESCRIPTION

The LP2987/8 are fixed-output 200 mA precision LDO voltage regulators with power-ON reset delay which can be implemented using a single external capacitor.

The LP2988 is specifically designed for noise-critical applications. A single external capacitor connected to the Bypass pin reduces regulator output noise.

Using an optimized VIP (Vertically Integrated PNP) process, these regulators deliver superior performance:

**Dropout Voltage:** 180 mV @ 200 mA load, and 1 mV @ 1 mA load (typical).

**Ground Pin Current:** 1 mA @ 200 mA load, and 200  $\mu\text{A}$  @ 10 mA load (typical).

**Sleep Mode:** The LP2987/8 draws less than 2  $\mu\text{A}$  quiescent current when shutdown pin is held low.

**Error Flag/Reset:** The error flag goes low when the output drops approximately 5% below nominal. This pin also provides a power-ON reset signal if a capacitor is connected to the DELAY pin.

**Precision Output:** Standard product versions of the LP2987 and LP2988 are available with output voltages of 5.0V, 3.8V, 3.3V, 3.2V, 3.0V, or 2.8V, with specified accuracy of 0.5% ("A" grade) and 1% (standard grade) at room temperature.

## Block Diagram



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**Connection Diagram (LP2987)**



**Figure 1. Top View  
SOIC-8/VSSOP-8 Package  
Surface Mount Packages  
See Package Drawing Number D0008A/DGK0008A**



**Figure 2. Top View  
8-Lead WSON Surface Mount Package  
See Package Drawing Number NGN0008A**

**Connection Diagram (LP2988)**



**Figure 3. Top View  
SOIC-8/VSSOP-8 Package  
Surface Mount Packages  
See Package Drawing Number D0008A/DGK0008A**



**Figure 4. Top View  
8-Lead WSON Surface Mount Package  
See Package Drawing Number NGN0008A**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	-40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating <sup>(3)</sup>	2 kV
Power Dissipation <sup>(4)</sup>	Internally Limited
Input Supply Voltage (Survival)	-0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
Shutdown Pin	-0.3V to +16V
Sense Pin	-0.3V to +6V
Output Voltage (Survival) <sup>(5)</sup>	-0.3V to +16V
I <sub>OUT</sub> (Survival)	Short Circuit Protected
Input-Output Voltage (Survival) <sup>(6)</sup>	-0.3V to +16V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) The ESD rating of the Bypass pin is 500V (LP2988 only). The ESD rating of the V<sub>IN</sub> pin is 1kV and the Delay pin is ESD rated at 1.5kV.
- (4) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance, θ<sub>J-A</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using: 
$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$
 The value of θ<sub>J-A</sub> for the SOIC-8 (D) package is 160°C/W, and the VSSOP-8 (DGK) package is 200°C/W. The value θ<sub>J-A</sub> for the WSON (NGN) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (literature number [SNOA401](#)). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
- (5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LM2987/8 output must be diode-clamped to ground.
- (6) The output PNP structure contains a diode between the V<sub>IN</sub> and V<sub>OUT</sub> terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see [APPLICATION HINTS](#)).

## ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T<sub>J</sub> = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V<sub>IN</sub> = V<sub>O</sub>(NOM) + 1V, I<sub>L</sub> = 1 mA, C<sub>OUT</sub> = 4.7 μF, C<sub>IN</sub> = 2.2 μF, V<sub>SD</sub> = 2V.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X <sup>(1)</sup>		LM2987/8I-X.X <sup>(1)</sup>		Units
				Min	Max	Min	Max	
ΔV <sub>O</sub>	Output Voltage Tolerance	0.1 mA < I <sub>L</sub> < 200 mA		-0.5	0.5	-1.0	1.0	%V <sub>NOM</sub>
				-0.8	0.8	-1.6	1.6	
				<b>-1.8</b>	<b>1.8</b>	<b>-2.8</b>	<b>2.8</b>	
ΔV <sub>O</sub> /ΔV <sub>IN</sub>	Output Voltage Line Regulation	V <sub>O</sub> (NOM) + 1V ≤ V <sub>IN</sub> ≤ 16V	0.007		0.014		0.014	%V
					<b>0.032</b>		<b>0.032</b>	

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

### ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified:  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{OUT} = 4.7\ \mu\text{F}$ ,  $C_{IN} = 2.2\ \mu\text{F}$ ,  $V_{S/D} = 2\text{V}$ .

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X <sup>(1)</sup>		LM2987/8I-X.X <sup>(1)</sup>		Units
				Min	Max	Min	Max	
$V_{IN-V_O}$	Dropout Voltage <sup>(2)</sup>	$I_L = 100\ \mu\text{A}$	1		2.0		2.0	mV
		$I_L = 75\ \text{mA}$	90		<b>3.5</b>		<b>3.5</b>	
		$I_L = 200\ \text{mA}$	180		120		120	
$I_{GND}$	Ground Pin Current	$I_L = 100\ \mu\text{A}$	100		120		120	$\mu\text{A}$
		$I_L = 75\ \text{mA}$	500		<b>150</b>		<b>150</b>	
		$I_L = 200\ \text{mA}$	1		800		800	mA
		$V_{S/D} < 0.3\text{V}$	0.05		<b>1400</b>		<b>1400</b>	
$I_O(\text{PK})$	Peak Output Current	$V_{OUT} \geq V_O(\text{NOM}) - 5\%$	400	250		250		mA
$I_O(\text{MAX})$	Short Circuit Current	$R_L = 0$ (Steady State) <sup>(3)</sup>	400					
$e_n$	LP2987 Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, $V_{OUT} = 3.3\text{V}$ $C_{OUT} = 10\ \mu\text{F}$	100					$\mu\text{V}(\text{RMS})$
	LP2988 Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, $V_{OUT} = 3.3\text{V}$ $C_{OUT} = 10\ \mu\text{F}$ $C_{BYPASS} = .01\ \mu\text{F}$	20					
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple Rejection	$f = 1\ \text{kHz}$ , $C_{OUT} = 10\ \mu\text{F}$ $C_{BYP} = 0$ (LP2988)	65					dB
$\Delta V_{OUT}/\Delta T$	Output Voltage Temperature Coefficient	<sup>(4)</sup>	20					ppm/ $^\circ\text{C}$
$I_{DELAY}$	Delay Pin Current Source		2.2	1.6	2.8	1.6	2.8	$\mu\text{A}$
				<b>1.4</b>	<b>3.0</b>	<b>1.4</b>	<b>3.0</b>	
<b>SHUTDOWN INPUT</b>								
$V_{S/D}$	S/D Input Voltage <sup>(5)</sup>	$V_H = \text{O/P ON}$	1.4	<b>1.6</b>		<b>1.6</b>		V
		$V_L = \text{O/P OFF}$	0.55		<b>0.18</b>		<b>0.18</b>	
$I_{S/D}$	S/D Input Current	$V_{S/D} = 0$	0		<b>-1</b>		<b>-1</b>	$\mu\text{A}$
		$V_{S/D} = 5\text{V}$	5		<b>15</b>		<b>15</b>	

- (2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.
- (3) See [TYPICAL PERFORMANCE CHARACTERISTICS](#) curves.
- (4) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.
- (5) To prevent mis-operation, the Shutdown input must be driven by a signal that swings above  $V_H$  and below  $V_L$  with a slew rate not less than 40 mV/ $\mu\text{s}$  (see [APPLICATION HINTS](#)).

**ELECTRICAL CHARACTERISTICS (continued)**

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified:  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{OUT} = 4.7\ \mu\text{F}$ ,  $C_{IN} = 2.2\ \mu\text{F}$ ,  $V_{S/D} = 2\text{V}$ .

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X <sup>(1)</sup>		LM2987/8I-X.X <sup>(1)</sup>		Units
				Min	Max	Min	Max	
<b>ERROR COMPARATOR</b>								
$I_{OH}$	Output "HIGH" Leakage	$V_{OH} = 16\text{V}$	0.01		1		1	$\mu\text{A}$
					<b>2</b>		<b>2</b>	
$V_{OL}$	Output "LOW" Voltage	$V_{IN} = V_O(\text{NOM}) - 0.5\text{V}$ , $I_O(\text{COMP}) = 300\ \mu\text{A}$	150		220		220	mV
					<b>350</b>		<b>350</b>	
$V_{THR}(\text{MAX})$	Upper Threshold Voltage		-4.6	-5.5	-3.5	-5.5	-3.5	% $V_{OUT}$
				<b>-7.7</b>	<b>-2.5</b>	<b>-7.7</b>	<b>-2.5</b>	
$V_{THR}(\text{MIN})$	Lower Threshold Voltage		-6.6	-8.9	-4.9	-8.9	-4.9	
				<b>-13.0</b>	<b>-3.3</b>	<b>-13.0</b>	<b>-3.3</b>	
HYST	Hysteresis		2.0					

### TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1 \text{mA}$ .



Figure 5.



Figure 6.



Figure 7.



Figure 8.



Figure 9.



Figure 10.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1 \text{ mA}$ .



Figure 11.



Figure 12.



50  $\mu\text{s}/\text{Div}$   
Figure 13.



50  $\mu\text{s}/\text{Div}$   
Figure 14.



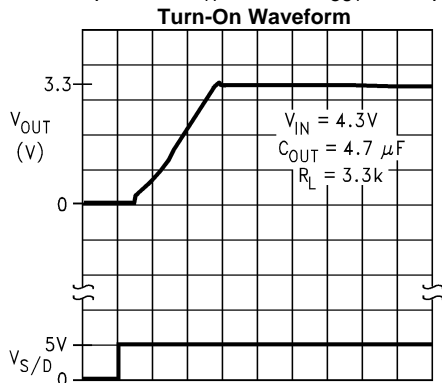
50  $\mu\text{s}/\text{Div}$   
Figure 15.



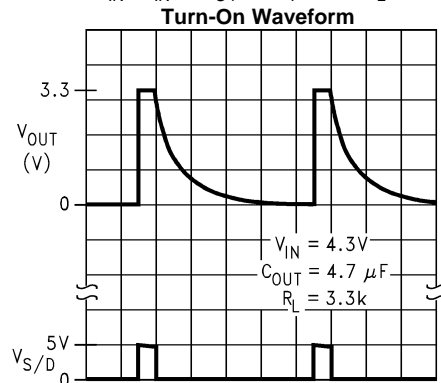
20  $\mu\text{s}/\text{Div}$   
Figure 16.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_{O(NOM)} + 1\text{V}$ ,  $I_L = 1 \text{ mA}$ .



20  $\mu\text{s}/\text{Div}$   
Figure 17.



20 ms/Div  
Figure 18.



500 ms/Div  
Figure 19.



200 ms/Div  
Figure 20.

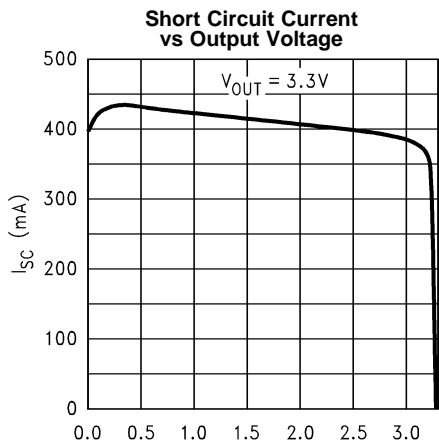


Figure 21.



Figure 22.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1 \text{ mA}$ .



Figure 23.



Figure 24.



Figure 25.



Figure 26.



Figure 27.



Figure 28.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1 \text{ mA}$ .

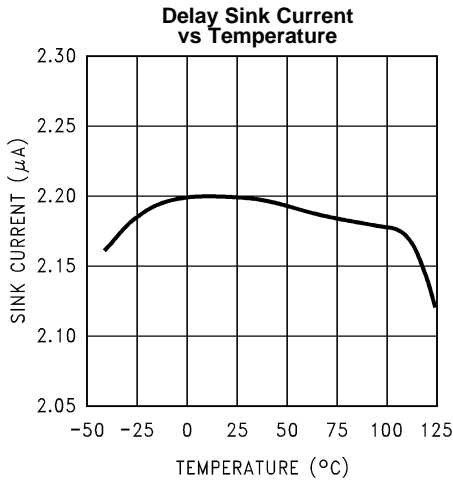


Figure 29.



Figure 30.



Figure 31.

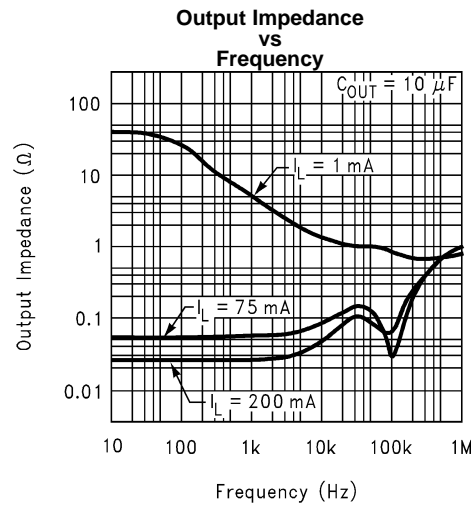


Figure 32.



Figure 33.

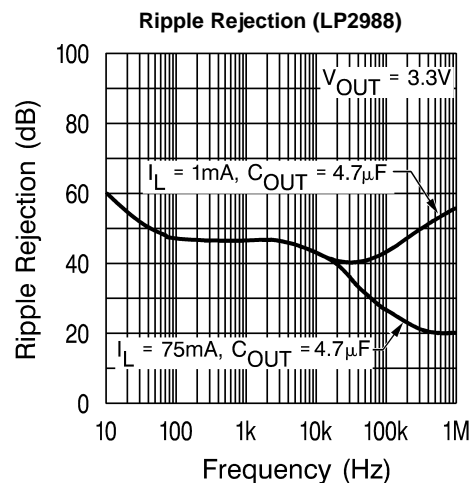


Figure 34.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1 \text{ mA}$ .



Figure 35.



Figure 36.



Figure 37.



Figure 38.



Figure 39.



Figure 40.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $C_{IN} = 2.2 \mu\text{F}$ , S/D is tied to  $V_{IN}$ ,  $V_{IN} = V_O(\text{NOM}) + 1\text{V}$ ,  $I_L = 1 \text{ mA}$ .

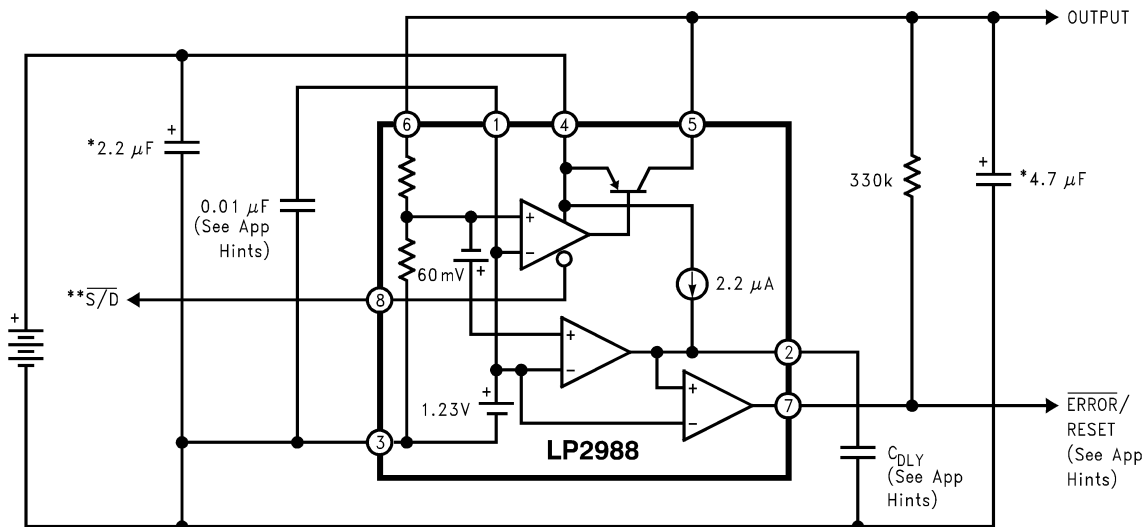


**Figure 41.**

BASIC APPLICATION CIRCUITS



Figure 42.



\*Capacitance value shown is minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

\*\*Shutdown must be actively terminated (see APPLICATION HINTS). Tie to INPUT (pin 4) if not used.

Figure 43.

## APPLICATION HINTS

### WSO Package Devices

The LP2987/LP2988 is offered in the 8 lead WSO surface mount package to allow for increased power dissipation compared to the SOIC-8 and the VSSOP-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187 (literature number [SNOA401](#)).

### EXTERNAL CAPACITORS

As with any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

**INPUT CAPACITOR:** An input capacitor ( $\geq 2.2 \mu\text{F}$ ) is required between the LP2987/8 input and ground (amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 0.5" from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor.

**OUTPUT CAPACITOR:** The output capacitor must meet the requirement for minimum amount of capacitance and also have an appropriate E.S.R. (equivalent series resistance) value.

Curves are provided which show the allowable ESR range as a function of load current for 3V and 5V outputs.



Figure 44. ESR Curves For 5V Output



Figure 45. ESR Curves For 3V Output

**IMPORTANT:** The output capacitor must maintain its ESR in the stable region *over the full operating temperature range of the application* to assure stability.

The minimum required amount of output capacitance is  $4.7 \mu\text{F}$ . Output capacitor size can be increased without limit.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. A good Tantalum capacitor will show very little variation with temperature, but a ceramic may not be as good (see next section).

The output capacitor should be located not more than 0.5" from the output pin and returned to a clean analog ground.

## CAPACITOR CHARACTERISTICS

**TANTALUM:** A solid tantalum capacitor is the best choice for the output capacitor on the LM2987/8. Available from many sources, their typical ESR is very close to the ideal value required on the output of many LDO regulators.

Tantalums also have good temperature stability: a 4.7  $\mu\text{F}$  was tested and showed only a 10% decline in capacitance as the temperature was decreased from +125°C to -40°C. The ESR increased only about 2:1 over the same range of temperature.

However, it should be noted that the increasing ESR at lower temperatures present in all tantalums can cause oscillations when marginal quality capacitors are used (where the ESR of the capacitor is near the upper limit of the stability range at room temperature).

**CERAMIC:** The ESR of ceramic capacitor can be low enough to cause an LDO regulator to oscillate: a 2.2  $\mu\text{F}$  ceramic was measured and found to have an ESR of 15 m $\Omega$ .

If a ceramic capacitor is to be used on the LP2987/8 output, a 1 $\Omega$  resistor should be placed in series with the capacitor to provide a minimum ESR for the regulator.

A disadvantage of ceramic capacitors is that their capacitance varies a lot with temperature: Large ceramic capacitors are typically manufactured with the Z5U temperature characteristic, which results in the capacitance dropping by 50% as the temperature goes from 25°C to 80°C.

This means you have to buy a capacitor with twice the minimum  $C_{\text{OUT}}$  to assure stable operation up to 80°C.

**ALUMINUM:** The large physical size of aluminum electrolytics makes them unsuitable for most applications. Their ESR characteristics are also not well suited to the requirements of LDO regulators. The ESR of a typical aluminum electrolytic is higher than a tantalum, and it also varies greatly with temperature.

A typical aluminum electrolytic can exhibit an ESR increase of 50X when going from 20°C to -40°C. Also, some aluminum electrolytics can not be used below -25°C because the electrolyte will freeze.

## POWER-ON RESET DELAY

A power-on reset function can be easily implemented using the LP2987/8 by adding a single external capacitor to the Delay pin. The Error output provides the power-on reset signal when input power is applied to the regulator.

The reset signal stays low for a pre-set time period after power is applied to the regulator, and then goes high (see Timing Diagram below).



Figure 46. Timing Diagram for Power-Up

The external capacitor  $C_{\text{DLY}}$  sets the delay time ( $T_{\text{DELAY}}$ ). The value of capacitor required for a given time delay may be calculated using the formula:

$$C_{\text{DLY}} = T_{\text{DELAY}} / (5.59 \times 10^5)$$

To simplify design, a plot is provided below which shows values of  $C_{\text{DLY}}$  versus delay time.



Figure 47. Plot of C<sub>DLY</sub> vs T<sub>DELAY</sub>

**DETAILS OF ERR/RESET CIRCUIT OPERATION:** (Refer to LP2987/8 Equivalent Circuit).

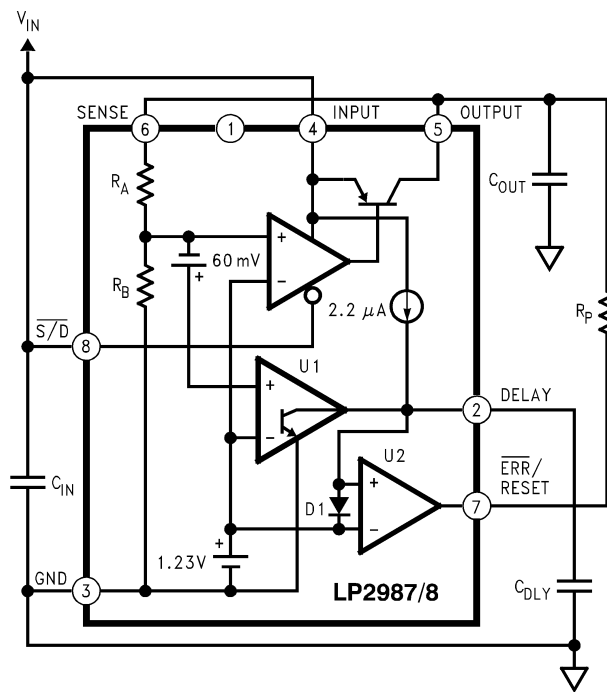


Figure 48. LP2987/8 Equivalent Circuit

The output of comparator U2 is the ERR/RESET flag. Since it is an open-collector output, it requires the use of a pull-up resistor (R<sub>P</sub>). The 1.23V reference is tied to the inverting input of U2, which means that its output is controlled by the voltage applied to the non-inverting input.

The output of U1 (also an open-collector) will force the non-inverting input of U2 to go low whenever the LP2987/8 regulated output drops about 5% below nominal.

U1's inverting input is also held at 1.23V. The other input samples the regulated output through a resistive divider (R<sub>A</sub> and R<sub>B</sub>). When the regulated output is at nominal voltage, the voltage at the divider tap point will be 1.23V. If this voltage drops about 60 mV below 1.23V, the output of U1 will go low forcing the output of U2 low (which is the ERROR state).

Power-ON reset delay occurs when a capacitor (shown as  $C_{DLY}$ ) is connected to the Delay pin. At turn-ON, this capacitor is initially fully discharged (which means the voltage at the Delay pin is 0V). The output of U1 keeps  $C_{DLY}$  fully discharged (by sinking the 2.2  $\mu$ A from the current source) until the regulator output voltage comes up to within about 5% of nominal. At this point, U1's output stops sinking current and the 2.2  $\mu$ A starts charging up  $C_{DLY}$ .

When the voltage across  $C_{DLY}$  reaches 1.23V, the output of U2 will go high (note that D1 limits the maximum voltage to about 2V).

**SELECTING  $C_{DLY}$ :** The maximum recommended value for this capacitor is 1  $\mu$ F. The capacitor must not have excessively high leakage current, since it is being charged from a 2.2  $\mu$ A current source.

Aluminum electrolytics can not be used, but good-quality tantalum, ceramic, mica, or film types will work.

## SHUTDOWN INPUT OPERATION

The LP2987/8 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to  $V_{IN}$  to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed as  $V_H$  and  $V_L$ , respectively (see [Electrical Characteristics](#)).

It is also important that the turn-on (and turn-off) voltage signals applied to the Shutdown input have a slew rate which is not less than 40 mV/ $\mu$ s.

### CAUTION

The regulator output state can not be ensured if a slow-moving AC (or DC) signal is applied that is in the range between  $V_H$  and  $V_L$ .

## REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP2987/8 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into  $V_{IN}$  (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from  $V_{IN}$  to  $V_{OUT}$  (cathode on  $V_{IN}$ , anode on  $V_{OUT}$ ), to limit the reverse voltage across the LP2987/8 to 0.3V (see [Absolute Maximum Ratings](#)).

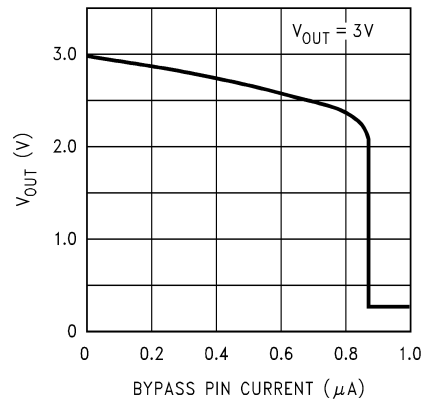
### BYPASS CAPACITOR (LP2988)

The capacitor connected to the Bypass pin must have very low leakage. The current flowing out of the Bypass pin comes from the Bandgap reference, which is used to set the output voltage. Since the Bandgap circuit has only a few microamps flowing in it, loading effects due to leakage current will cause a change in the regulated output voltage.

Curves are provided which show the effect of loading the Bypass pin on the regulated output voltage.

Care must be taken to ensure that the capacitor selected for bypass will not have significant leakage current over the operating temperature range of the application.

A high quality ceramic capacitor which uses either NPO or COG type dielectric material will typically have very low leakage. Small surface-mount polypropylene or polycarbonate film capacitors also have extremely low leakage, but are slightly larger in size than ceramics.



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## REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">18</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2987AILD-3.0/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L007A	<a href="#">Samples</a>
LP2987AILD-5.0/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L009A	<a href="#">Samples</a>
LP2987AILD-5.0/NOPB	ACTIVE	WSON	NGN	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L009A	<a href="#">Samples</a>
LP2987AIMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L44A	<a href="#">Samples</a>
LP2987AIMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987A IM5.0	<a href="#">Samples</a>
LP2987ILD-3.3/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L008A B	<a href="#">Samples</a>
LP2987IM-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0	<a href="#">Samples</a>
LP2987IM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.3	<a href="#">Samples</a>
LP2987IM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0	<a href="#">Samples</a>
LP2987IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L43B	<a href="#">Samples</a>
LP2987IMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L44B	<a href="#">Samples</a>
LP2987IMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L43B	<a href="#">Samples</a>
LP2987IMX-3.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0	<a href="#">Samples</a>
LP2987IMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0	<a href="#">Samples</a>
LP2988AIM-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2988A IM5.0	
LP2988AIM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988A IM5.0	<a href="#">Samples</a>
LP2988AIMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L49A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2988AIMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L50A	<a href="#">Samples</a>
LP2988AIMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L51A	<a href="#">Samples</a>
LP2988AIMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988A IM3.3	<a href="#">Samples</a>
LP2988ILD-3.8/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L083A B	<a href="#">Samples</a>
LP2988IM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0	<a href="#">Samples</a>
LP2988IMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L49B	<a href="#">Samples</a>
LP2988IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L50B	<a href="#">Samples</a>
LP2988IMM-5.0	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L51B	
LP2988IMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L51B	<a href="#">Samples</a>
LP2988IMMX-3.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L49B	<a href="#">Samples</a>
LP2988IMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L50B	<a href="#">Samples</a>
LP2988IMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2987AILD-3.0/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AILD-5.0/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AILD-5.0/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AIMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987AIMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2987ILD-3.3/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2987IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2988AIMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2988ILD-3.8/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2988IMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2988IMM-5.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2987AILD-3.0/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2987AILD-5.0/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2987AILDX-5.0/NOPB	WSON	NGN	8	4500	367.0	367.0	35.0
LP2987AIMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2987AIMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2987ILD-3.3/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2987IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2987IMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2987IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2987IMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2987IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2988AIMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2988AIMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988AIMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988AIMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2988ILD-3.8/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2988IMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMM-5.0	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2988IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2988IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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