



**THE DATASHEET OF  
IPD70R900P7SAUMA1**



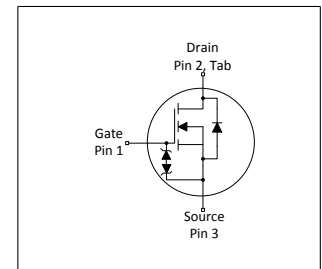
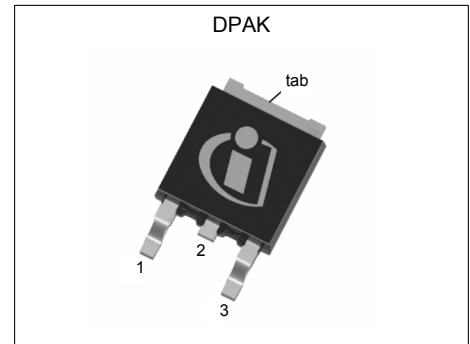
# MOSFET

## 700V CoolMOS™ P7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

The latest CoolMOS™ P7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, lighting, TV, etc.

The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- Excellent thermal behavior
- Integrated ESD protection diode
- Low switching losses ( $E_{oss}$ )
- Product validation acc. JEDEC Standard

### Benefits

- Cost competitive technology
- Lower temperature
- High ESD ruggedness
- Enables efficiency gains at higher switching frequencies
- Enables high power density designs and small form factors

### Potential applications

Recommended for Flyback topologies for example used in Chargers, Adapters, Lighting Applications, etc.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j=25^{\circ}C}$	700	V
$R_{DS(on),max}$	0.9	$\Omega$
$Q_{g,typ}$	6.8	nC
$I_{D,pulse}$	12.8	A
$E_{oss} @ 400V$	0.9	$\mu J$
$V_{(GS)th,typ}$	3	V
ESD class (HBM)	1C	

Type / Ordering Code	Package	Marking	Related Links
IPD70R900P7S	PG-TO 252-3	70S900P7	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	6.0 3.5	A	$T_C = 20^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	12.8	A	$T_C=25^\circ\text{C}$
Application (Flyback) relevant avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	-	3.6	A	measured with standard leakage inductance of transformer of $5\mu\text{H}$
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	$V_{GS}$	-16 -30	-	16 30	V	static; AC ( $f > 1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	30.5	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	4.1	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	12.8	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>4)</sup>	dv/dt	-	-	1	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Maximum diode commutation speed <sup>4)</sup>	di/dt	-	-	50	A/ $\mu\text{s}$	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{ min}$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction	$R_{thJC}$	-	-	4.1	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	$^\circ\text{C/W}$	Device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	$^\circ\text{C/W}$	Device on $40\text{mm} \times 40\text{mm} \times 1.5$ epoxy PCB FR4 with $6\text{cm}^2$ (one layer $70\mu\text{m}$ thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{solid}$	-	-	260	$^\circ\text{C}$	reflow MSL3

<sup>1)</sup> Limited by  $T_{j,max}$ .  $T_j = 20^\circ\text{C}$ . Maximum duty cycle  $D=0.5$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Proven during verification test. For explanation please read AN - CoolMOS™ 700V P7.

<sup>4)</sup>  $V_{DClink}=400\text{V}$ ;  $V_{DS,peak} < V_{(BR)DSS}$ ; identical low side and high side switch with identical  $R_G$

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.06mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=700V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=700V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current incl. Zener diode	$I_{GSS}$	-	-	1	$\mu A$	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.74	0.90	$\Omega$	$V_{GS}=10V, I_D=1.1A, T_j=25^\circ C$ $V_{GS}=10V, I_D=1.1A, T_j=150^\circ C$
Gate resistance	$R_G$	-	1.6	-	$\Omega$	$f=1\text{ MHz, open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	211	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	5	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	13	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	177	-	pF	$I_D=constant, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.9A,$ $R_G=5.3\Omega$
Rise time	$t_r$	-	4.7	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.9A,$ $R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	58	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.9A,$ $R_G=5.3\Omega$
Fall time	$t_f$	-	31	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.9A,$ $R_G=5.3\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	0.9	-	nC	$V_{DD}=400V, I_D=0.9A, V_{GS}=0\text{ to }10V$
Gate to drain charge	$Q_{gd}$	-	2.6	-	nC	$V_{DD}=400V, I_D=0.9A, V_{GS}=0\text{ to }10V$
Gate charge total	$Q_g$	-	6.8	-	nC	$V_{DD}=400V, I_D=0.9A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=400V, I_D=0.9A, V_{GS}=0\text{ to }10V$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=1.4A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	160	-	ns	$V_R=400V, I_F=0.9A, di_F/dt=50A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	0.5	-	$\mu C$	$V_R=400V, I_F=0.9A, di_F/dt=50A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	7	-	A	$V_R=400V, I_F=0.9A, di_F/dt=50A/\mu s$

## 4 Electrical characteristics diagrams

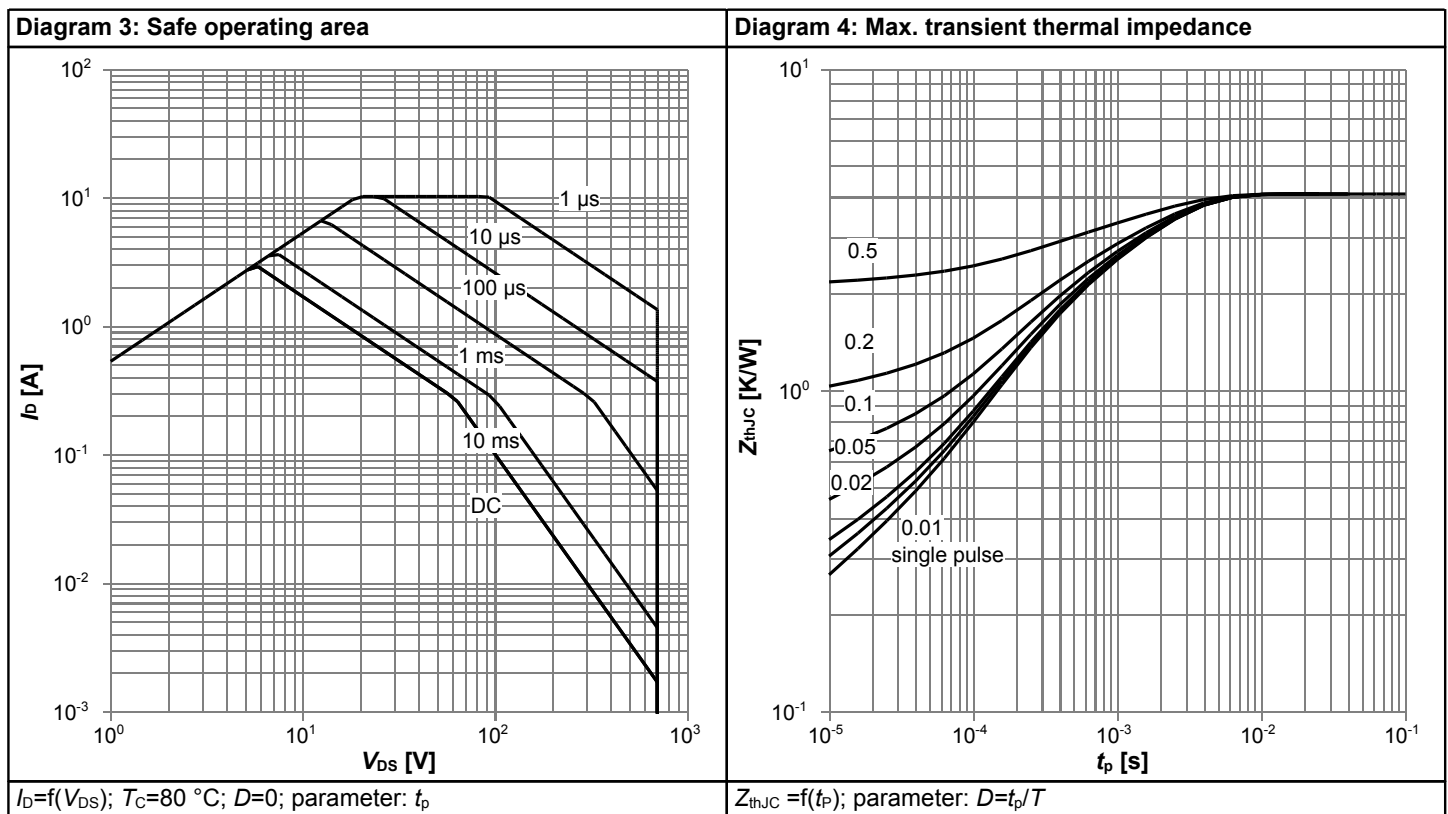
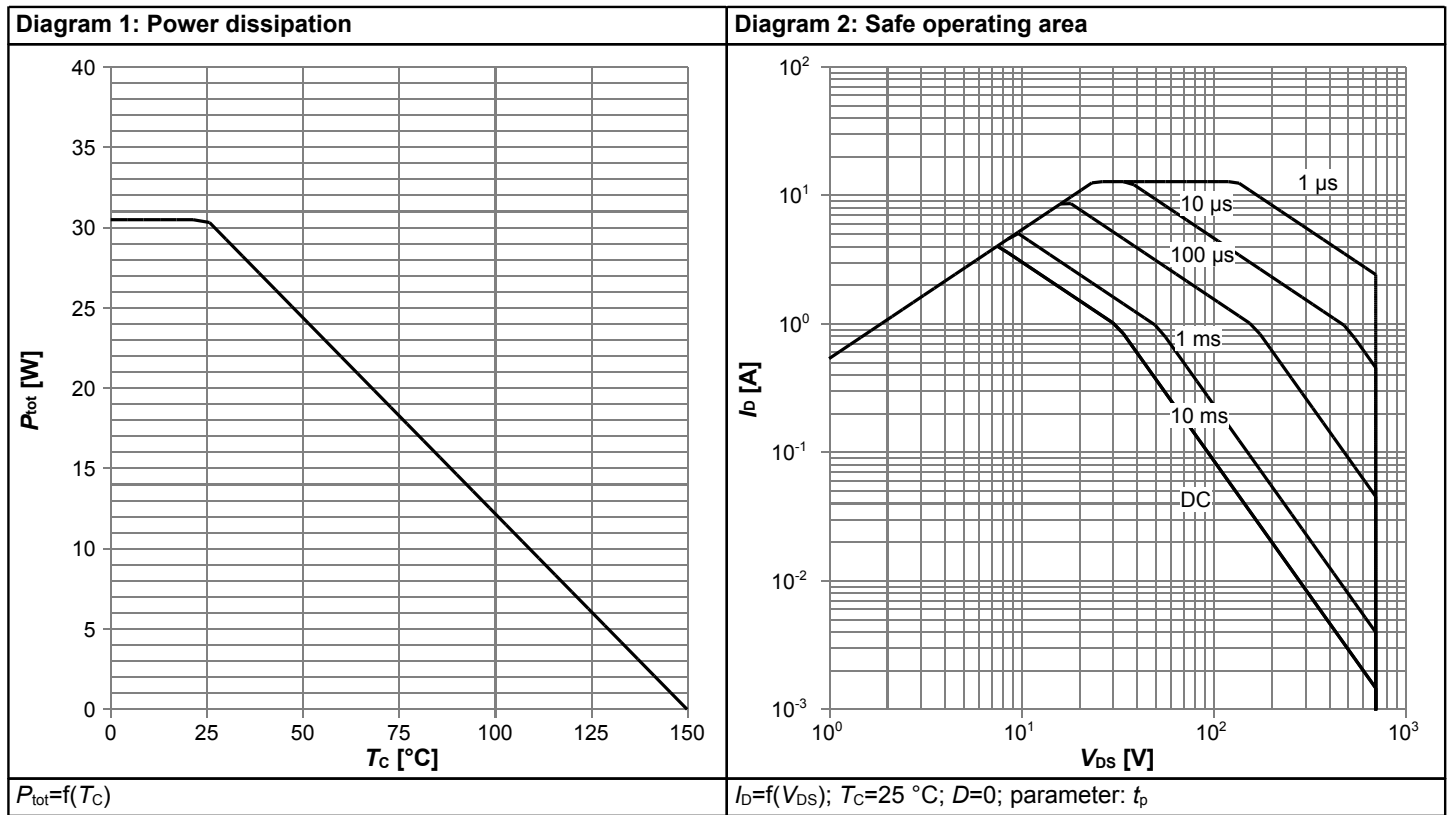
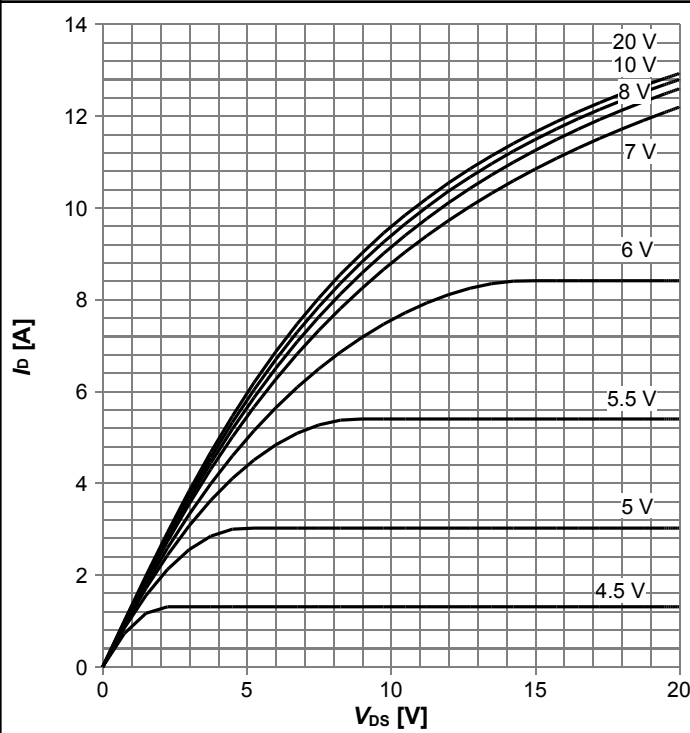
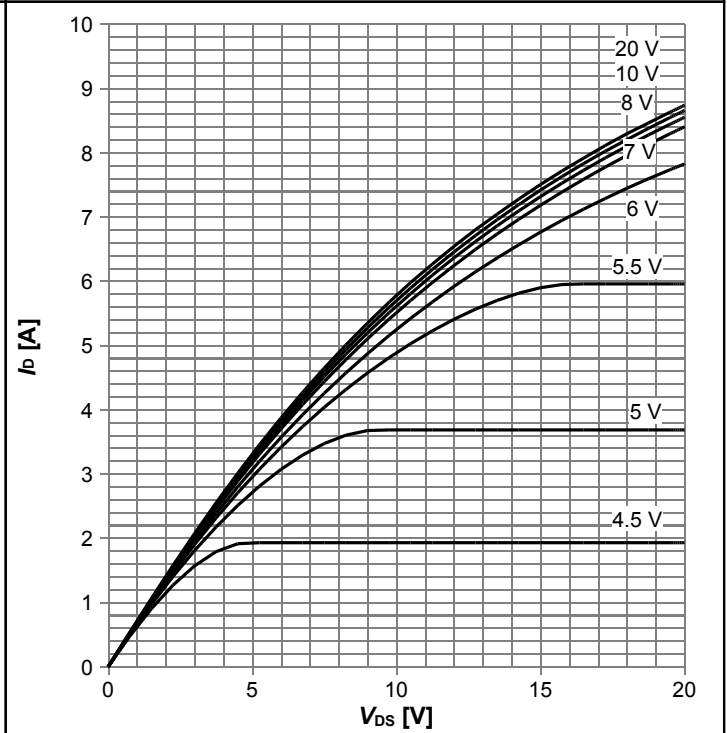


Diagram 5: Typ. output characteristics



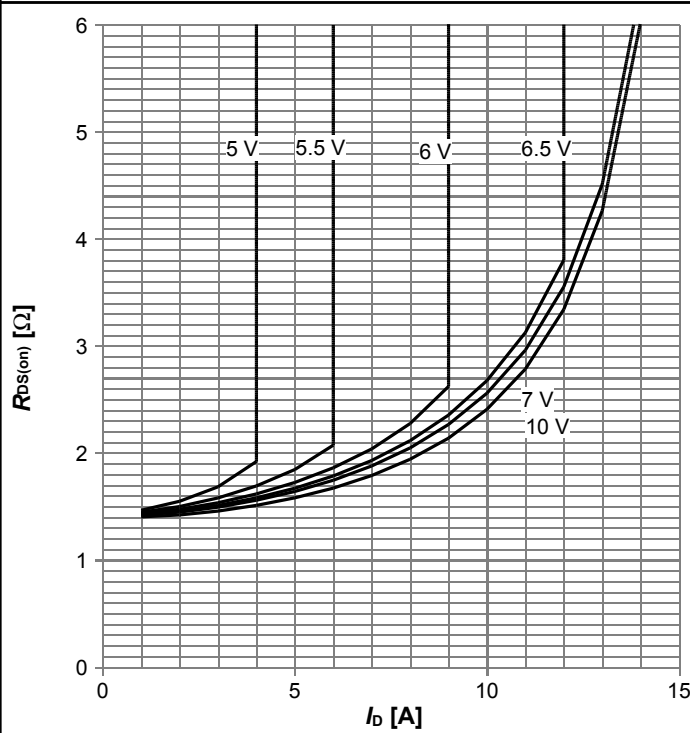
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



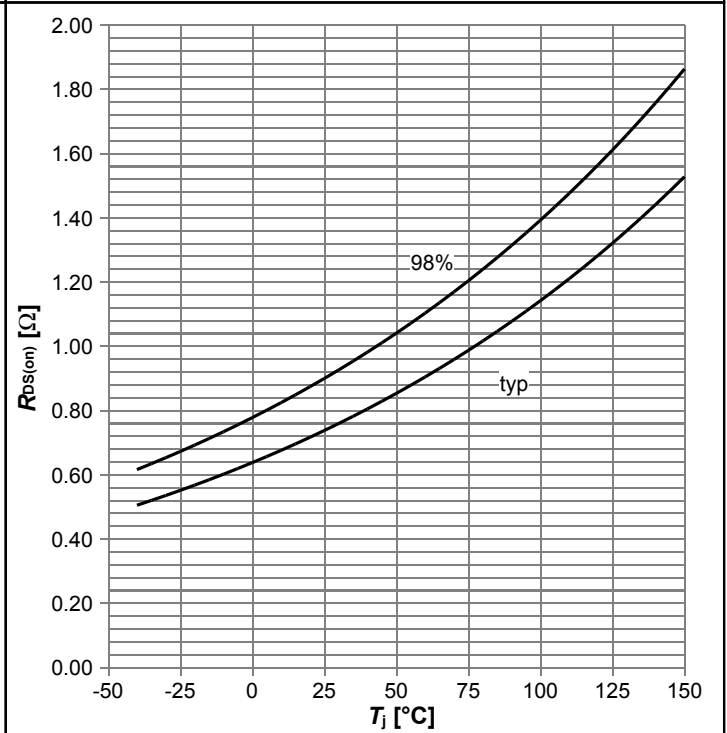
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



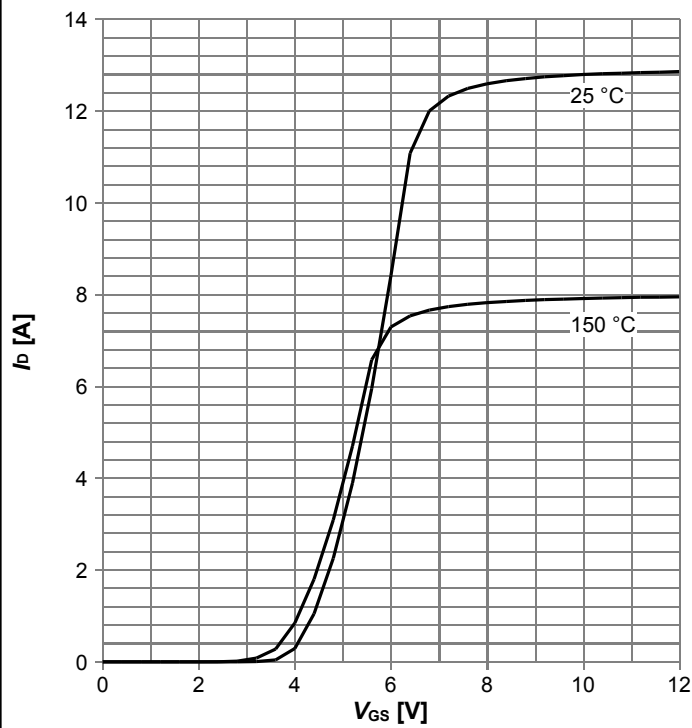
$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



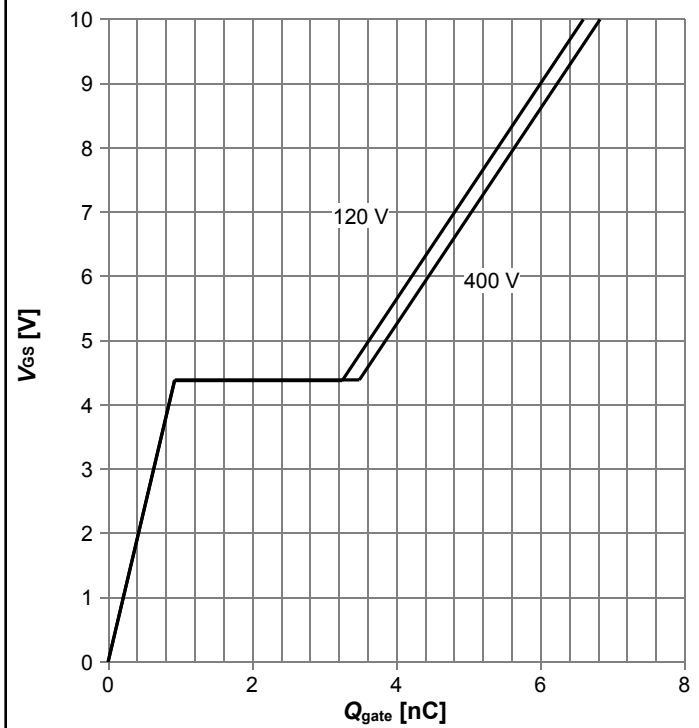
$R_{DS(on)}=f(T_j)$ ;  $I_D=1.1\text{ A}$ ;  $V_{GS}=10\text{ V}$

**Diagram 9: Typ. transfer characteristics**



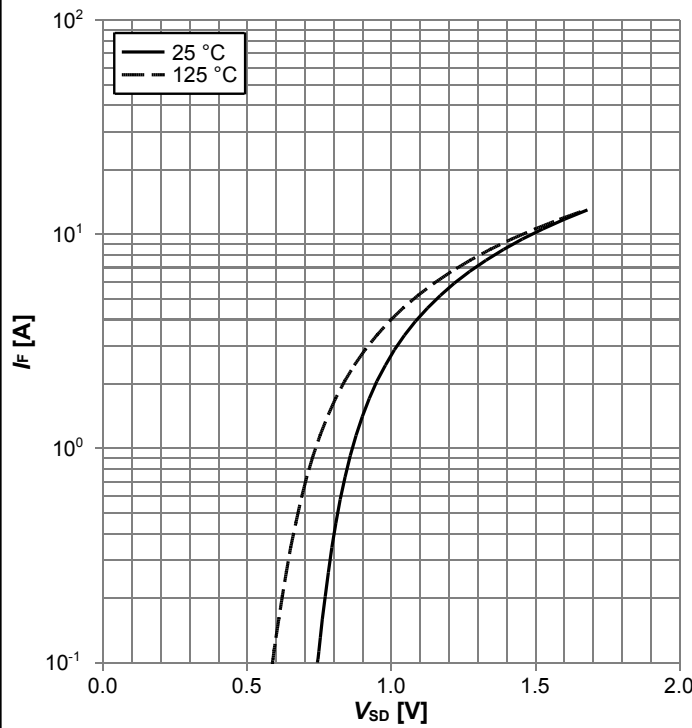
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

**Diagram 10: Typ. gate charge**



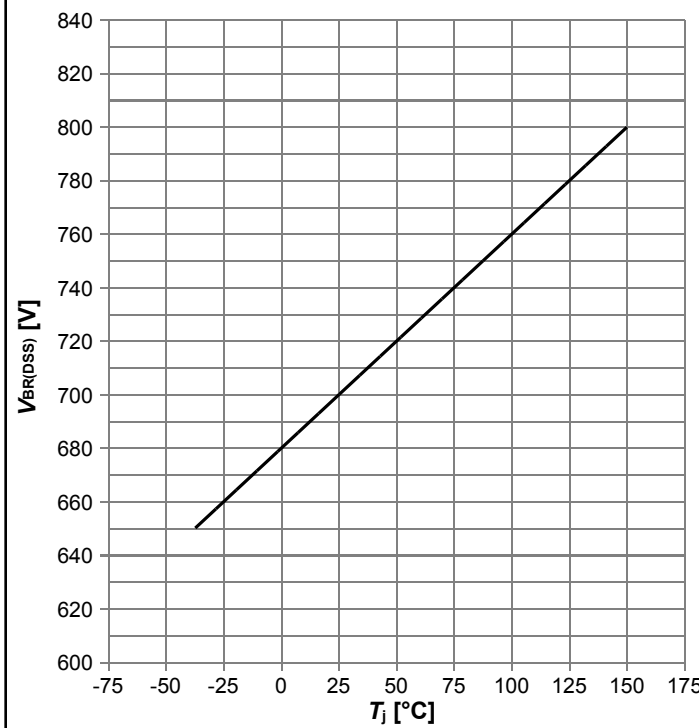
$V_{GS} = f(Q_{gate}); I_D = 0.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



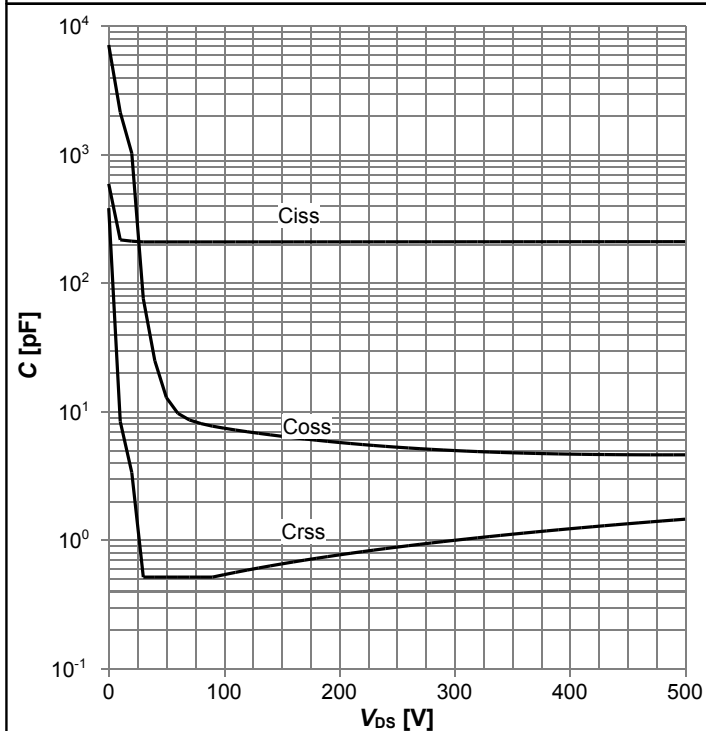
$I_F = f(V_{SD}); \text{parameter: } T_j$

**Diagram 13: Drain-source breakdown voltage**



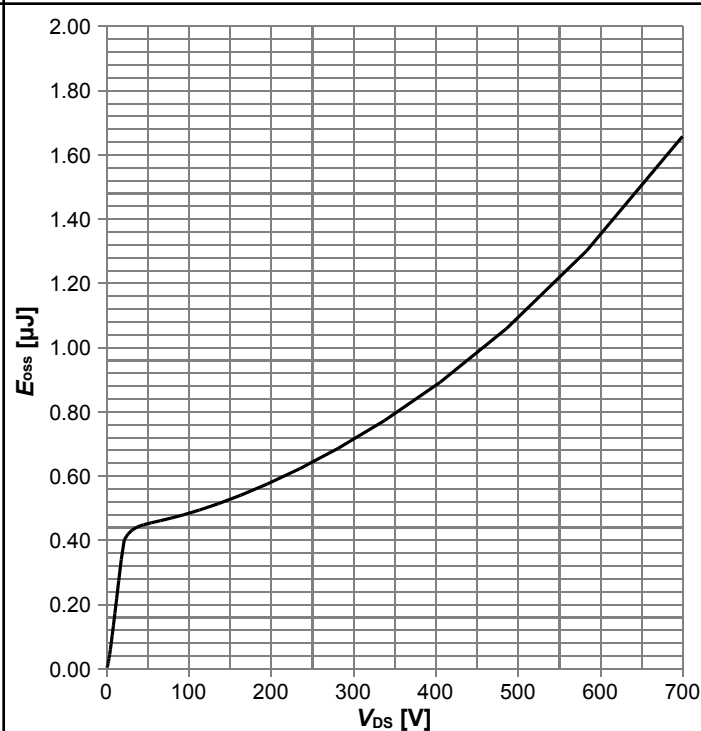
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

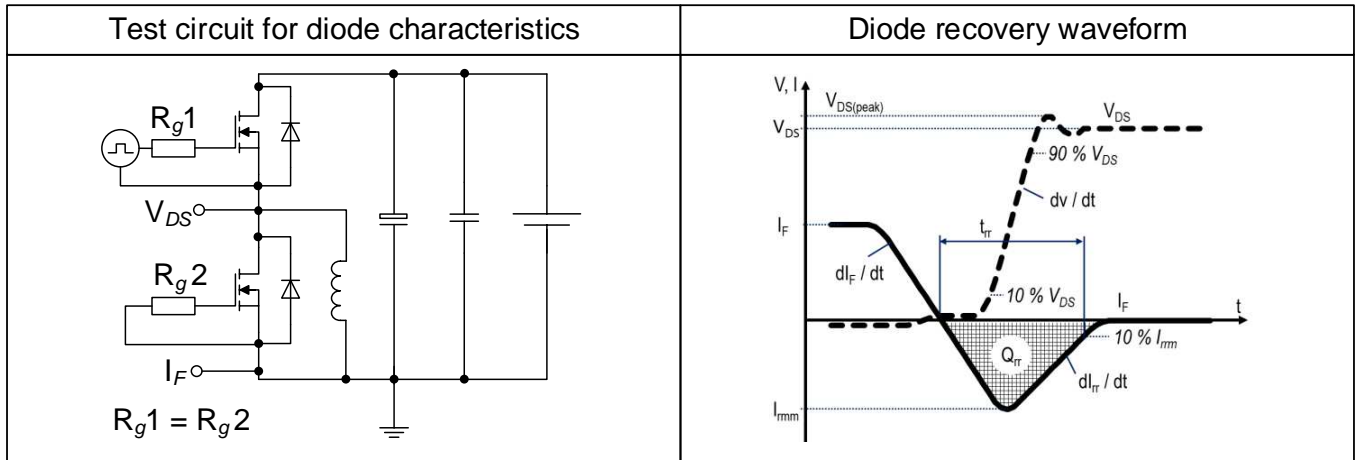
Diagram 15: Typ. Coss stored energy



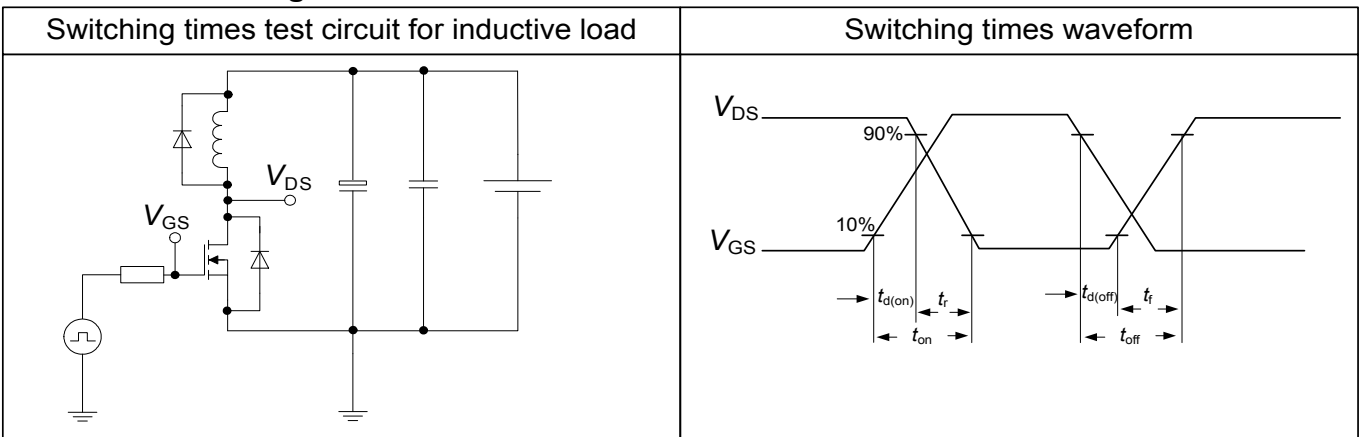
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

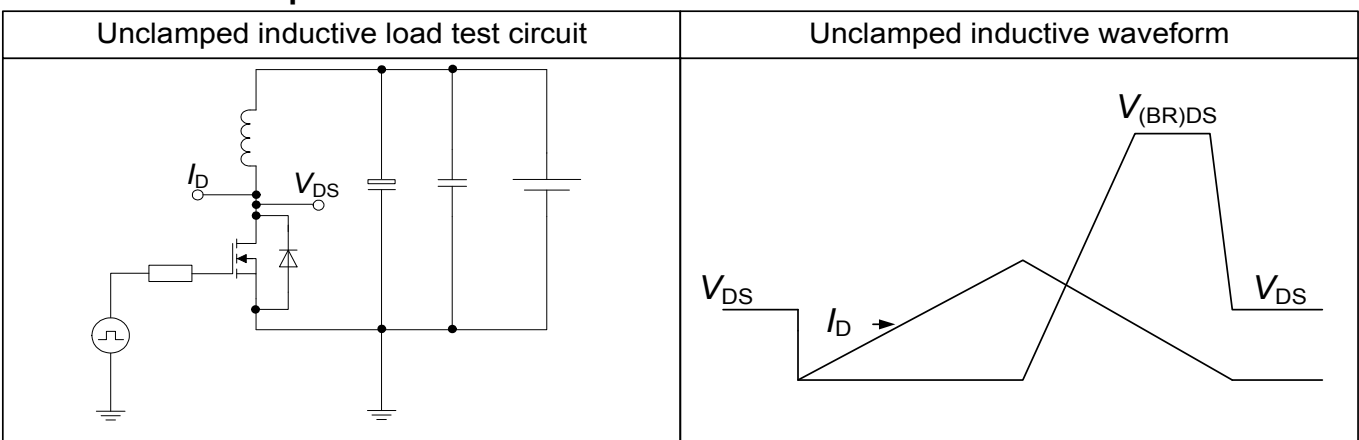
**Table 8 Diode characteristics**



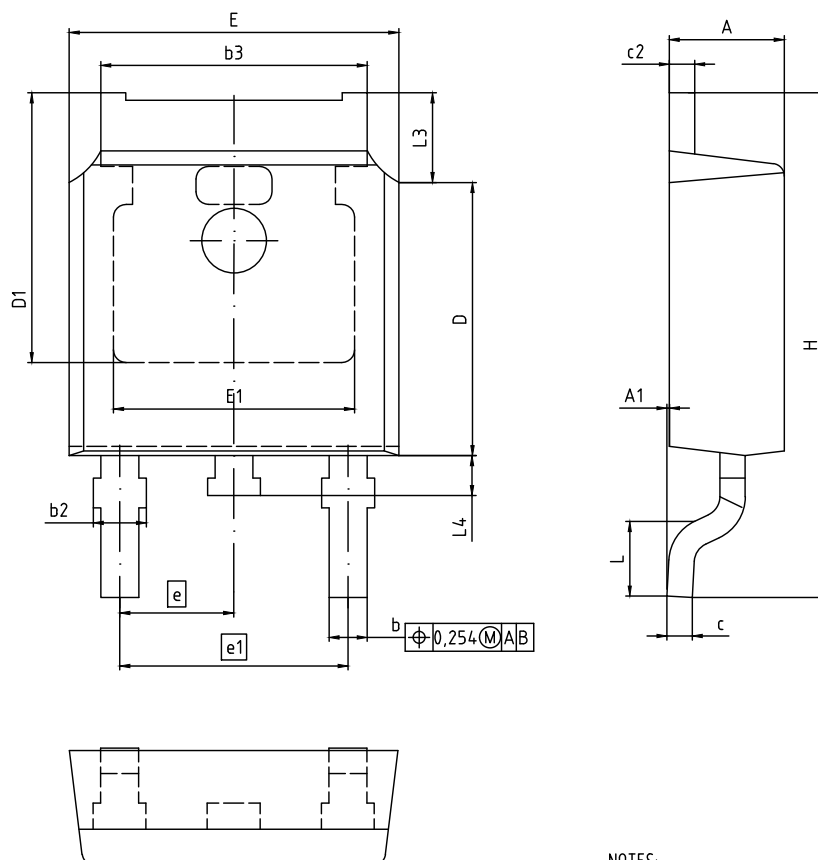
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



NOTES:

1. STANDARD QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
A1	0.00	0.15	0.000	0.006
b	0.68	0.89	0.027	0.035
b2	0.72	1.10	0.028	0.043
b3	5.13	5.50	0.202	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.60	0.018	0.024
D	5.98	6.22	0.235	0.245
D1	5.25	5.40	0.207	0.213
E	6.40	6.73	0.252	0.265
E1	4.70	5.60	0.185	0.220
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.38	1.70	0.054	0.067
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039

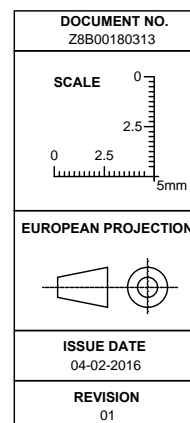


Figure 1 Outline PG-TO 252-3, dimensions in mm/inches

## **7 Appendix A**

### **Table 11 Related Links**

- IFX CoolMOS™ P7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPD70R900P7S

**Revision: 2018-02-13, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-11-24	Release of final version
2.1	2018-02-13	Corrected front page text

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