THE DATASHEET OF

AD5542ABRUZ

2.7 V to 5.5 V, Serial-Input, Voltage-Output, 12-/16-Bit DAC

Data Sheet **AD5512A/AD5542A**

FEATURES

- 12-/16-bit resolution
- 1 LSB INL
- 11.8 nV/√Hz noise spectral density
- 1 µs settling time
- 1.1 nV-sec glitch energy
- 0.05 ppm/°C temperature drift
- 5 kV HBM ESD classification
- 0.375 mW power consumption at 3 V
- 2.7 V to 5.5 V single-supply operation
- Hardware $\overline{CLR}$ and $\overline{LDAC}$ functions
- 50 MHz SPI-/QSPI-/MICROWIRE-/DSP-compatible interface
- Power-on reset clears DAC output to midscale
- Available in 3 mm × 3 mm, 10-/16-lead LFCSP and 16-lead TSSOP

APPLICATIONS

- Automatic test equipment
- Precision source-measure instruments
- Data acquisition systems
- Medical and aerospace instrumentation
- Communication equipment

FUNCTIONAL BLOCK DIAGRAM

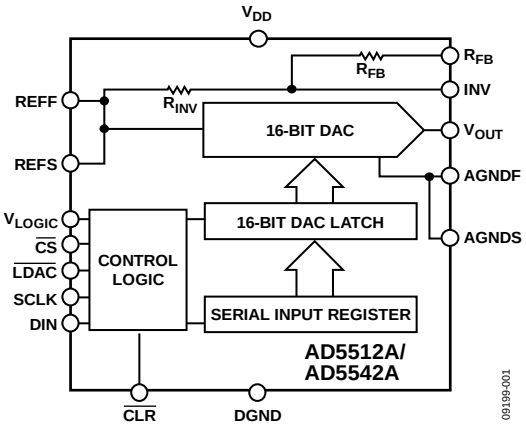

Figure 1. 16-Lead TSSOP and 16-Lead LFCSP

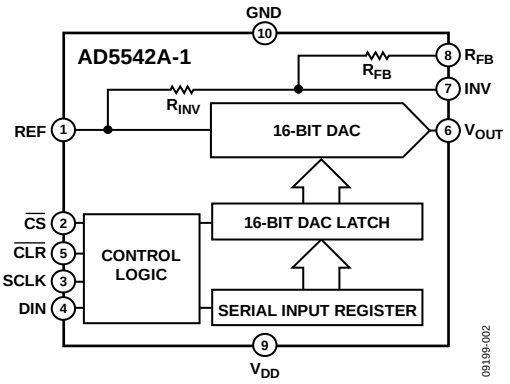

Figure 2. 10-Lead LFCSP

GENERAL DESCRIPTION

The AD5512A/AD5542A are single, 12-/16-bit, serial input, unbuffered voltage output digital-to-analog converters (DAC) that operate from a single 2.7 V to 5.5 V supply. The DAC output range extends from 0 V to V_{REF} and is guaranteed monotonic, providing 1 LSB INL accuracy at 16 bits without adjustment over the full specified temperature range of −40°C to +85°C (AD5542A) or −40°C to +125°C (AD5512A).

Offering unbuffered outputs, the AD5512A/AD5542A achieve a 1 µs settling time with low offset errors ideal for high speed open loop control.

The AD5512A/AD5542A incorporate a bipolar mode of operation that generates a $\pm V_{REF}$ output swing. The AD5512A/AD5542A also include Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity.

The AD5512A/AD5542A are available in a 16-lead LFCSP with the AD5542A also available in a 10-lead LFCSP and a 16-lead TSSOP. The AD5512A/AD5542A use a versatile 3-wire interface that is compatible with 50 MHz SPI, QSPI™, MICROWIRE™, and DSP interface standards.

Table 1. Related Devices

Part No.	Description
AD5040/AD5060	2.7 V to 5.5 V 14-/16-bit buffed output DACs
AD5541/AD5542	2.7 V to 5.5 V 16-bit voltage output DACs
AD5781/AD5791	18-/20-bit voltage output DACs
AD5570	16-bit ±12 V/±15 V bipolar output DAC
AD5024/AD5064	4.5 V to 5.5 V, 12-/16-bit quad channel DAC
AD5764	16-bit, bipolar, voltage output DAC

PRODUCT HIGHLIGHTS

1. 16-bit performance without adjustment.
2. 2.7 V to 5.5 V single supply operation.
3. Low 11.8 nV/√Hz noise spectral density.
4. Low 0.05 ppm/°C temperature drift.
5. 3 mm × 3 mm LFCSP and TSSOP packaging.

Rev. C Document Feedback

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REVISION HISTORY

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4/2015—Rev. A to Rev. B

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5/2011—Rev. 0 to Rev. A

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10/2010—Revision 0: Initial Version

SPECIFICATIONS

AD5512A

V_{DD} = 2.7 V to 5.5 V, V_{LOGIC} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, AGND = DGND = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Condition
STATIC PERFORMANCE					
Resolution	12			Bits	
Relative Accuracy (INL)		±0.5	±1.0	LSB	
Differential Nonlinearity (DNL)		±0.5	±1.0	LSB	Guaranteed monotonic
Gain Error		+0.5	±2	LSB	
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Unipolar Zero-Code Error		0.03	±0.5	LSB	
Unipolar Zero-Code Temperature Coefficient		±0.05		ppm/°C	
Bipolar Resistor Matching		1		Ω/Ω	R_{FB}/R_{INV}, typically $R_{FB} = R_{INV}$ = 28 kΩ
		±0.02	±0.08	%	Ratio error
Bipolar Zero Offset Error		±0.07	±2	LSB	
Bipolar Zero Temperature Coefficient		±0.2		ppm/°C	
Bipolar Zero-Code Offset Error		±0.02	±0.5	LSB	
Bipolar Gain Error		±0.07	±2	LSB	
Bipolar Gain Temperature Coefficient		±0.1		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF} − 1 LSB	V	Unipolar operation
	$-V_{REF}$		$+V_{REF}$ − 1 LSB	V	Bipolar operation
DAC Output Impedance		6.25		kΩ	Tolerance typically 20%
Power Supply Rejection Ratio			±1.0	LSB	ΔV_{DD} ± 10%
Output Noise Spectral Density		11.8		nV/√Hz	DAC code = 0x840 (AD5512A) or 0x8400 (AD5542A), frequency = 1 kHz, unipolar mode
Output Noise		0.134		µV p-p	0.1 Hz to 10 Hz, unipolar mode
DAC REFERENCE INPUT[2]					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance[3]	9			kΩ	Unipolar operation
	7.5			kΩ	Bipolar operation
Reference Input Capacitance		26		pF	Code 0x0000
		26		pF	Code 0x3FFF
LOGIC INPUTS					
Input Current			±1	µA	
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
Input High Voltage, V_{INH}	2.4			V	V_{DD} = 2.7 V to 5.5 V
Input Capacitance[2]			10	pF	
Hysteresis Voltage[2]		0.15		V	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All digital inputs at 0 V, V_{LOGIC}, or V_{DD}
I_{DD}		125	150	µA	$V_{IH} = V_{LOGIC}$ or V_{DD} and V_{IL} = GND
V_{LOGIC}	1.8		5.5	V	
I_{LOGIC}		15	24	µA	All digital inputs at 0 V, V_{LOGIC}, or V_{DD}
Power Dissipation		1.5	6.05	mW	

[1] Temperatures are as follows: A version −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.
[3] Reference input resistance is code-dependent, minimum at 0x855.

AD5542A

V_{DD} = 2.7 V to 5.5 V, V_{LOGIC} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, AGND = DGND = 0 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Condition
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy (INL)		±0.5	±1.0	LSB	B grade
			±2.0		A grade
Differential Nonlinearity (DNL)		±0.5	±1.0	LSB	Guaranteed monotonic
Gain Error		+0.5	±2	LSB	T_A = 25°C
			±3	LSB	
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Unipolar Zero-Code Error		0.3	±0.7	LSB	T_A = 25°C
			±1.5	LSB	
Unipolar Zero-Code Temperature Coefficient		±0.05		ppm/°C	
Bipolar Resistor Matching		1.000		Ω/Ω	R_{FB}/R_{INV}, typically $R_{FB} = R_{INV}$ = 28 kΩ
		±0.0015	±0.0076	%	Ratio error
Bipolar Zero Offset Error		±1	±5	LSB	T_A = 25°C
			±6	LSB	
Bipolar Zero Temperature Coefficient		±0.2		ppm/°C	
Bipolar Zero-Code Offset Error		±1	±5	LSB	T_A = 25°C
			±6	LSB	
Bipolar Gain Error		±1	±5	LSB	T_A = 25°C
			±6	LSB	
Bipolar Gain Temperature Coefficient		±0.1		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF} − 1 LSB	V	Unipolar operation
	$-V_{REF}$		$+V_{REF}$ − 1 LSB	V	Bipolar operation
DAC Output Impedance		6.25		kΩ	Tolerance typically 20%
Power Supply Rejection Ratio			±1.0	LSB	ΔV_{DD} ± 10%
Output Noise Spectral Density		11.8		nV/√Hz	DAC code = 0x840 (AD5512A) or 0x8400 (AD5542A), frequency = 1 kHz, unipolar mode
Output Noise		0.134		µV p-p	0.1 Hz to 10 Hz
DAC REFERENCE INPUT[2]					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance[3]	9			kΩ	Unipolar operation
	7.5			kΩ	Bipolar operation
Reference Input Capacitance		26		pF	Code 0x0000
		26		pF	Code 0xFFFF
LOGIC INPUTS					
Input Current			±1	µA	
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
Input High Voltage, V_{INH}	2.4			V	V_{DD} = 2.7 V to 5.5 V
Input Capacitance[2]			10	pF	
Hysteresis Voltage[2]		0.15		V	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All digital inputs at 0 V, V_{LOGIC}, or V_{DD}
I_{DD}		125	150	µA	$V_{IH} = V_{LOGIC}$ or V_{DD} and V_{IL} = GND
V_{LOGIC}	1.8		5.5	V	
I_{LOGIC}		15	24	µA	All digital inputs at 0 V, V_{LOGIC}, or V_{DD}
Power Dissipation		0.625	0.825	mW	

[1] For 2.7 V ≤ V_{LOGIC} ≤ 5.5 V, temperatures are as follows: A, B versions −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.
[3] Reference input resistance is code-dependent, minimum at 0x8555.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, V_{LOGIC} = 2.7 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, AGND = DGND = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Condition
Output Voltage Settling Time		1		µs	To 1/2 LSB of FS, C_L = 10 pF
Slew Rate		17		V/µs	C_L = 10 pF, measured from 0% to 63%
Digital-to-Analog Glitch Impulse		1.1		nV-sec	1 LSB change around major carry
Reference −3 dB Bandwidth		2.2		MHz	All 1s loaded
Reference Feedthrough		1		mV p-p	All 0s loaded, V_{REF} = 1 V p-p at 100 kHz
Digital Feedthrough		0.2		nV-sec	
Signal-to-Noise Ratio		92		dB	
Spurious Free Dynamic Range		80		dB	Digitally generated sine wave at 1 kHz
Total Harmonic Distortion		74		dB	DAC code = 0x3FFF (AD5512A) or 0xFFFF (AD5542A), frequency 10 kHz, V_{REF} = 2.5 V ± 1 V p-p

TIMING CHARACTERISTICS

V_{DD} = 5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, V_{INH} = 90% of V_{LOGIC}, V_{INL} = 10% of V_{LOGIC}, AGND = DGND = 0 V, unless otherwise noted.

Table 5.

Parameter[1, 2]	Limit 1.8 ≤ V_{LOGIC} ≤ 2.7 V[3]	Limit 2.7 V ≤ V_{LOGIC} ≤ 5.5 V[4]	Unit	Description
f_{SCLK}	14	50	MHz max	SCLK cycle frequency
t_1	70	20	ns min	SCLK cycle time
t_2	35	10	ns min	SCLK high time
t_3	35	10	ns min	SCLK low time
t_4	5	5	ns min	$\overline{CS}$ low to SCLK high setup
t_5	5	5	ns min	$\overline{CS}$ high to SCLK high setup
t_6	5	5	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	10	5	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	35	10	ns min	Data setup time
t_9	5	4	ns min	Data hold time (V_{INH} = 90% of V_{DD}, V_{INL} = 10% of V_{DD})
t_9	5	5	ns min	Data hold time (V_{INH} = 3 V, V_{INL} = 0 V)
t_{10}	20	20	ns min	$\overline{LDAC}$ pulsewidth
t_{11}	10	10	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup
t_{12}	15	15	ns min	$\overline{CS}$ high time between active periods
t_{13}	15	15	ns	$\overline{CLR}$ pulsewidth

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of (V_{INL} + V_{INH})/2.
[3] –40°C < T_A < +105°C.
[4] –40°C < T_A < +125°C.

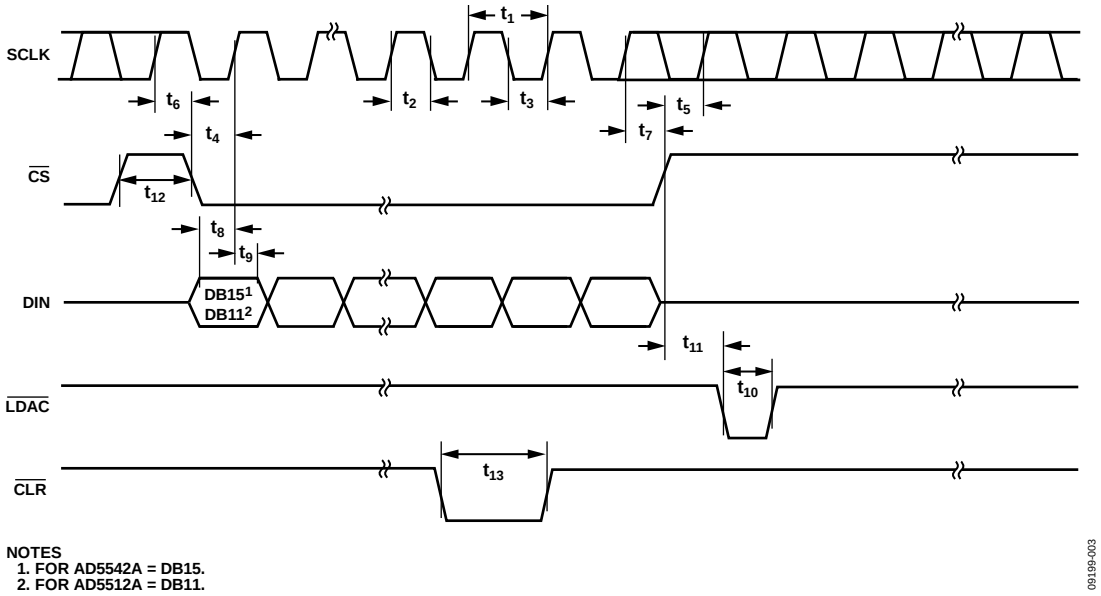


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
AGNDF, AGNDS to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range	
AD5512A Industrial (A Version)	−40°C to +125°C
AD5542A Industrial (A, B Versions)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_J max)	150°C
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Thermal Impedance, θ_{JA}	
TSSOP (RU-16)	113°C/W
LFCSP (CP-16-22)	73°C/W
LFCSP (CP-10-9)	74°C/W
Lead Temperature, Soldering	
Peak Temperature[1]	260°C
ESD[2]	5 kV

[1] As per JEDEC Standard 20.
[2] HBM classification.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

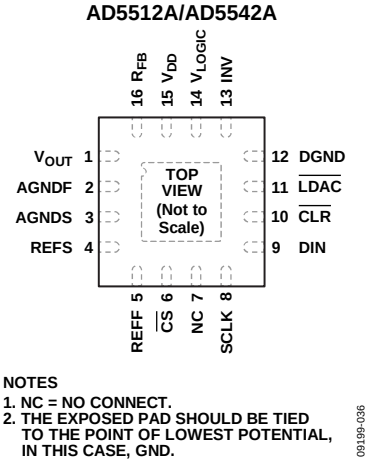


Figure 4. AD5512A/AD5542A 16-Lead LFCSP Pin Configuration

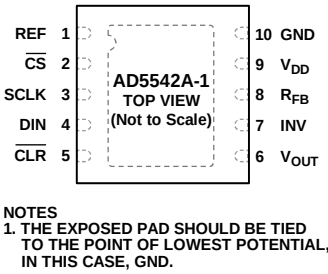


Figure 5. AD5542A-1 10-Lead LFCSP Pin Configuration

Table 7. AD5512A/AD5542A Pin Function Descriptions

Pin No.			
16-Lead LFCSP	10-Lead LFCSP	Mnemonic	Description
1	6	V_{OUT}	Analog Output Voltage from the DAC.
2		AGNDF	Ground Reference Point for Analog Circuitry (Force).
3		AGNDS	Ground Reference Point for Analog Circuitry (Sense).
4		REFS	Voltage Reference Input (Sense) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
5		REFF	Voltage Reference Input (Force) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
6	2	$\overline{CS}$	Logic Input Signal. The chip select signal is used to frame the serial data input.
7		NC	No Connect.
8	3	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
9	4	DIN	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
10	5	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the DAC register is cleared to the model selectable midscale.
11		$\overline{LDAC}$	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
12		DGND	Digital Ground. Ground reference for digital circuitry.
13	7	INV	Connection to the Internal Scaling Resistors of the DAC. Connect the INV pin to the external op amps inverting input in bipolar mode.
14		V_{LOGIC}	Logic Power Supply.
15	9	V_{DD}	Analog Supply Voltage, 5 V ± 10%.
16	8	R_{FB}	Feedback Resistor Pin. In bipolar mode, connect this pin to the external op amp output.
	1	REF	Voltage Reference Input for the DAC. Connect this pin to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
	10	GND	Ground.
EPAD	EPAD	Exposed Pad	The exposed pad should be tied to the point of lowest potential, in this case, GND.

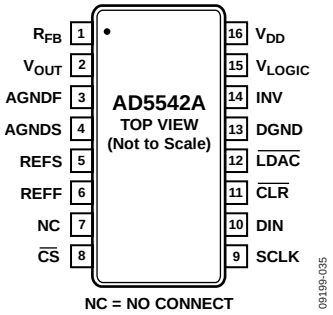


Figure 6. AD5542A 16-Lead TSSOP Pin Configuration

Table 8. AD5542A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{FB}	Feedback Resistor Pin. In bipolar mode, connect this pin to the external op amp output.
2	V_{OUT}	Analog Output Voltage from the DAC.
3	AGNDF	Ground Reference Point for Analog Circuitry (Force).
4	AGNDS	Ground Reference Point for Analog Circuitry (Sense).
5	REFS	Voltage Reference Input (Sense) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
6	REFF	Voltage Reference Input (Force) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
7	NC	No Connect.
8	$\overline{CS}$	Logic Input Signal. The chip select signal is used to frame the serial data input.
9	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
10	DIN	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
11	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the DAC register is cleared to the model selectable midscale.
12	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
13	DGND	Digital Ground. Ground reference for digital circuitry.
14	INV	Connection to the Internal Scaling Resistors of the DAC. Connect the INV pin to the external op amps inverting input in bipolar mode.
15	V_{LOGIC}	Logic Power Supply.
16	V_{DD}	Analog Supply Voltage, 5 V ± 10%.

TYPICAL PERFORMANCE CHARACTERISTICS

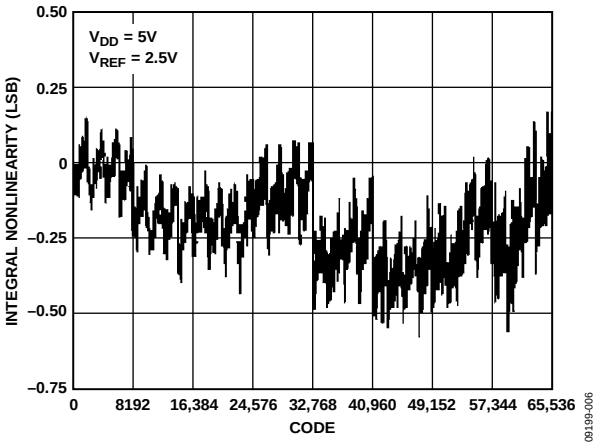


Figure 7. AD5542A Integral Nonlinearity vs. Code

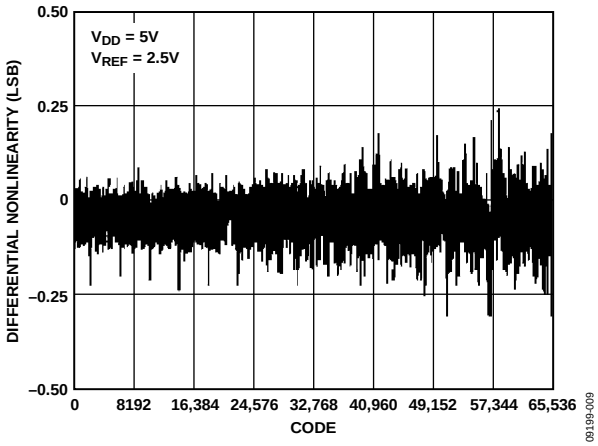


Figure 10. AD5542A Differential Nonlinearity vs. Code

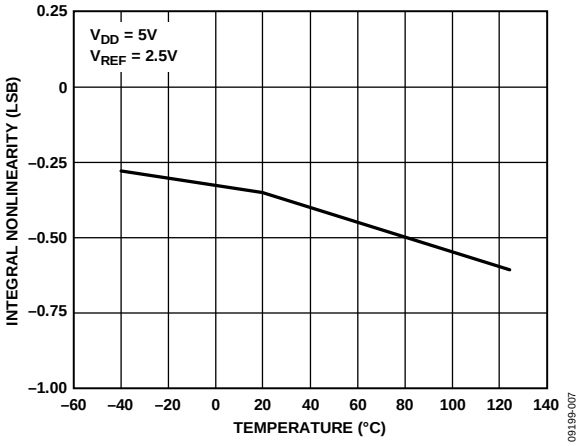


Figure 8. AD5542A Integral Nonlinearity vs. Temperature

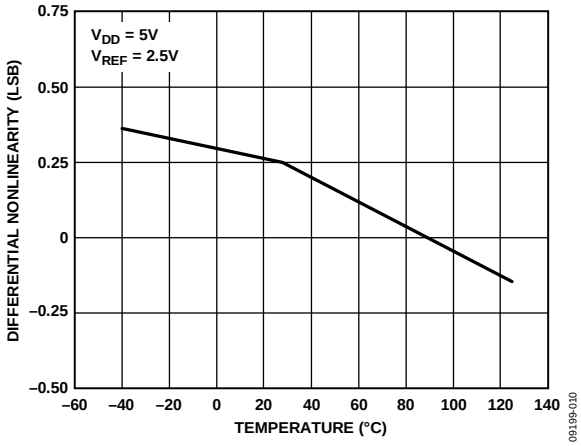


Figure 11. AD5542A Differential Nonlinearity vs. Temperature

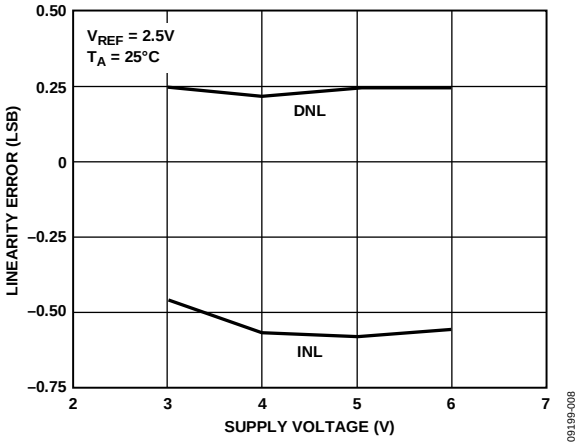


Figure 9. AD5542A Linearity Error vs. Supply Voltage

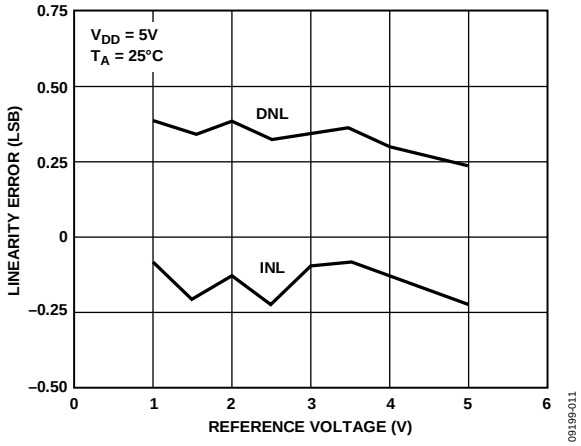


Figure 12. AD5542A Linearity Error vs. Reference Voltage

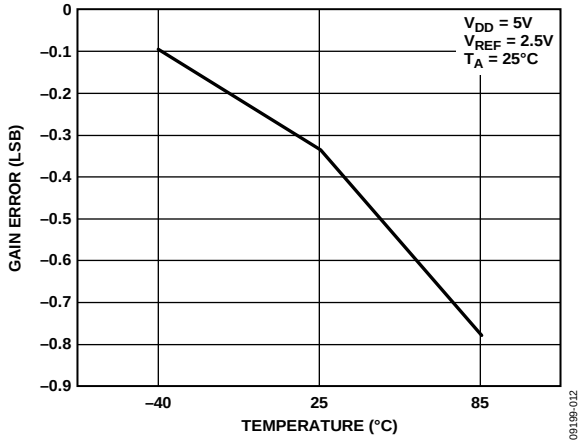


Figure 13. AD5512A/AD5542A Gain Error vs. Temperature

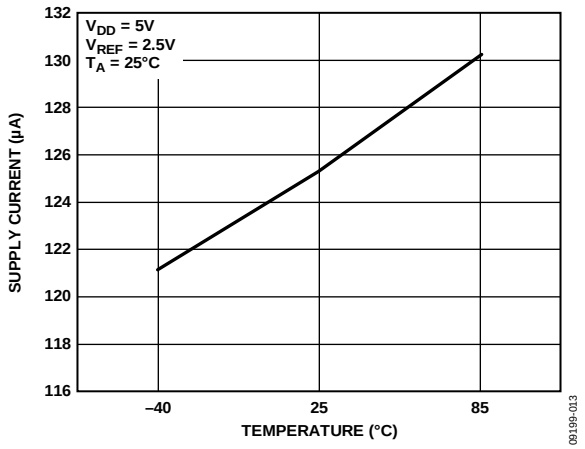


Figure 14. AD5512A/AD5542A Supply Current vs. Temperature

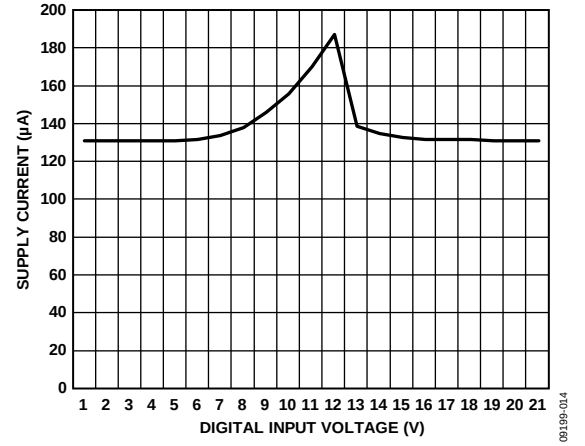


Figure 15. AD5512A/AD5542A Supply Current vs. Digital Input Voltage

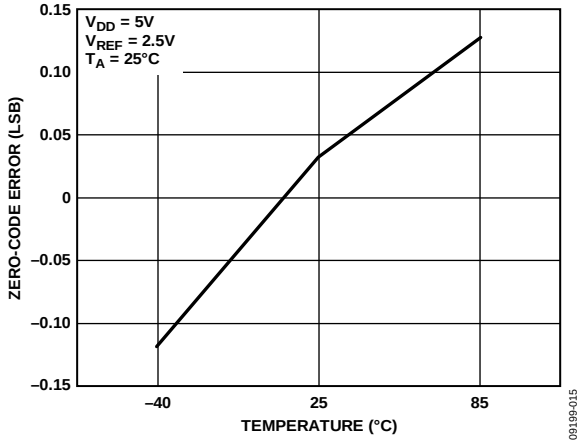


Figure 16. AD5512A/AD5542A Zero-Code Error vs. Temperature

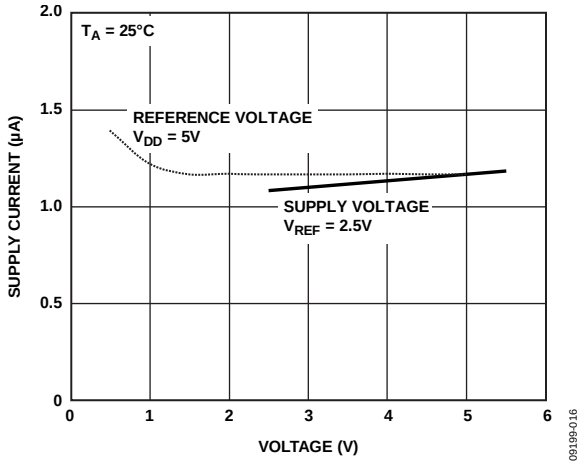


Figure 17. AD5512A/AD5542A Supply Current vs. Reference Voltage or Supply Voltage

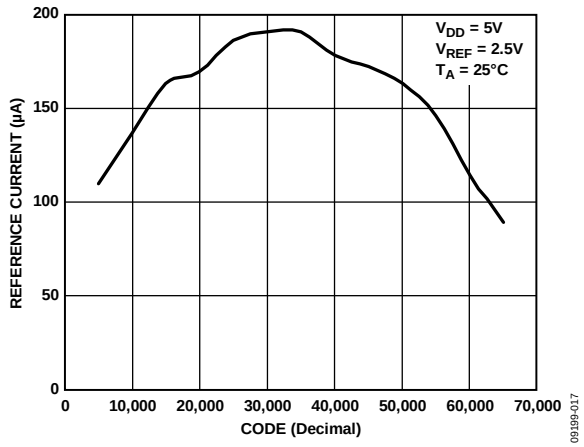


Figure 18. AD5512A/AD5542A Reference Current vs. Code

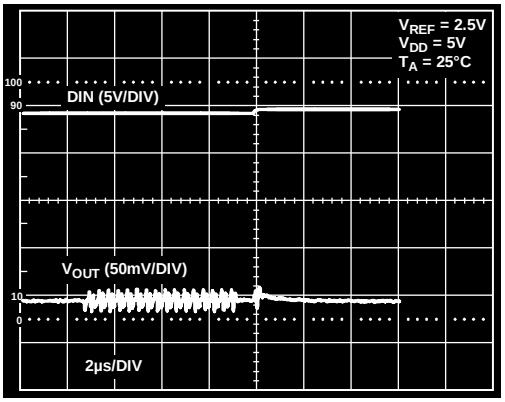


Figure 19. AD5512A/AD5542A Digital Feedthrough

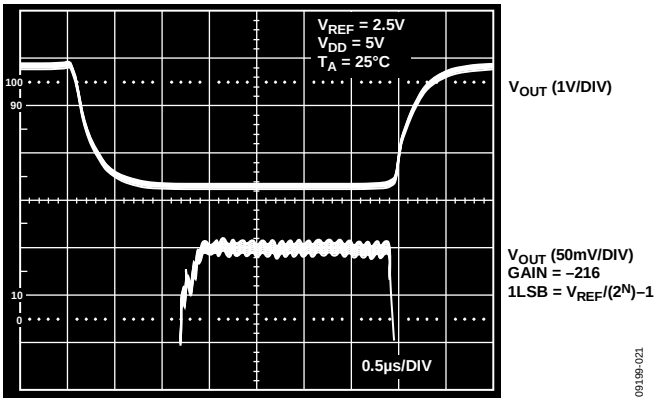


Figure 22. AD5512A/AD5542A Small Signal Settling Time

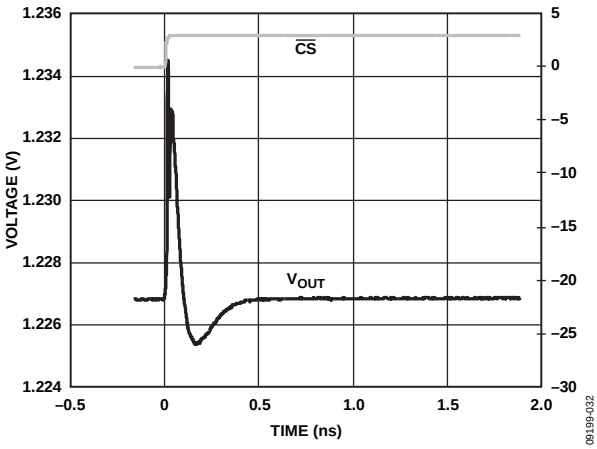


Figure 20. AD5512A/AD5542A Digital-to-Analog Glitch Impulse

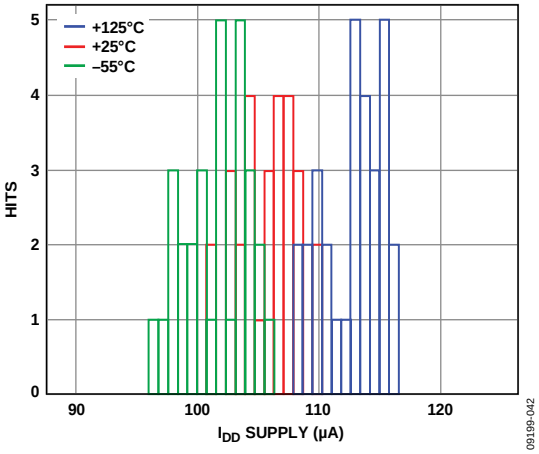


Figure 23. AD5512A/AD5542A Analog Supply Current Histogram

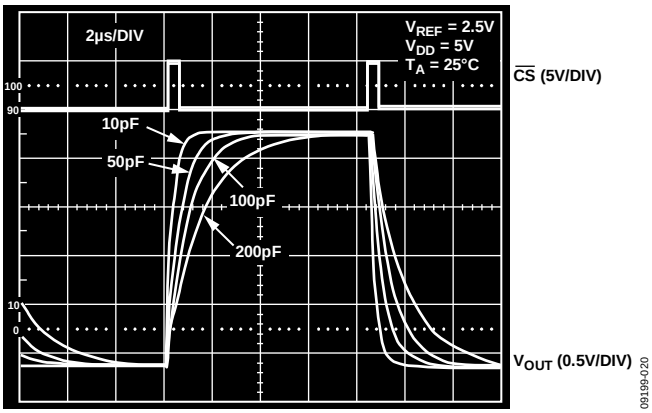


Figure 21. AD5512A/AD5542A Large Signal Settling Time

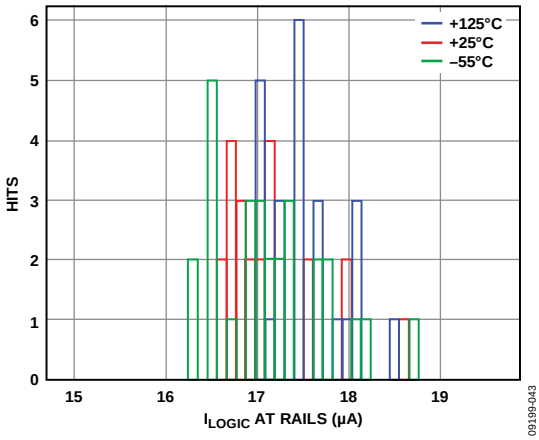


Figure 24. AD5512A/AD5542A Digital Supply Current Histogram

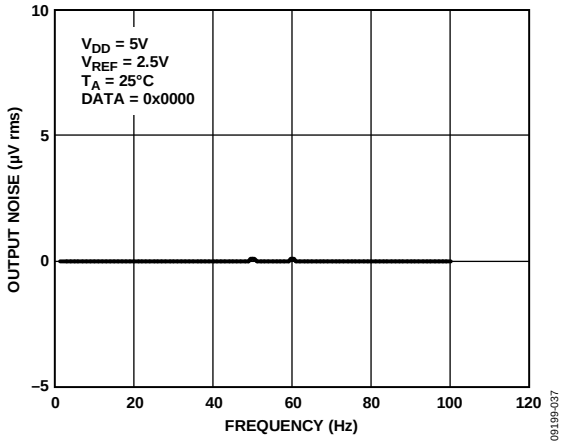


Figure 25. AD5512A/AD5542A 0.1 Hz to 10 Hz Output Noise

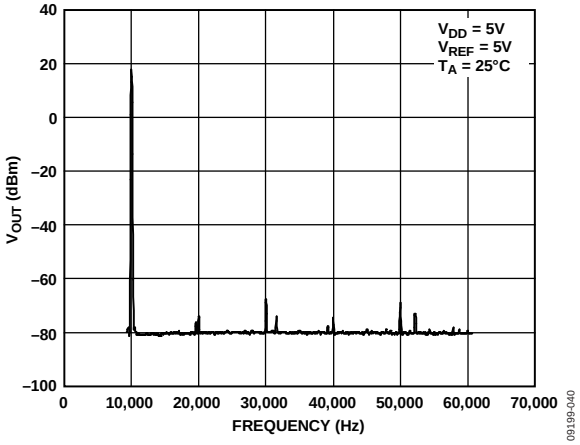


Figure 28. AD5512A/AD5542A Total Harmonic Distortion

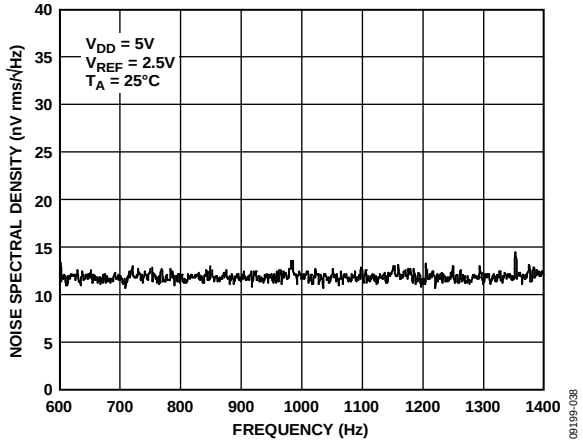


Figure 26. AD5512A/AD5542A Noise Spectral Density vs. Frequency,1 kHz

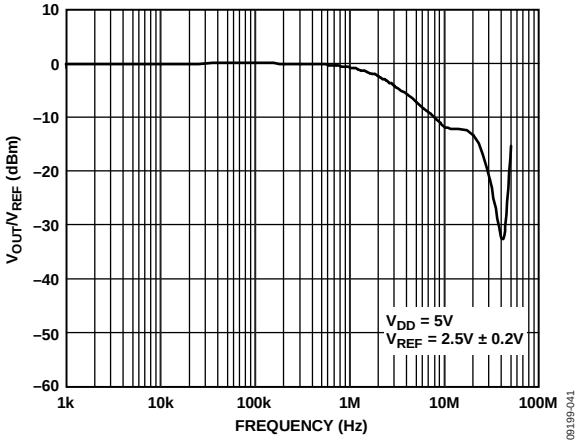


Figure 29. AD5512A/AD5542A Multiplying Bandwidth

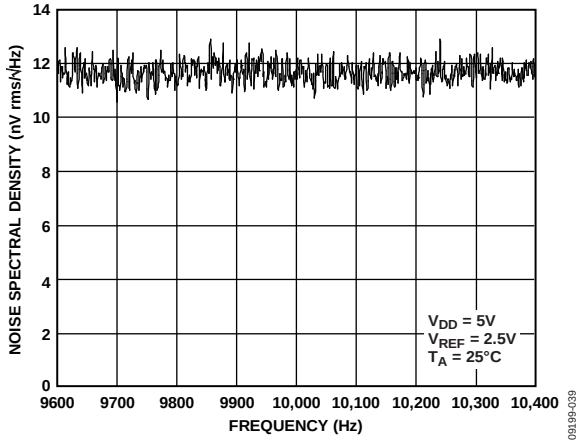


Figure 27. AD5512A/AD5542A Noise Spectral Density vs. Frequency, 10 kHz

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 7.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. A typical DNL vs. code plot is shown in Figure 10.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero-Code Error
Zero-code error is a measure of the output error when zero code is loaded to the DAC register.

Zero-Code Temperature Coefficient
This is a measure of the change in zero-code error with a change in temperature. It is expressed in mV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition. A digital-to-analog glitch impulse plot is shown in Figure 20.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. $\overline{CS}$ is held high while the SCLK and DIN signals are toggled. It is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa. A typical digital feedthrough plot is shown in Figure 19.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage. The power supply rejection ratio is quoted in terms of percent change in output per percent change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
Reference feedthrough is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

THEORY OF OPERATION

The AD5512A/AD5542A are single, 12-/16-bit, serial input, voltage output DACs. They operate from a single supply ranging from 2.7 V to 5 V and consume typically 125 µA with a supply of 5 V. Data is written to these devices in a 12-bit (AD5512A) or 16-bit (AD5542A) word format, via a 3- or 4-wire serial interface. To ensure a known power-up state, these parts are designed with a power-on reset function. In unipolar mode, the output is reset to midscale; in bipolar mode, the output is set to 0 V. Kelvin sense connections for the reference and analog ground are included on the AD5512A/AD5542A.

DIGITAL-TO-ANALOG SECTION

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 30. The DAC architecture of the AD5512A/AD5542A is segmented. The four MSBs of the 16-bit (AD5542A)/12-bit (AD5512A) data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data-word drive the S0 to S11 switches of a 12-bit voltage mode R-2R ladder network.

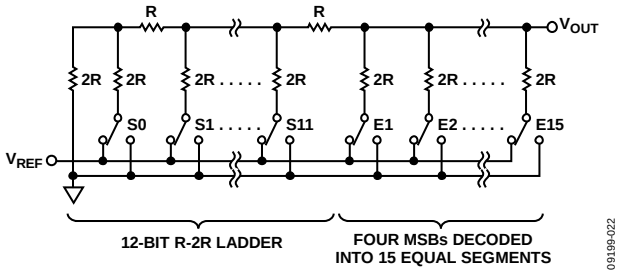


Figure 30. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal data-word loaded to the DAC register.
N is the resolution of the DAC.

For a reference of 2.5 V, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 \times D}{65{,}536}$$

This gives a V_{OUT} of 1.25 V with midscale loaded, and 2.5 V with full scale loaded to the DAC.

The LSB size is V_{REF}/65,536.

SERIAL INTERFACE

The AD5512A/AD5542A are controlled by a versatile 3- or 4-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram is shown in Figure 3. Input data is framed by the chip select input, $\overline{CS}$. After a high-to-low transition on $\overline{CS}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 12-bit (AD5512A) or 16-bit (AD5542A) words. After 12 (AD5512A) or 16 (AD5542A) data bits have been loaded into the serial input register, a low-to-high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC. Data can be loaded to the part only while $\overline{CS}$ is low.

The AD5512A/AD5542A have an $\overline{LDAC}$ function that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be maintained high while data is written to the shift register. Alternatively, $\overline{LDAC}$ can be tied permanently low to update the DAC synchronously. With $\overline{LDAC}$ tied permanently low, the rising edge of $\overline{CS}$ loads the data to the DAC.

UNIPOLAR OUTPUT OPERATION

These DACs are capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current, typically 300 µA, and a low offset error. The AD5512A/AD5542A provide a unipolar output swing ranging from 0 V to V_{REF}. The AD5512A/AD5542A can be configured to output both unipolar and bipolar voltages. Figure 31 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 9.

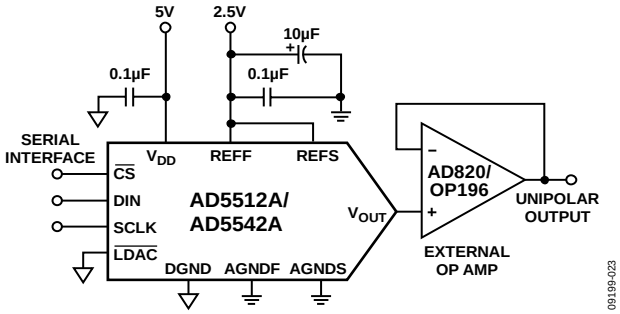


Figure 31. Unipolar Output

Table 9. AD5542A Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$V_{REF} \times (65{,}535/65{,}536)$
1000 0000 0000 0000	$V_{REF} \times (32{,}768/65{,}536) = ½\ V_{REF}$
0000 0000 0000 0001	$V_{REF} \times (1/65{,}536)$
0000 0000 0000 0000	0 V

Assuming a perfect reference, the unipolar worst-case output voltage can be calculated from the following equation:

$$V_{OUT-UNI} = \frac{D}{2^N} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

where:
$V_{OUT-UNI}$ is the unipolar mode worst-case output.
D is the code loaded to DAC.
N is the resolution of the DAC.
V_{REF} is the reference voltage applied to the part.
V_{GE} is the gain error in volts.
V_{ZSE} is the zero-scale error in volts.
INL is the integral nonlinearity in volts.

BIPOLAR OUTPUT OPERATION

With the aid of an external op amp, the AD5512A/AD5542A can be configured to provide a bipolar voltage output. A typical circuit is shown in Figure 32. The matched bipolar offset resistors, R_{FB} and R_{INV}, are connected to an external op amp to achieve this bipolar output swing, typically $R_{FB} = R_{INV} = 28\ k\Omega$. Table 10 shows the transfer function for this output operating mode. Also provided on the AD5542A are a set of Kelvin connections to the analog ground inputs. The example includes the ADR421 2.5 V reference and the AD8628 low offset and zero-drift reference buffer.

Table 10. AD5542A Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$+V_{REF} \times (32{,}767/32{,}768)$
1000 0000 0000 0001	$+V_{REF} \times (1/32{,}768)$
1000 0000 0000 0000	0 V
0111 1111 1111 1111	$-V_{REF} \times (1/32{,}768)$
0000 0000 0000 0000	$-V_{REF} \times (32{,}768/32{,}768) = -V_{REF}$

Assuming a perfect reference, the worst-case bipolar output voltage can be calculated from the following equation:

$$V_{OUT-BIP} = \frac{[(V_{OUT-UNI} + V_{OS})(2 + RD) - V_{REF}(1 + RD)]}{\frac{1 + (2 + RD)}{A}}$$

where:
$V_{OUT-BIP}$ is the bipolar mode worst-case output
$V_{OUT-UNI}$ is the unipolar mode worst-case output.
V_{OS} is the external op amp input offset voltage.
RD is the R_{FB} and R_{INV} resistor matching error.
A is the op amp open-loop gain.

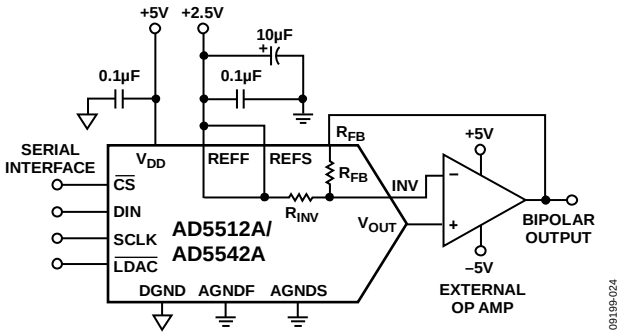


Figure 32. Bipolar Output

OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used and supplied from a dual power supply. This provides the $\pm V_{REF}$ output. In a single-supply application, selection of a suitable op amp may be more difficult because the output swing of the amplifier does not usually include the negative rail, in this case, AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp must have a very low-offset voltage (the DAC LSB is 38 μV for the AD5542A with a 2.5 V reference) to eliminate the need for output offset trims. Input bias current should also be very low because the bias current, multiplied by the DAC output impedance (approximately 6 kΩ), adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

FORCE SENSE AMPLIFIER SELECTION

Use single-supply, low-noise amplifiers. A low-output impedance at high frequencies is preferred because the amplifiers must be able to handle dynamic currents of up to ±20 mA.

REFERENCE AND GROUND

Because the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The AD5512A/AD5542A operate with a voltage reference ranging from 2 V to V_{DD}. References below 2 V result in reduced accuracy. The full-scale output voltage of the DAC is determined by the reference. Table 9 and Table 10 outline the analog output voltage or particular digital codes. For optimum performance, Kelvin sense connections are provided on the AD5512A/AD5542A.

If the application doesn't require separate force and sense lines, tie the lines close to the package to minimize voltage drops between the package leads and the internal die.

POWER-ON RESET

The AD5512A/AD5542A have a power-on reset function to ensure that the output is at a known state on power-up. On power-up, the DAC register MSB is 1 and all other bits are 0 until the data is loaded from the serial register. However, the serial register is not cleared on power-up; therefore, its contents are undefined. When loading data initially to the DAC, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept, and if less than 16 bits are loaded, bits remain from the previous word. If the AD5512A/AD5542A must be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5512A/AD5542A is via a serial bus that uses standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3- or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5512A/AD5542A require a 16-bit data-word with data valid on the rising edge of SCLK. The DAC update can be done automatically when all the data is clocked in, or it can be done under the control of the $\overline{\text{LDAC}}$.

AD5512A/AD5542A TO ADSP-BF531 INTERFACE

The SPI interface of the AD5512A/AD5542A is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 33 shows how the AD5512A/AD5542A can be connected to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5512A/AD5542A.

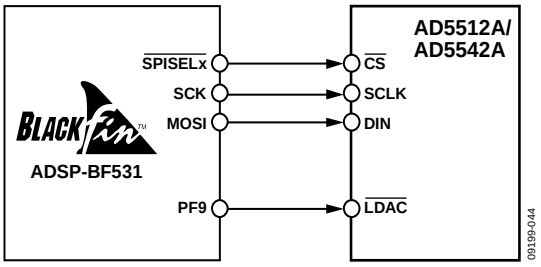


Figure 33. AD5512A/AD5542A to ADSP-BF531 Interface

AD5512A/AD5542A TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT serial port. Figure 34 shows how one SPORT interface can be used to control the AD5512A/AD5542A.

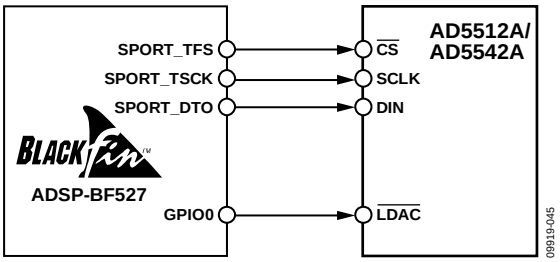
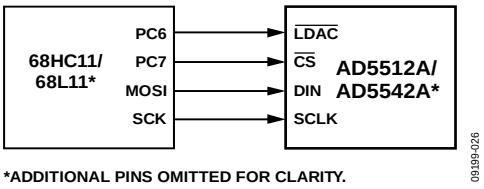


Figure 34. AD5512A/AD5542A to ADSP-BF527 Interface

AD5512A/AD5542A TO 68HC11/68L11 INTERFACE

Figure 35 shows a serial interface between the AD5512A/AD5542A and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the DAC, and the MOSI output drives the serial data line serial DIN. The $\overline{\text{CS}}$ signal is driven from one of the port lines. The 68HC11/68L11 is configured for master mode: MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

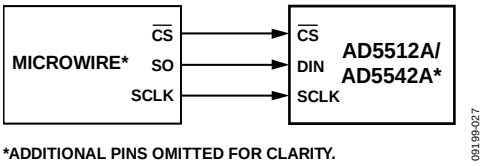


*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 35. AD5512A/AD5542A to 68HC11/68L11 Interface

AD5512A/AD5542A TO MICROWIRE INTERFACE

Figure 36 shows an interface between the AD5512A/AD5542A and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the AD5512A/AD5542A on the rising edge of the serial clock. No glue logic is required because the DAC clocks data into the input shift register on the rising edge.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 36. AD5512A/AD5542A to MICROWIRE Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the AD5512A/AD5542A is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5512A/AD5542A are in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

The AD5512A/AD5542A should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5512A/AD5542A makes the parts ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 37 shows a 4-channel isolated interface to the AD5512A/AD5542A using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

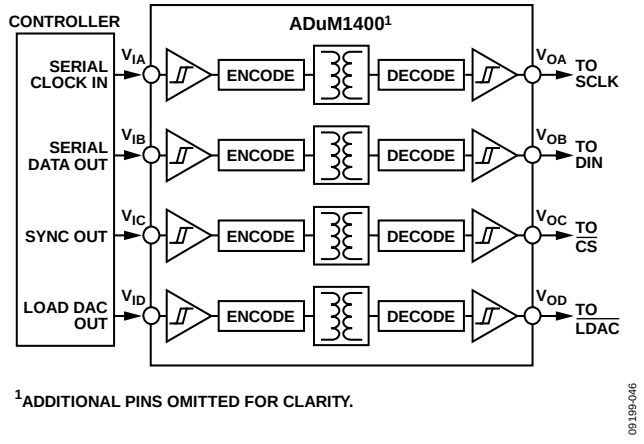


Figure 37. Isolated Interface

DECODING MULTIPLE DACS

The $\overline{CS}$ pin of the AD5512A/AD5542A can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device receives the $\overline{CS}$ signal at any one time. The DAC addressed is determined by the decoder. There is some digital feedthrough from the digital input lines. Using a burst clock minimizes the effects of digital feedthrough on the analog signal channels. Figure 38 shows a typical circuit.

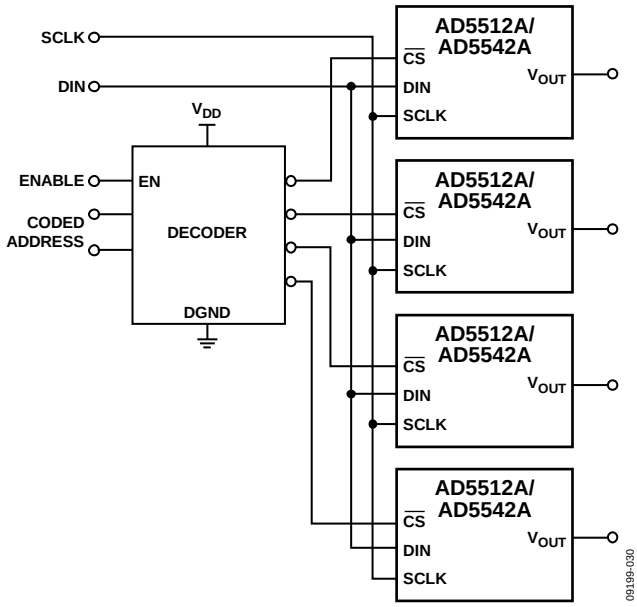


Figure 38. Addressing Multiple DACs

OUTLINE DIMENSIONS

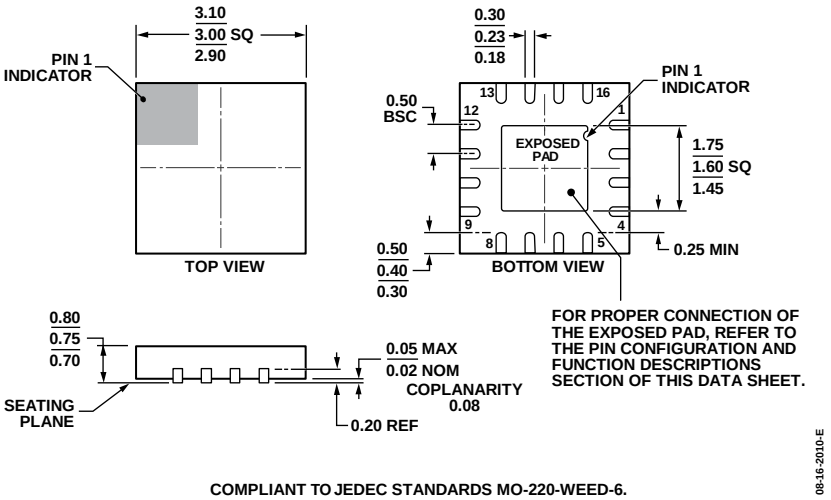


Figure 39. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

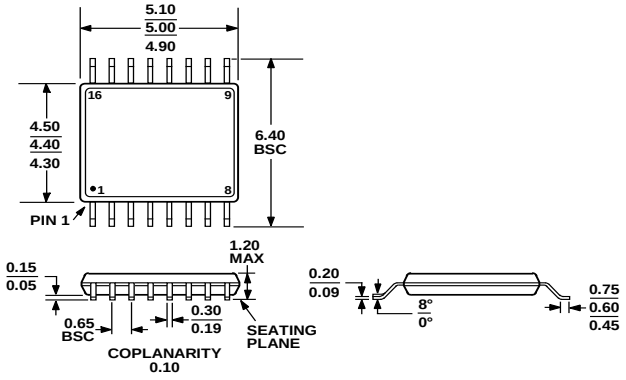


Figure 40. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

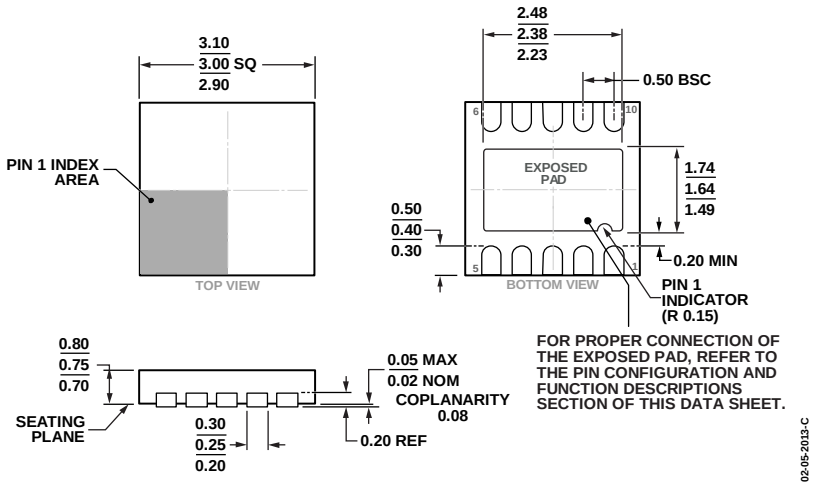


Figure 41. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	INL	DNL	Power On Reset to Code	Temperature Range	Package Description	Package Option	Branding
AD5512AACPZ-REEL7	±1 LSB	±1 LSB	Midscale	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DFQ
AD5512AACPZ-500RL7	±1 LSB	±1 LSB	Midscale	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DFQ
AD5542ABRUZ	±1 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead TSSOP	RU-16	
AD5542ABRUZ-REEL7	±1 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead TSSOP	RU-16	
AD5542AARUZ	±2 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead TSSOP	RU-16	
AD5542AARUZ-REEL7	±2 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead TSSOP	RU-16	
AD5542ABCPZ-REEL7	±1 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead LFCSP_WQ	CP-16-22	DFL
AD5542AACPZ-REEL7	±2 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead LFCSP_WQ	CP-16-22	DFK
AD5542ABCPZ-1-RL7	±1 LSB	±1 LSB	Midscale	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	DFM
AD5542ABCPZ-500RL7	±1 LSB	±1 LSB	Midscale	−40°C to +85°C	16-Lead LFCSP_WQ	CP-16-22	DFL
EVAL-AD5542ASDZ					AD5541A Evaluation Board		

[1] Z = RoHS Compliant Part.

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