



**THE DATASHEET OF
AD557JNZ**



FEATURES

Complete 8-Bit DAC
Voltage Output—0 V to 2.56 V
Internal Precision Band-Gap Reference
Single-Supply Operation: 5 V ($\pm 10\%$)
Full Microprocessor Interface
Fast: 1 μ s Voltage Settling to $\pm 1/2$ LSB
Low Power: 75 mW
No User Trims Required
Guaranteed Monotonic Over Temperature
All Errors Specified T_{MIN} to T_{MAX}
Small 16-Lead DIP or 20-Lead PLCC Package
Low Cost

PRODUCT DESCRIPTION

The AD557 DACPORT[®] is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.

The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single 5 V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ± 2.5 LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to $\pm 1/2$ LSB for a full-scale step in 800 ns.

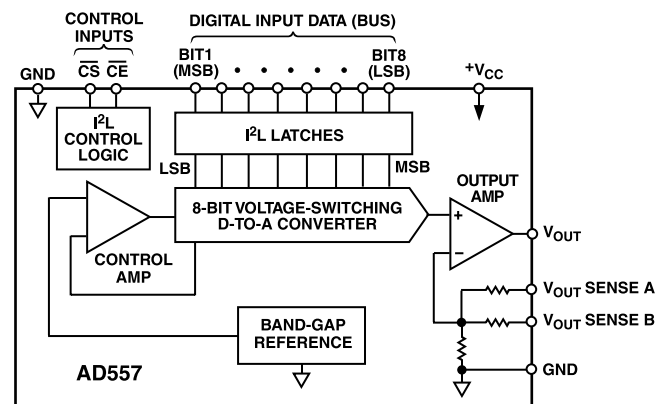
The AD557 is available in two package configurations. The AD557JN is packaged in a 16-lead plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-lead JEDEC-standard PLCC. Both versions are specified over the operating temperature range of 0°C to 70°C.

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REV. B

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FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD557 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The AD557 is designed and specified to operate from a single 4.5 V to 5.5 V power supply.
5. Low digital input currents, 100 μ A max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible.
6. The single-chip, low power I^2L design of the AD557 is inherently more reliable than hybrid multichip or conventional single-chip bipolar designs.

AD557—SPECIFICATIONS (@ $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ unless otherwise noted)

Model	Min	Typ	Max	Unit
RESOLUTION			8	Bits
RELATIVE ACCURACY 0°C to 70°C		±1/2	1	LSB
OUTPUT Ranges Current Source Sink	5	0 to 2.56		V mA
		Internal Passive Pull-Down to Ground ²		
OUTPUT SETTling TIME ³		0.8	1.5	µs
FULL-SCALE ACCURACY ⁴ @ 25°C T_{MIN} to T_{MAX}		±1.5 ±2.5	±2.5 ±4.0	LSB LSB
ZERO ERROR @ 25°C T_{MIN} to T_{MAX}			±1 ±3	LSB LSB
MONOTONICITY ⁵ T_{MIN} to T_{MAX}	Guaranteed But Not Tested			
DIGITAL INPUTS T_{MIN} to T_{MAX} Input Current Data Inputs, Voltage Bit On—Logic “1” Bit On—Logic “0” Control Inputs, Voltage On—Logic “1” On—Logic “0” Input Capacitance			±100	µA
	2.0 0		0.8	V V
	2.0 0		0.8	V V
		4		pF
TIMING ⁶ t_W Strobe Pulsewidth T_{MIN} to T_{MAX} t_{DH} Data Hold Time T_{MIN} to T_{MAX} t_{DS} Data Setup Time T_{MIN} to T_{MAX}		225 300 10 10 225 300		ns ns ns ns ns ns
POWER SUPPLY Operating Voltage Range (V_{CC}) 2.56 Volt Range Current (I_{CC}) Rejection Ratio	4.5	15	5.5 25	V mA %/%
POWER DISSIPATION, $V_{CC} = 5\text{ V}$		75	125	mW
OPERATING TEMPERATURE RANGE	0		70	°C

NOTES

¹Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See “Measuring Offset Error” on the AD558 data sheet.

²Passive pull-down resistance is 2 kΩ.

³Settling time is specified for a positive-going full-scale step to ±1/2 LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

⁴The full-scale output voltage is 2.55 V and is guaranteed with a 5 V supply.

⁵A monotonic converter has a maximum differential linearity error of ±1 LSB.

⁶See Figure 7.

Specifications shown in **boldface** are tested on all production units at electrical test. Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD557JN	0°C to 70°C	Plastic DIP	N-16
AD557JP	0°C to 70°C	Plastic Leaded Chip Carrier	P-20A

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground 0 V to 18 V
Digital Inputs (Pins 1–10) 0 V to 7.0 V
 V_{OUT} Indefinite Short to Ground
Momentary Short to V_{CC}

Power Dissipation 450 mW

Storage Temperature Range

N/P (Plastic) Packages –25°C to +100°C

Lead Temperature (Soldering, 10 sec) 300°C

Thermal Resistance

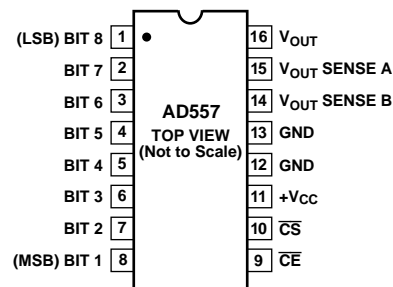
Junction to Ambient/Junction to Case

N/P (Plastic) Packages 140/55°C/W

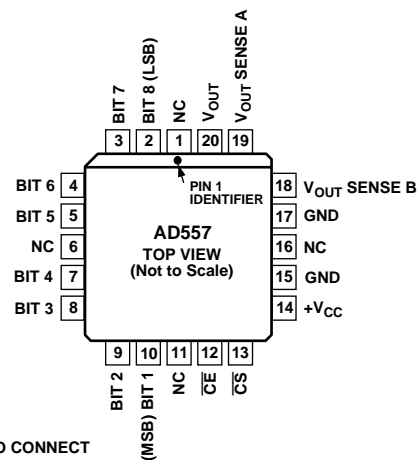
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

AD557

APPLICATIONS

Grounding and Bypassing

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD557 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD557 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 4 shows how the ground connections should be made.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD557, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD557, it is recommended that analog common be selected.

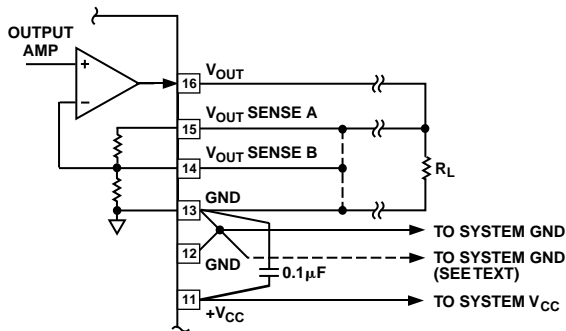


Figure 4. Recommended Grounding and Bypassing

Using a "False" Ground

Many applications, such as disk drives, require servo control voltages that swing on either side of a "false" ground. This ground is usually created by dividing the 12 V supply equally and calling the midpoint voltage "ground."

Figure 5 shows an easy and inexpensive way to implement this. The AD586 is used to provide a stable 5 V reference from the system's 12 V supply. The op amp shown likewise operates from a single (12 V) supply available in the system. The resulting output at the V_{OUT} node is ± 2.5 V around the "false" ground point of 5 V. AD557 input code vs. V_{OUT} is shown in Figure 6.

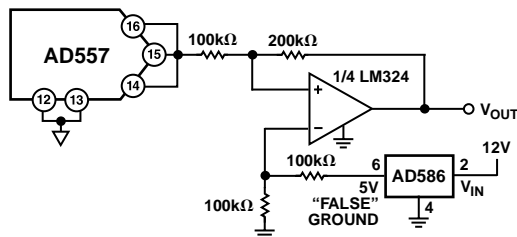


Figure 5. Level Shifting the AD557 Output Around a "False" Ground

Timing and Control

The AD557 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable (\overline{CE}) and Chip Select (\overline{CS}) inputs. \overline{CE} and \overline{CS} are internally "NORed" so that the latches transmit input data to the DAC section when both \overline{CE} and \overline{CS} are at Logic "0." If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either \overline{CE} or \overline{CS} go to Logic "1," the input data is latched into the registers and held until both \overline{CE} and \overline{CS} return to "0." (Unused \overline{CE} or \overline{CS} inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

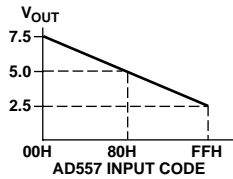


Figure 6. AD557 Input Code vs. Level Shifted Output in a "False" Ground Configuration

Table I. AD557 Control Logic Truth Table

Input Data	\overline{CE}	\overline{CS}	DAC Data	Latch Condition
0	0	0	0	"Transparent"
1	0	0	1	"Transparent"
0	f	0	0	Latching
1	f	0	1	Latching
0	0	f	0	Latching
1	0	f	1	Latching
X	1	X	Previous Data	Latched
X	X	1	Previous Data	Latched

NOTES

X = Does not matter

f = Logic Threshold at Positive-Going Transition

In a level-triggered latch such as that used in the AD557, there is an interaction between the data setup and hold times and the width of the enable pulse. In an effort to reduce the time required to test all possible combinations in production, the AD557 is tested with $t_{DS} = t_W = 225$ ns at 25°C and 300 ns at T_{MIN} and T_{MAX} , with $t_{DH} = 10$ ns at all temperatures. Failure to comply with these specifications may result in data not being latched properly.

Figure 7 shows the timing for the data and control signals, \overline{CE} and \overline{CS} are identical in timing as well as in function.

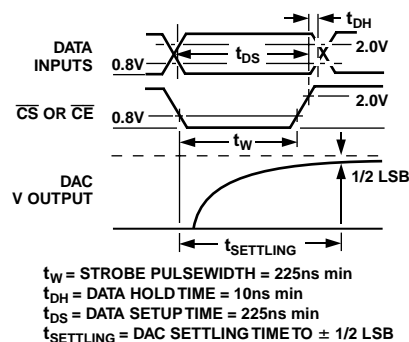
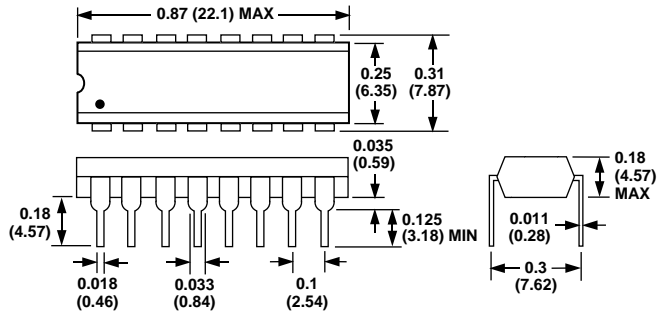


Figure 7. AD557 Timing

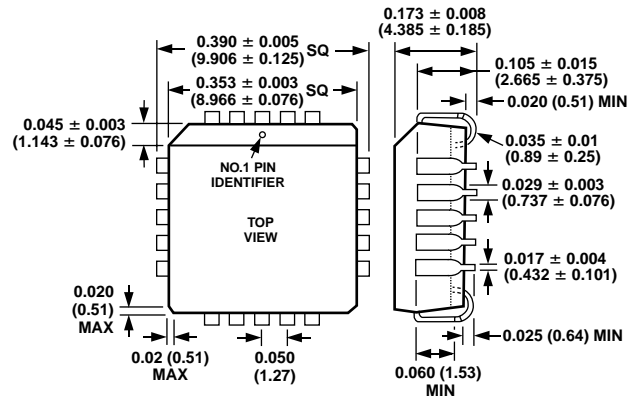
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

N-16 (Plastic) Package



P-20A (PLCC) Package



AD557—Revision History

Location	Page
Data sheet changed from REV. A to REV. B.	
Changes to MONOTONICITY section of spec. page	2

C00512a-0-1/01 (rev. B)

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