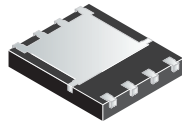




**THE DATASHEET OF  
CSD16342Q5A**





## N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16342Q5A](#)

### FEATURES

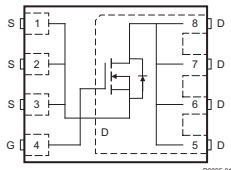
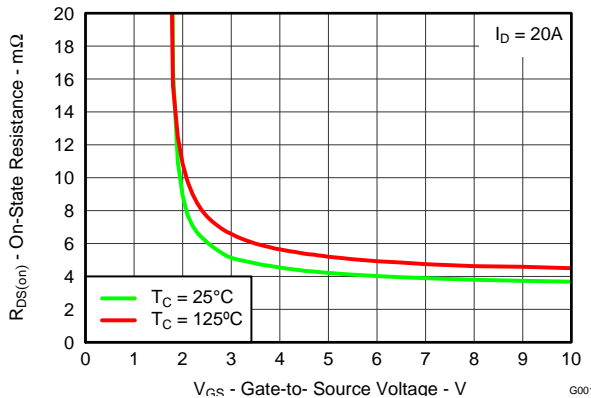
- Optimized for 5V Gate Drive
- Resistance Rated at  $V_{GS} = 2.5V$
- Ultra Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5mm x 6mm Plastic Package

### APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.

**Top View**

 **$R_{DS(ON)}$  vs  $V_{GS}$** 


### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	6.8	nC
$Q_{gd}$	Gate Charge Gate to Drain	1.2	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 2.5V$	6.1 mΩ
		$V_{GS} = 4.5V$	4.3 mΩ
		$V_{GS} = 8V$	3.8 mΩ
$V_{th}$	Threshold Voltage	0.85	V

### ORDERING INFORMATION

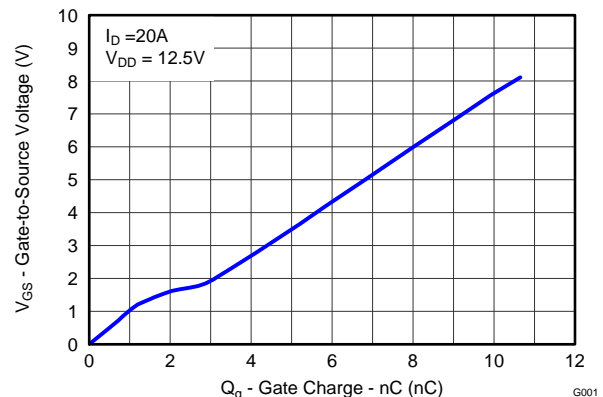
Device	Package	Media	Qty	Ship
CSD16342Q5A	SON 5 x 6 Plastic Package	13-inch reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ C$	100	A
	Continuous Drain Current <sup>(1)</sup>	21	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ C$ <sup>(2)</sup>	131	A
$P_D$	Power Dissipation <sup>(1)</sup>	3	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 40A, L = 0.1mH, R_G = 25\Omega$	80	mJ

(1) Typical  $R_{\theta JA} = 40^\circ C/W$  on 1in<sup>2</sup> Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$

**Gate Charge**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

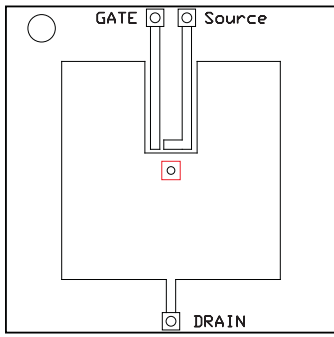
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$B_{V_{DSS}}$	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = 250\mu A$	25			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	0.6	0.85	1.1	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 2.5V, I_{DS} = 20A$		6.1	7.8	$m\Omega$
		$V_{GS} = 4.5V, I_{DS} = 20A$		4.3	5.5	$m\Omega$
		$V_{GS} = 8V, I_{DS} = 20A$		3.8	4.7	$m\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_{DS} = 20A$		91		S
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		1050	1350	pF
$C_{OSS}$	Output Capacitance			730	950	pF
$C_{RSS}$	Reverse Transfer Capacitance			53	69	pF
$R_g$	Series Gate Resistance			1.5	3	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 12.5V, I_D = 20A$		6.8	7.1	nC
$Q_{gd}$	Gate Charge Gate to Drain			0.9		nC
$Q_{gs}$	Gate Charge Gate to Source			1.9		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.2		nC
$Q_{OSS}$	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		13.7		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A$ $R_G = 2\Omega$		5.2		ns
$t_r$	Rise Time			16.6		ns
$t_{d(off)}$	Turn Off Delay Time			13.4		ns
$t_f$	Fall Time			3.1		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_S = 20A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 20A, di/dt = 300A/\mu s$		14.5		nC
$t_{rr}$	Reverse Recovery Time			20		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

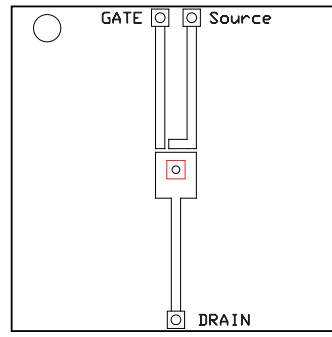
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			50	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



M0161-01

Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on 1  
 $\text{inch}^2$  of 2 oz. Cu.



M0161-02

Max  $R_{\theta JA} = 123^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

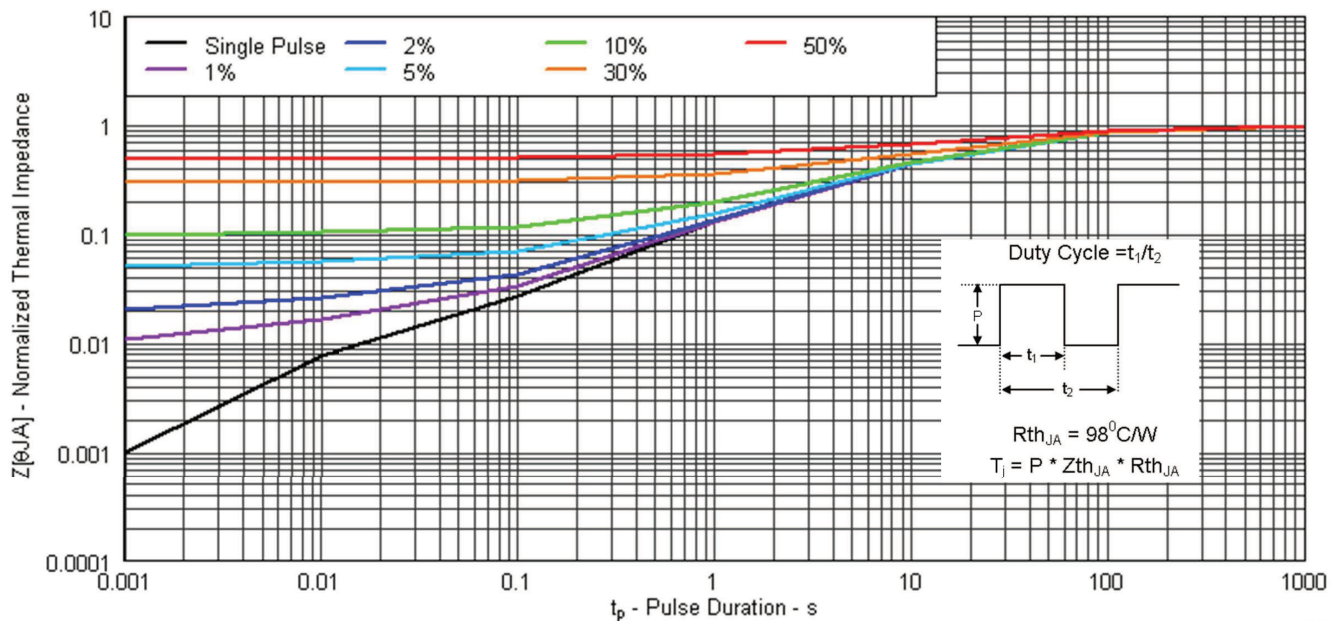
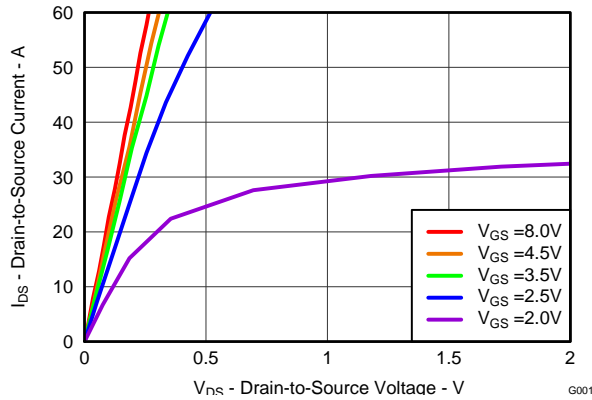


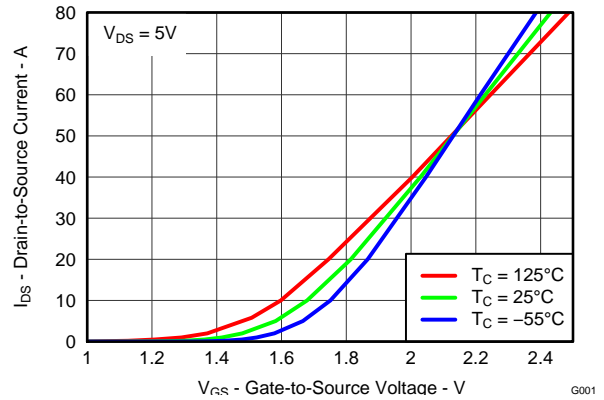
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

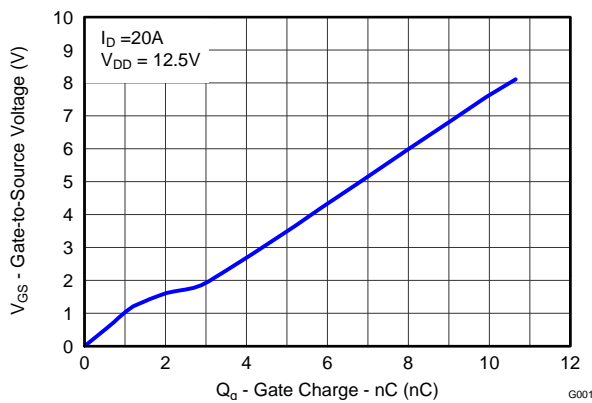
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



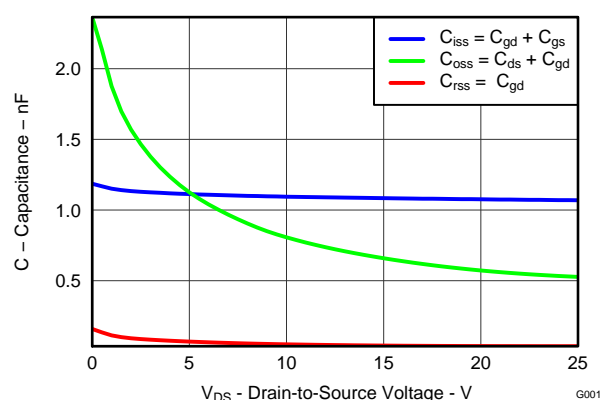
**Figure 2. Saturation Characteristics**



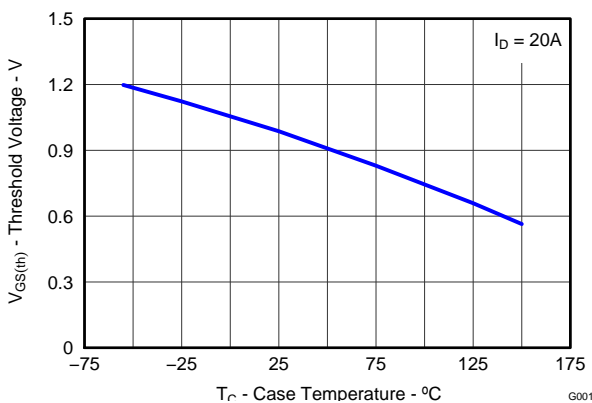
**Figure 3. Transfer Characteristics**



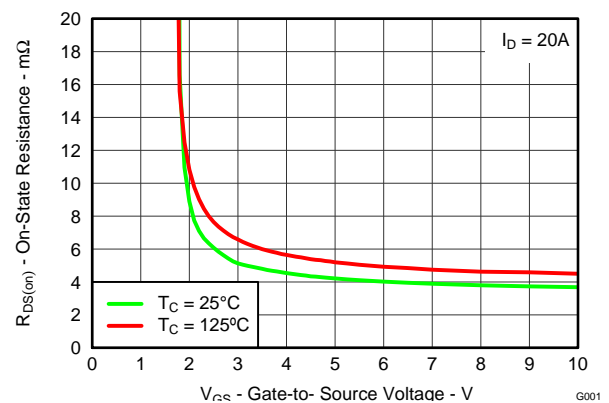
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On Resistance vs. Gate Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

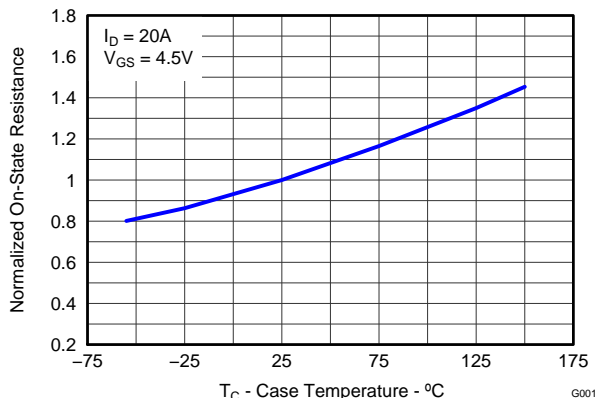


Figure 8. Normalized On Resistance vs. Temperature

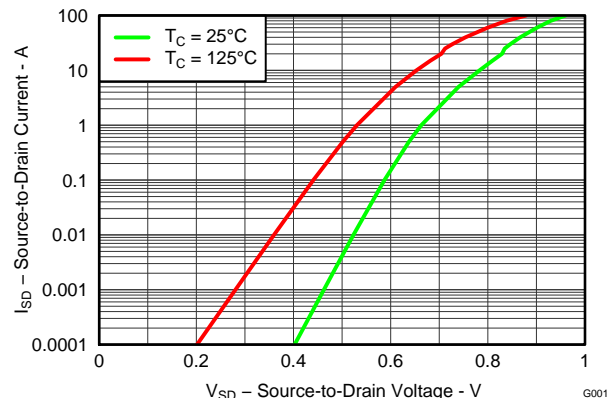


Figure 9. Typical Diode Forward Voltage

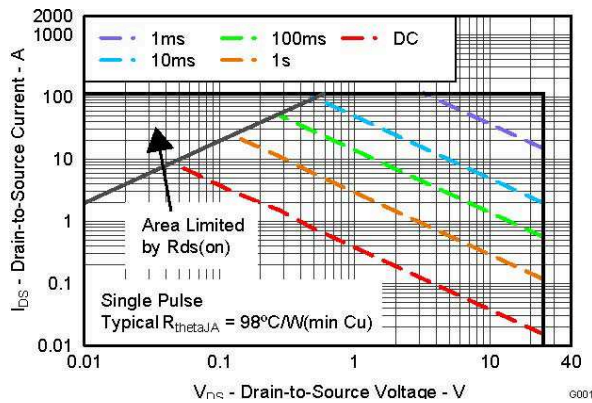


Figure 10. Maximum Safe Operating Area

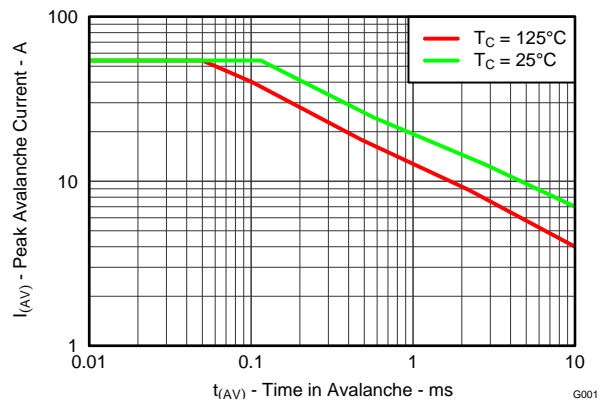


Figure 11. Single Pulse Unclamped Inductive Switching

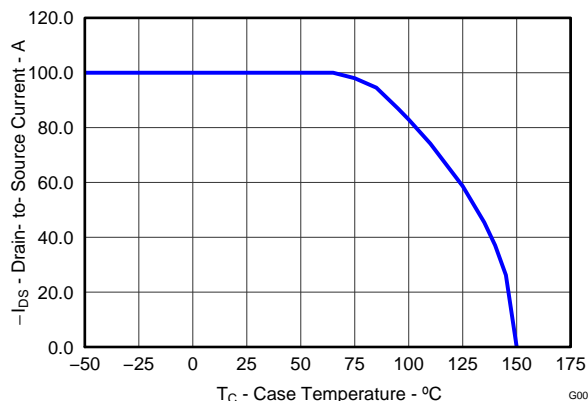
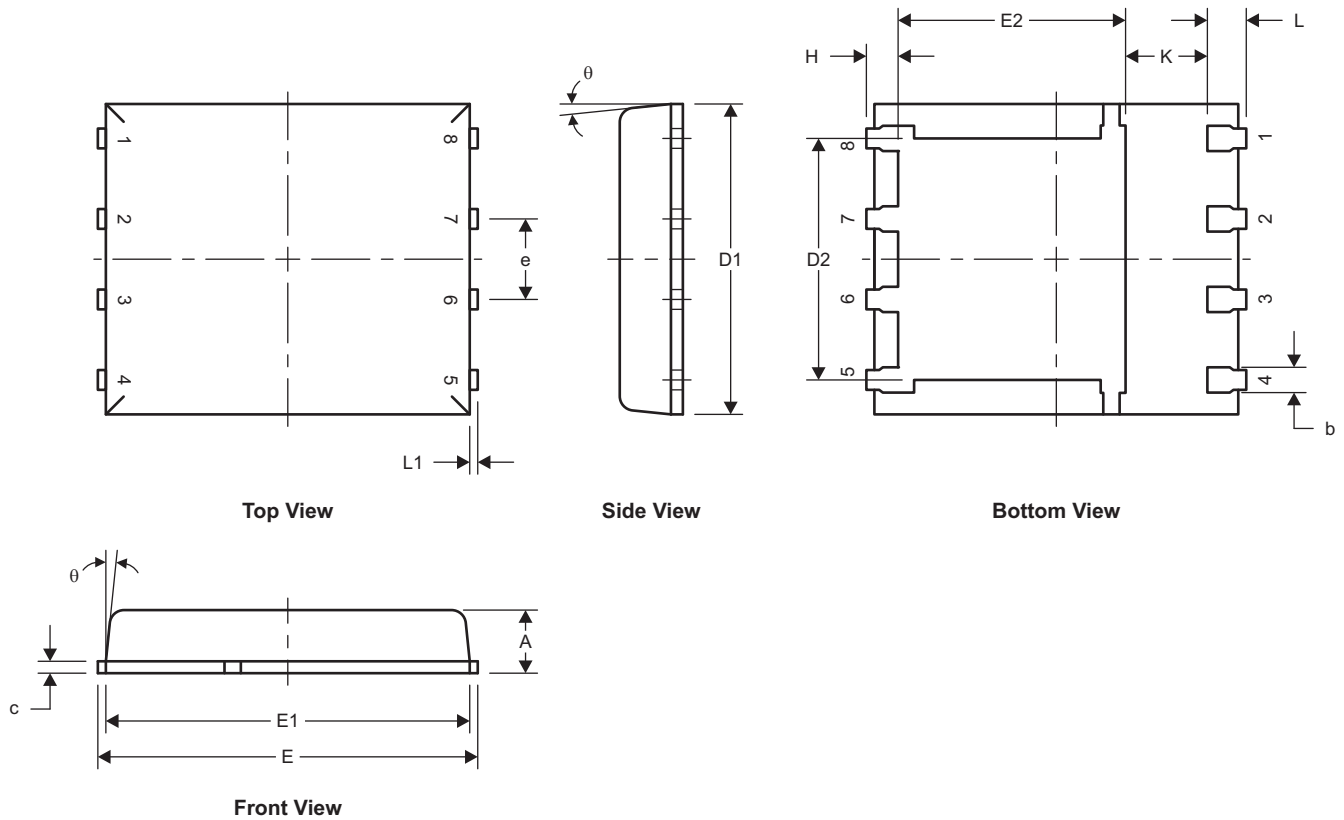


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

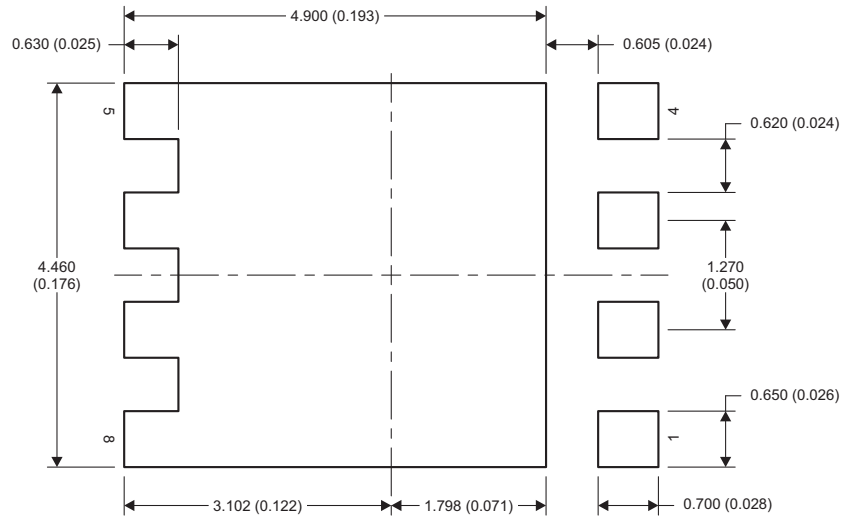
**Q5A Package Dimensions**



M0135-01

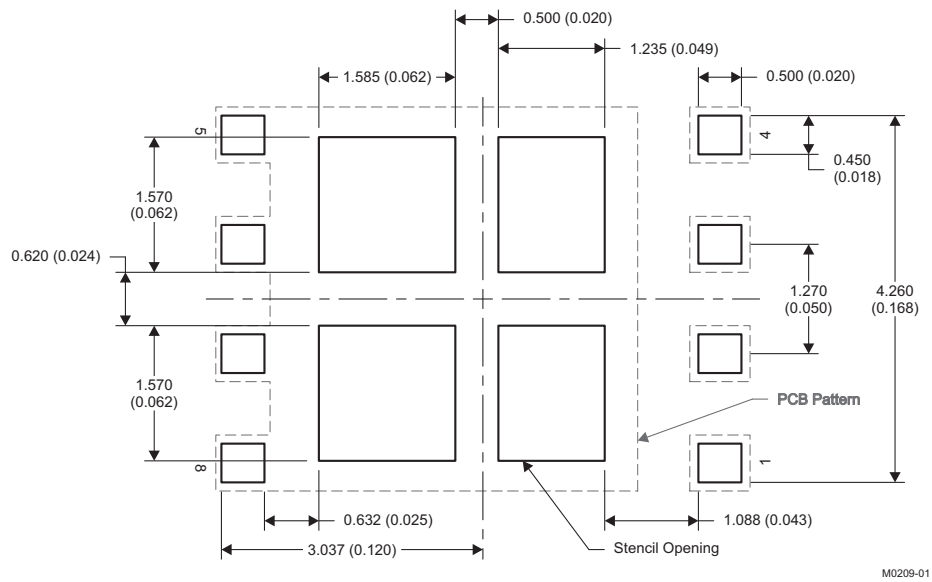
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.037	0.039	0.043
b	0.33	0.41	0.51	0.000	0.000	0.002
c	0.20	0.25	0.34	0.011	0.013	0.016
D1	4.80	4.90	5.00	0.006	0.008	0.010
D2	3.61	3.81	4.02	0.126	0.130	0.134
E	5.90	6.00	6.10	-	-	-
E1	5.70	5.75	5.80	0.065	0.069	0.071
E2	3.38	3.58	3.78	0.126	0.130	0.134
e	1.17	1.27	1.37	-	-	-
H	0.41	0.56	0.71	0.093	0.096	0.100
K	1.10					
L	0.51	0.61	0.71	0.014	0.018	0.022
L1	0.06	0.13	0.20	0.014	0.018	0.022
$\theta$	0°		12°	-	-	-
$\theta$	-	-	-	-	-	-

### Recommended PCB Pattern



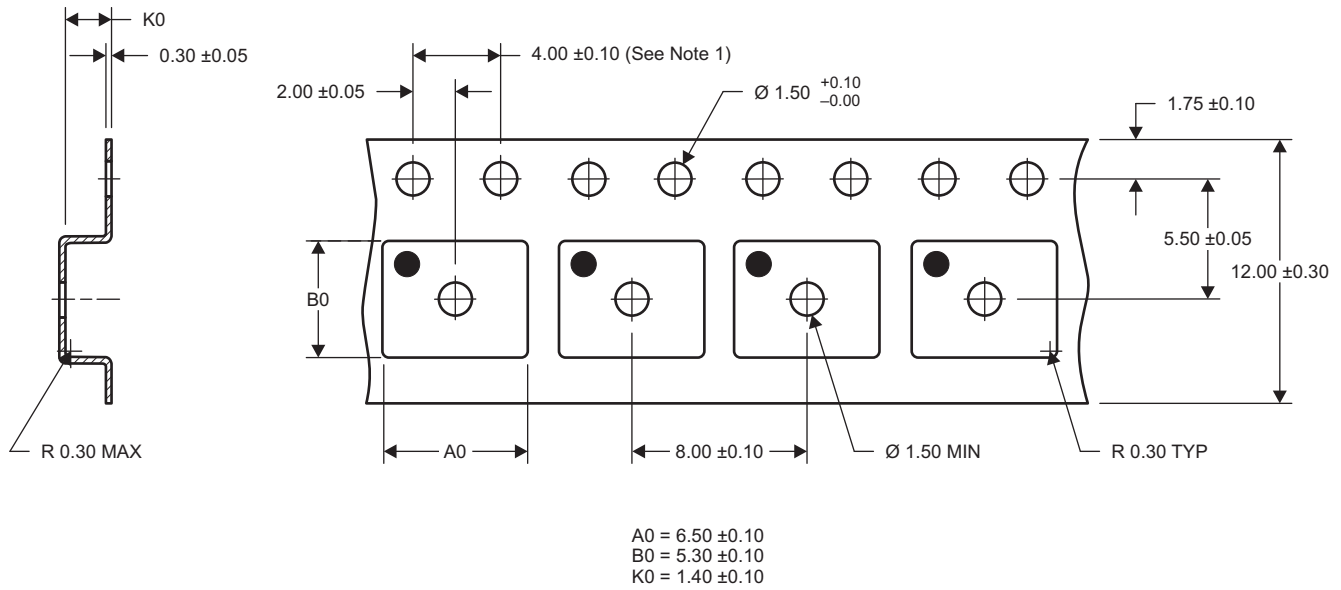
For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Stencil Recommendation



NOTE: Dimensions are in mm (inches).

**Q5A Tape and Reel Information**



M0138-01

- NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2  
 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm  
 3. Material: black static-dissipative polystyrene  
 4. All dimensions are in mm (unless otherwise specified)  
 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

**REVISION HISTORY**

Changes from Original (February 2012) to Revision A	Page
• Changed the device status From: Product Preview To: Production .....	1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16342Q5A	ACTIVE	VSONP	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16342	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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### Applications

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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