



THE DATASHEET OF LP2980IM5-1.8/NOPB



LP2980LV

Micropower SOT, 50 mA Low-Voltage Low-Dropout Regulator For Applications With Output Voltages < 2V

General Description

The LP2980LV is a 50 mA, fixed-output voltage regulator designed for high performance in applications requiring output voltages below 2V.

Using an optimized VIP® (Vertically Integrated PNP) process, the LP2980LV delivers unequalled performance in all specifications critical to battery-powered designs:

Low Ground Pin Current. Typically 280 μ A @ 50 mA load, and 75 μ A @ 1 mA load.

Sleep Mode. Less than 1 μ A quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size. SOT-23 package uses absolute minimum board space.

Precision Output. 0.5% tolerance output voltages available (A grade).

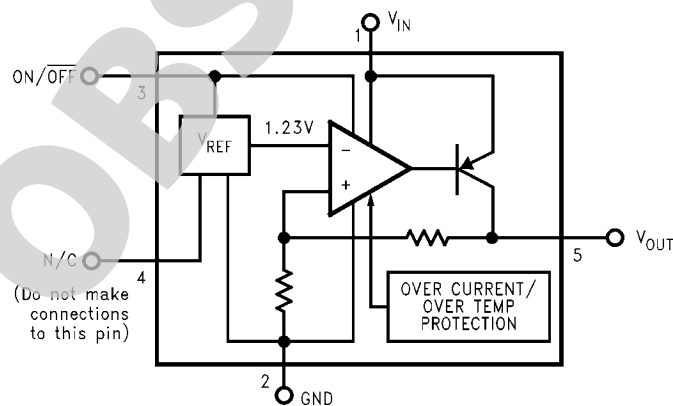
Features

- Guaranteed 50 mA output current
- Smallest possible size (SOT-23 Package)
- Requires few external components
- < 1 μ A quiescent current when shutdown
- Low ground pin current at all load currents
- Output voltage accuracy 0.5% (A Grade)
- High peak current capability (150 mA typical)
- Wide supply voltage range (16V max)
- Fast dynamic response to line and load
- Low Z_{OUT} 0.1 Ω typical (10 Hz to 1 MHz)
- Overtemperature/overcurrent protection
- -40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

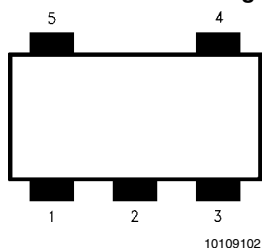
Block Diagram



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Connection Diagrams

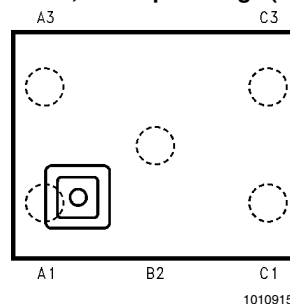
5-Lead Small Outline Package (M5)



Top View

See NS Package Number MF05A
For ordering information see Table 1

micro SMD, 5 Bump Package (BPA05)



Top View

See NS Package Number BPA05

Note: The actual physical placement of the package marking will vary from part to part. The package marking will designate the date code and will vary considerably. Package marking does not correlate to device type in any way.

Pin Descriptions

Name	Pin Number		Function
	SOT-23	micro SMD	
V_{IN}	1	C3	Input Voltage
GND	2	A1	Common Ground (device substrate)
ON/OFF	3	A3	Logic high enable input
N/C	4	B2	Post package trim - do not connect to this pin
V_{OUT}	5	C1	Regulated output voltage

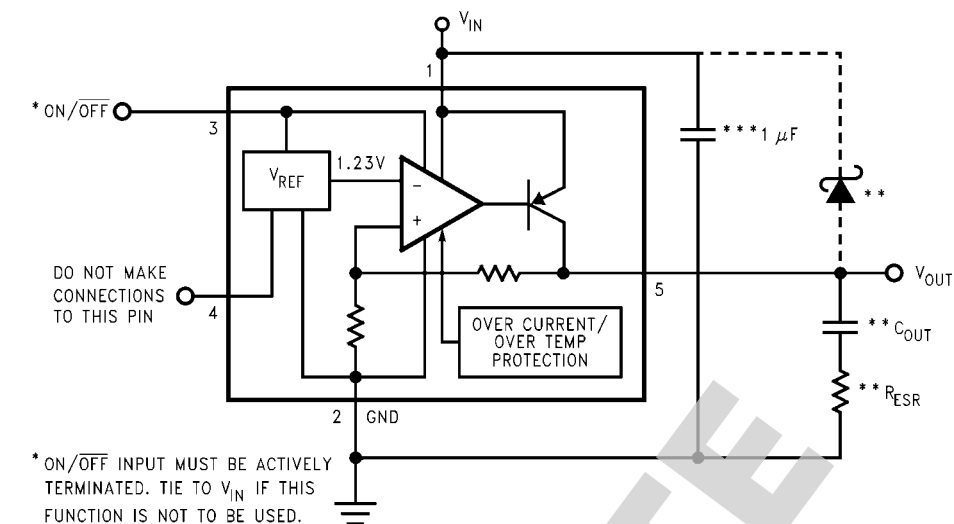
Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
1.5V	A	LP2980AIM5X-1.5	LANA	3000 Units on Tape and Reel
1.5V	A	LP2980AIM5-1.5	LANA	1000 Units on Tape and Reel
1.5V	STD	LP2980IM5X-1.5	LANB	3000 Units on Tape and Reel
1.5V	STD	LP2980IM5-1.5	LANB	1000 Units on Tape and Reel
1.8V	A	LP2980AIM5X-1.8	LAGA	3000 Units on Tape and Reel
1.8V	A	LP2980AIM5-1.8	LAGA	1000 Units on Tape and Reel
1.8V	STD	LP2980IM5X-1.8	LAGB	3000 Units on Tape and Reel
1.8V	STD	LP2980IM5-1.8	LAGB	1000 Units on Tape and Reel

For output voltages > 2V, refer to LP2980 datasheet. If a non-standard voltage is required, see LP2980-ADJ.

Basic Application Circuit



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	-40°C to +125°C
Lead Temperature (Soldering, 5 sec.)	260°C
ESD Rating (Note 2)	2 kV

Power Dissipation (Note 3)

Input Supply Voltage (Survival)	-0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
ON/OFF Input Voltage (Survival)	-0.3V to +16V
Output Voltage (Survival), (Note 4)	-0.3V to +9V
I _{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival), (Note 5)	-0.3V to +16V

Internally Limited

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = V_{O(NOM)} + 1V, I_L = 1 mA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{ON/OFF} = 2V.

Symbol	Parameter	Conditions	Typ	LP2980LVAI-XX (Note 6)		LP2980LVI-XX (Note 6)		Units
				Min	Max	Min	Max	
ΔV _O	Output Voltage Tolerance	I _L = 1 mA		-0.50	0.50	-1.00	1.00	%V _{NOM}
		1 mA < I _L < 50 mA		-0.75	0.75	-1.50	1.50	
				-2.50	2.50	-3.50	-3.50	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output Voltage Line Regulation	V _{O(NOM)} + 1V ≤ V _{IN} ≤ 16V	0.007		0.014 0.032		0.014 0.032	%/V
I _{GND}	Ground Pin Current	I _L = 0	65		85 110		85 110	µA
		I _L = 1 mA	75		95 160		95 160	
		I _L = 10 mA	120		175 325		175 325	
		I _L = 50 mA	280		475 850		475 850	
		V _{ON/OFF} < 0.18V	0		1		1	
V _{IN(min)}	Minimum input voltage required to maintain output regulation	I _L = 50 mA	2.05		2.20		2.20	V
V _{ON/OFF}	ON/OFF Input Voltage (Note 7)	High = O/P ON	1.4	1.6		1.6		V
		Low = O/P OFF	0.55		0.18		0.18	
I _{ON/OFF}	ON/OFF Input Current	V _{ON/OFF} = 0	0		-1		-1	µA
		V _{ON/OFF} = 5V	5		15		15	
I _{O(PK)}	Peak Output Current	V _{OUT} ≥ V _{O(NOM)} - 5%	150	100		100		mA
e _n	Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, C _{OUT} = 10 µF	125					µV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	f = 1kHz C _{OUT} = 10 µF	63					dB
I _{O(MAX)}	Short Circuit Current	R _L = 0 (Steady State) (Note 8)	150					mA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: The ESD rating of pins 3 and 4 is 1 kV.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J(MAX)}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(\text{MAX}) = \frac{T_J(\text{MAX}) - T_A}{\theta_{JA}}$$

The value of θ_{JA} for the SOT-23 package is 220°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 4: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2980LV output must be diode-clamped to ground.

Note 5: The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} will turn on this diode and possibly damage the device (see Application Hints).

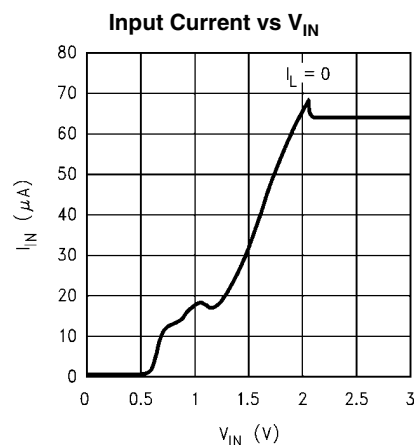
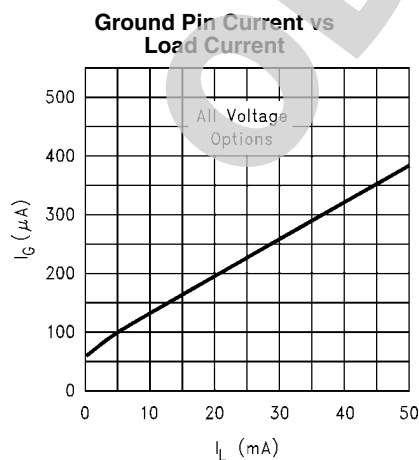
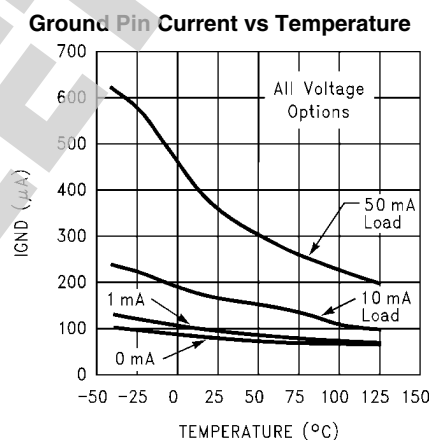
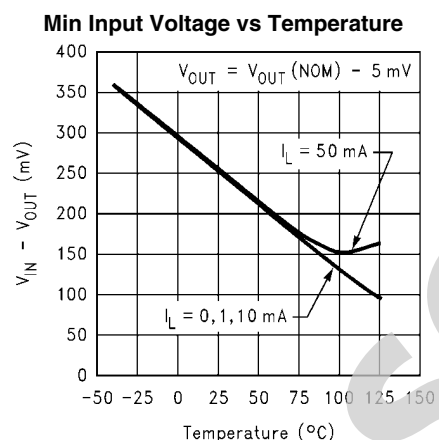
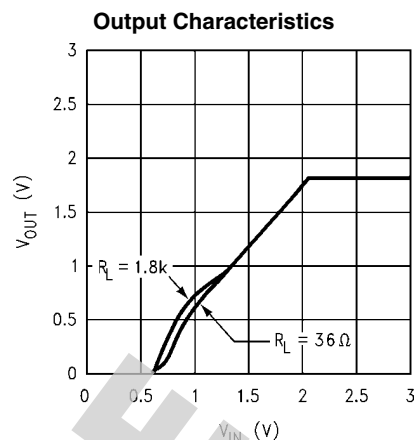
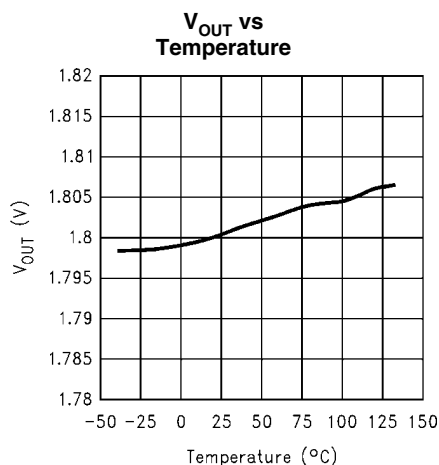
Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

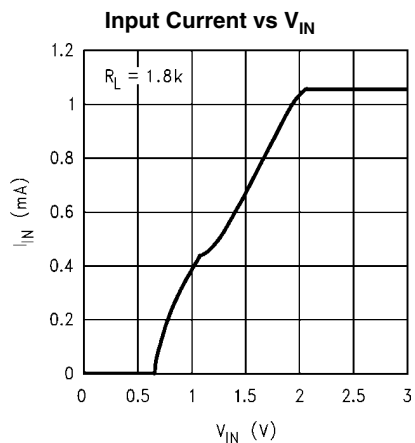
Note 7: The ON/OFF input must be properly driven to prevent misoperation. For details, refer to Application Hints.

Note 8: See Typical Performance Characteristics curves.

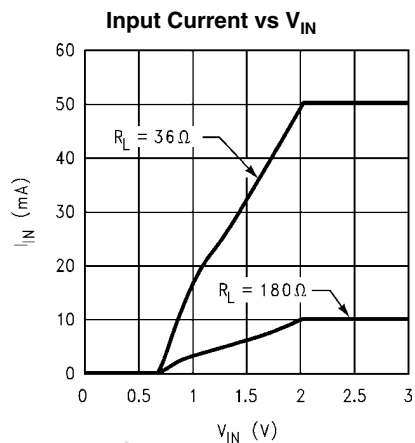
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Typical Performance Characteristics Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 1\ \mu\text{F}$, ON/OFF pin tied to V_{IN} , $V_{IN} = V_{O(NOM)} + 1\text{V}$, $V_{OUT(NOM)} = 1.8\text{V}$.

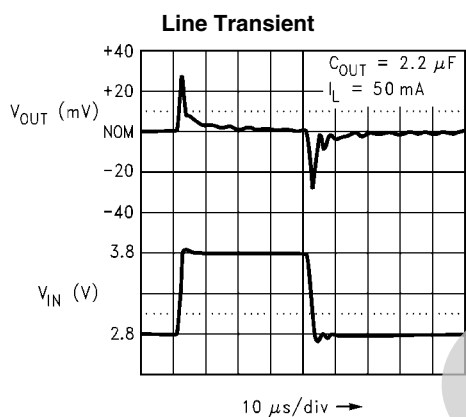




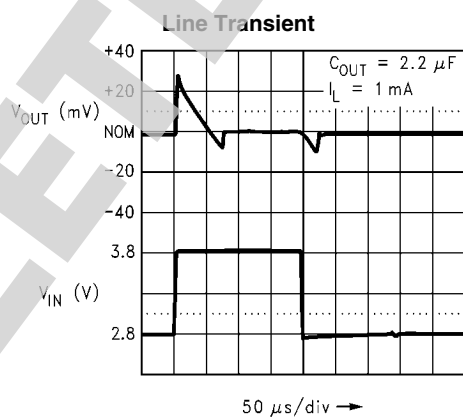
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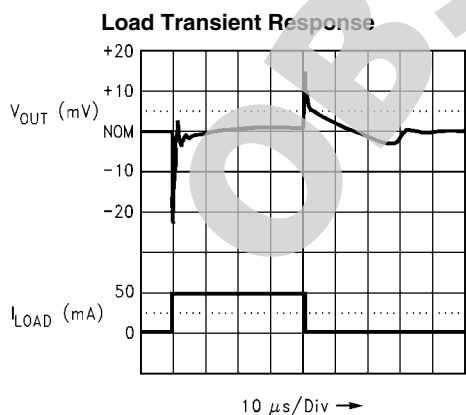
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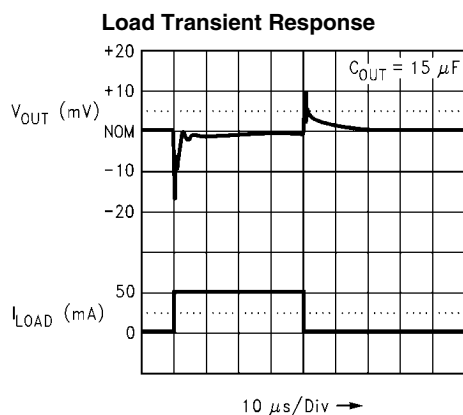
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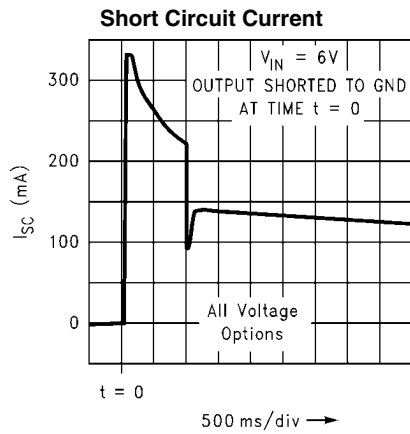
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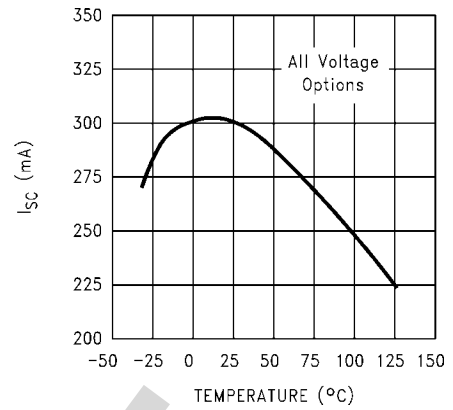
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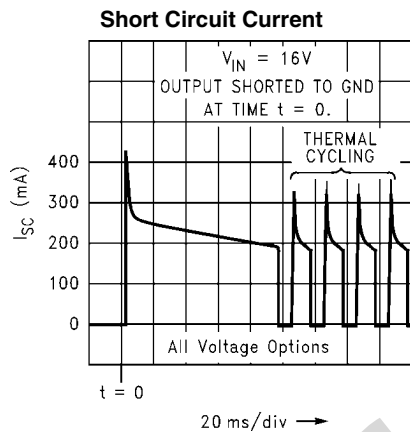
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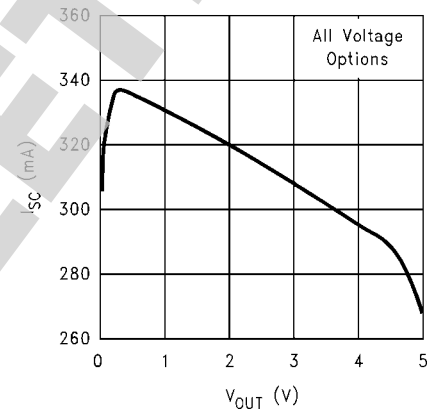
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Instantaneous Short Circuit Current vs Temperature

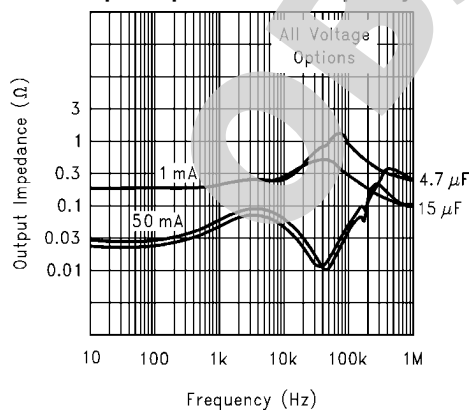
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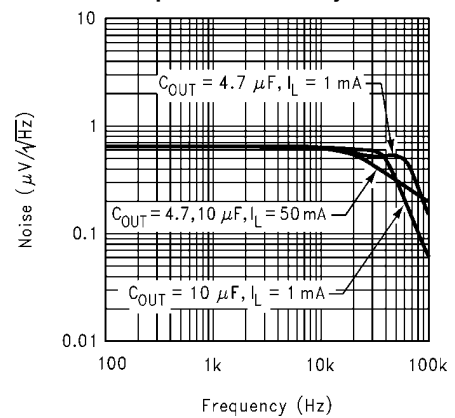
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Instantaneous Short Circuit Current vs Output Voltage

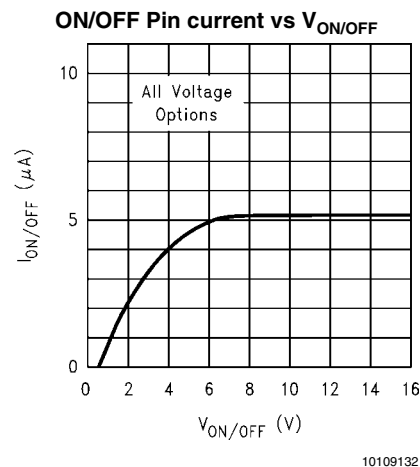
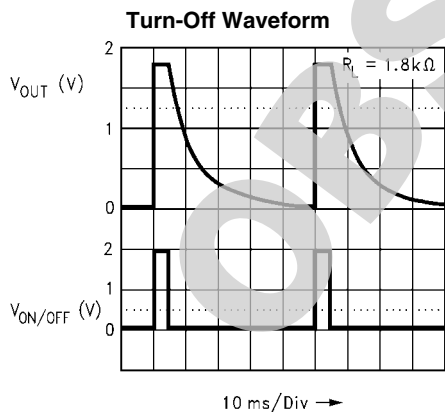
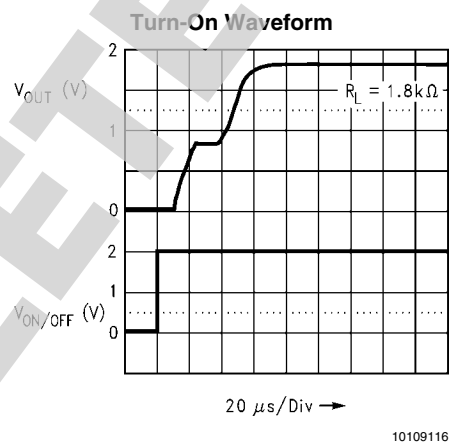
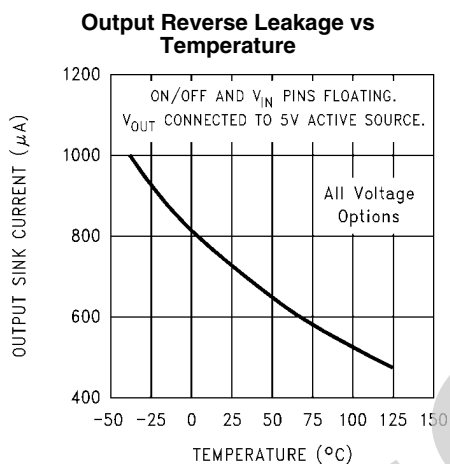
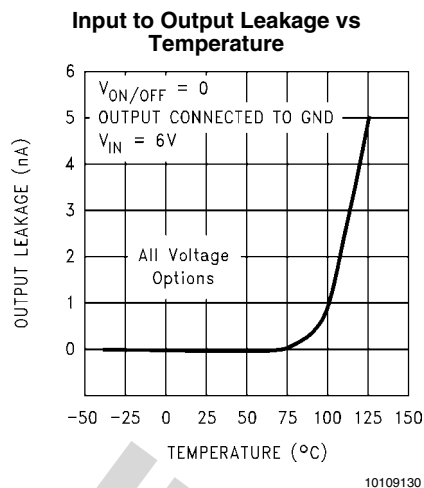
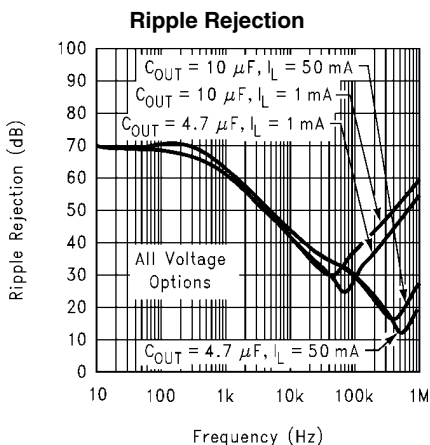
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Output Impedance vs Frequency

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Output Noise Density

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Application Hints

INPUT CAPACITOR

An input capacitor whose capacitance is $\geq 1 \mu\text{F}$ is required between the LP2980 input pin and ground (the amount of capacitance may be increased without limit).

The input capacitor must be located a distance of not more than 1 cm away from the input pin and returned to a clean analog ground. Any good quality ceramic, Tantalum, or film capacitor may be used at the input.

IMPORTANT: Tantalum capacitors may suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a Tantalum input capacitor is used, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

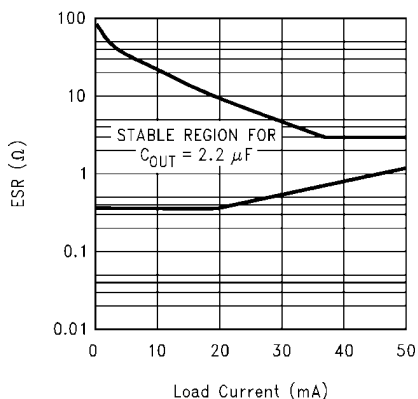
There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be $\geq 1 \mu\text{F}$ over the entire operating range.

OUTPUT CAPACITOR

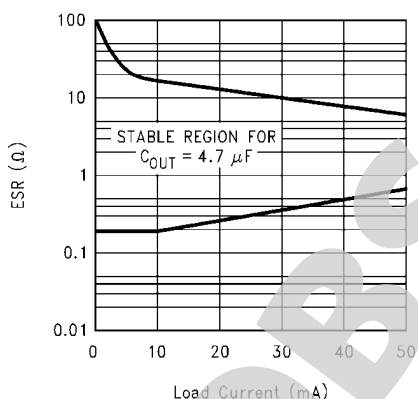
The LP2980 requires an output capacitor to maintain loop stability. The capacitor must be selected to meet the requirements of capacitance and ESR (equivalent series resistance) over the full operating temperature range of the application (see **SELECTING THE OUTPUT CAPACITOR**).

The minimum amount of capacitance which can be used on the output is 2.2 μF , but this value may be increased without limit.

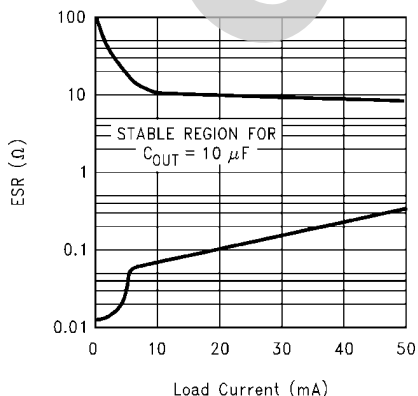
Four curves are provided which show the stable ESR range of the LP2980-1.8V operated with output capacitances of 2.2, 4.7, 10, and 15 μF :



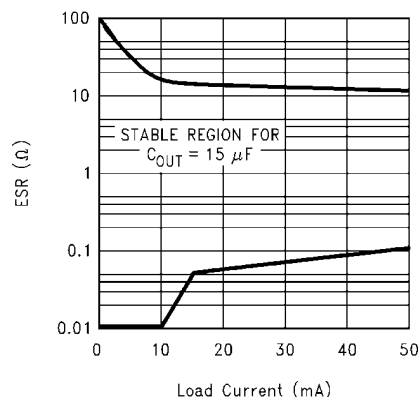
2.2 μF ESR Curves For 1.8V Output



4.7 μF ESR Curves For 1.8V Output



10 μF ESR Curves For 1.8V Output



15 μF ESR Curves For 1.8V Output

It should be noted that for the lower values of the output capacitance ($< 10 \mu\text{F}$), it may be necessary to use a capacitor and series resistance to provide sufficient ESR. To understand why this is true, the basic characteristics of capacitance types must be explained:

CAPACITOR CHARACTERISTICS

Ceramic Capacitors have an extremely low ESR (in the range of 5–15 $\text{m}\Omega$), and can only be used on the output of the LP2980 if an external resistor is placed in series to supply the needed ESR (a resistance value of about $2\Omega \pm 30\%$ is recommended).

Be careful of the temperature coefficient of ceramics: select X7R or X5R if possible, because those types typically vary less than $\pm 25\%$ over the range of -40 to $+125^\circ\text{C}$. Z5U types are worse, and will typically lose half (or more) of their capacitance over the same temperature range.

A source for large-value ceramics with good performance is Taiyo-Yuden. Their web address is :

<http://www.t-yuden.com/hicap.html>

Tantalum capacitors have ESR values that are more difficult to determine: the manufacturers specify only a maximum limit, which is typically 10X or 20X the typical value. ESR values can vary considerably from lot to lot and from manufacturer to manufacturer. For example, some 4.7 $\mu\text{F}/10\text{V}$ devices tested showed typical values in the range of 0.5 - 1 Ω , but values as high as 6 Ω have been seen.

It should also be noted that the ESR typically increases about 2X - 3X when going from $+125^\circ\text{C}$ down to -40°C .

Another factor to consider is that Tantalum manufacturers are presently designing their products toward the goal of getting the lowest possible ESR, in an attempt to compete with the new high-value ceramic capacitors. This means that the typical values will probably continue to decline in the future.

SELECTING THE OUTPUT CAPACITOR

This section contains guidelines for selecting an output capacitor which will maintain good regulator stability over the entire operating temperature range (refer to **ESR CURVES**).

2.2 μF Output Capacitor

The smallest output capacitor which can be used with the LP2980-1.8 is 2.2 μF . However, care must be exercised if this value is used because of the ESR requirement.

At load currents $\leq 25\text{mA}$, the stable ESR range is approximately 0.5 Ω to 6 Ω . This range is probably sufficiently wide that most 2.2 μF Tantalum capacitors would fall within it.

At higher values of load currents (using a 2.2 μF output capacitor), the stable ESR window gets very narrow. It is likely that a Tantalum capacitor would not be a good choice for a design that must be robust enough for mass production. Instead, a 2.2 μF capacitor with very low ESR (either ceramic or film) should be used with a 2Ω external resistor placed in series to provide the ESR.

4.7 μF Output Capacitor

If a 4.7 μF capacitor is used, the stable range of ESR values for 50 mA operation is approximately 0.6Ω to 6Ω . Because of the reduced ESR values of the new Tantalum, it is possible to find 4.7 μF Tantalum capacitors with ESR values at or below 0.6Ω . To ensure a stable design, it is recommended that an external resistor (value about 0.5Ω) be added in series with the 4.7 μF Tantalum to provide adequate minimum ESR.

At values of load current ≤ 20 mA, the ESR range is wide enough that Tantalum can be used without external resistance for added ESR.

Another acceptable configuration for 50 mA operation is to use a ceramic or film 4.7 μF capacitor (which has very low ESR) with an external 2Ω resistor in series.

10 μF Output Capacitor

50 mA operation using a 10 μF output capacitor requires an ESR in the range of approximately 0.4Ω to 7Ω . As stated previously, it is possible that solid Tantalum capacitors can be found with ESR values near to or below 0.4Ω . An external resistor in series with the Tantalum (value of about 0.5Ω) is recommended to assure unconditional stability.

At values of load current ≤ 20 mA, the ESR range is wide enough that Tantalum can be used without external resistance for added ESR.

Another acceptable configuration for 50 mA operation is to use a ceramic or film 10 μF capacitor (which has very low ESR) with an external 2Ω resistor in series.

15 μF Output Capacitor

The stable ESR range (for 50 mA load current) using a 15 μF output capacitor is approximately 0.1Ω to 10Ω . It is extremely unlikely that a 15 μF Tantalum capacitor would be found with

an ESR below 0.1Ω , so no external resistance is required with a Tantalum.

As before, another acceptable configuration for 50 mA operation is to use a ceramic or film 15 μF capacitor with an external 2Ω resistor in series.

ON/OFF INPUT OPERATION

The LP2980 is shut off by pulling the ON/OFF input low, and turned on by pulling it high. If this feature is not to be used, this pin should be tied to V_{IN} to keep the regulator on at all times.

To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds (see Electrical Characteristics).

It is also important that the turn-on (and turn-off) voltage signals applied to the ON/OFF input have a slew rate which is not less than $40 \text{ mV}/\mu\text{s}$.

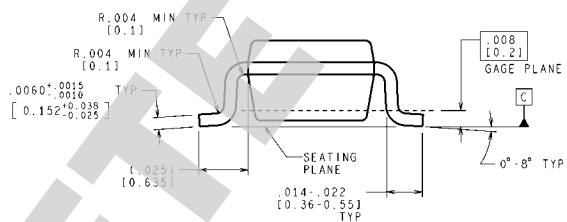
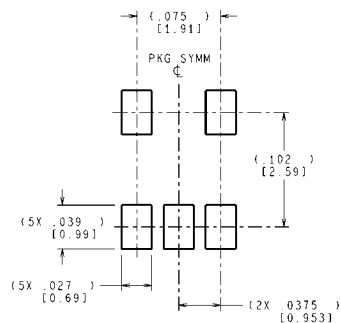
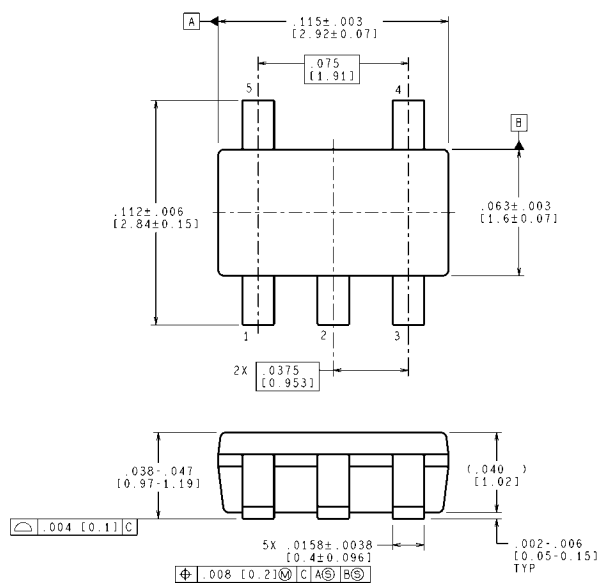
CAUTION: The regulator output state can not be guaranteed if a slow-moving AC (or DC) signal is applied that it is in the range between the turn-on/turn-off voltage thresholds specified in the Electrical Characteristics section.

REVERSE INPUT/OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP2980 has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN} , anode on V_{OUT}), to limit the reverse voltage across the LP2980 to 0.3V (see Basic Application Circuit).



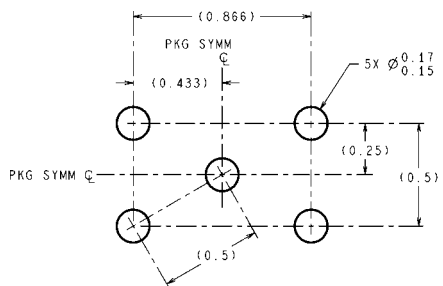
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VALUES IN [] ARE MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

MF05A (Rev D)

5-Lead Small Outline Package (M5)
NS Package Number MF05A

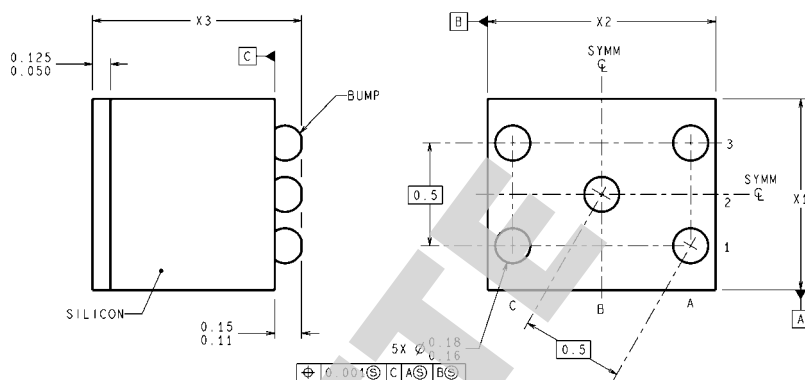
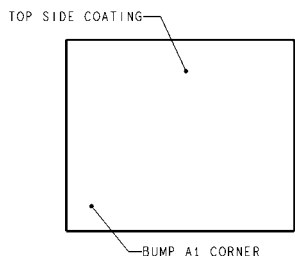
NS Package Number MF05A

For Order Numbers, refer to *Table 1* in the “Order Information” section of this document.



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LAND PATTERN RECOMMENDATION



BPA05XXX (Rev D)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCK-WISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. NO JEDEC REGISTRATION AS OF AUG. 1999.

micro SMD, 5 Bump, Package (BPA05) NS Package Number BPA05A

For Order Numbers, refer to *Table 1* in the "Ordering Information" section of this document.

The dimensions for X1, X2 and X3 are as given:

X1 = 0.930 +/- 0.030mm
X2 = 1.107 +/- 0.030mm
X3 = 0.850 +/- 0.050mm

Notes

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