THE DATASHEET OF

TLC542CDWR

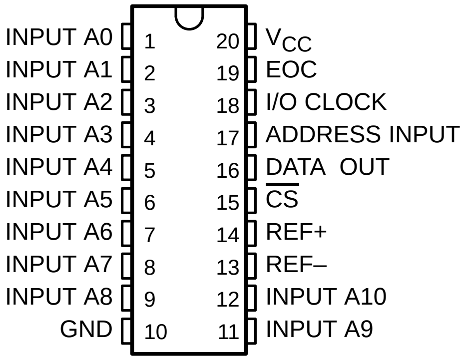
TLC542C, TLC542I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS075C – FEBRUARY 1989 – REVISED JUNE 2001

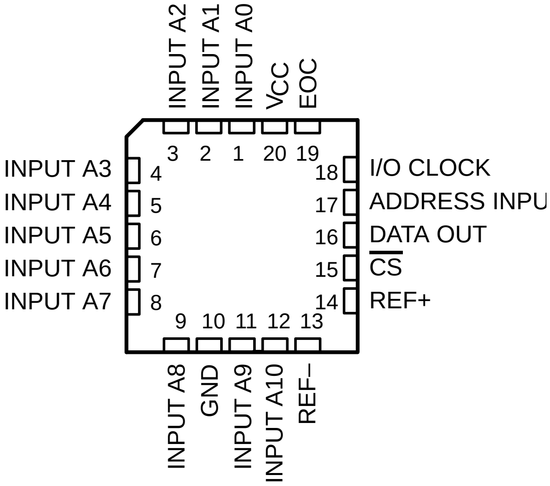
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Direct Replacement for Motorola MC145041**
- **Onboard System Clock**
- **End-of-Conversion (EOC) Output**
- **Pinout and Control Signals Compatible With the TLC1542/3 10-Bit A/D Converters**
- **CMOS Technology**

PARAMETER	VALUE
Channel Acquisition/Sample Time	16 µs
Conversion Time (Max)	20 µs
Samples per Second (Max)	25×10^3
Power Dissipation (Max)	10 mW

DW OR N PACKAGE (TOP VIEW)



FN PACKAGE (TOP VIEW)



description

The TLC542 is a CMOS converter built around an 8-bit switched-capacitor successive-approximation analog-to-digital converter. The device is designed for serial interface to a microprocessor or peripheral via a 3-state output with three inputs [including I/O CLOCK, CS (chip select), and ADDRESS INPUT]. The TLC542 allows high-speed data transfers and sample rates of up to 40,000 samples per second. In addition to the high-speed converter and versatile control logic, an on-chip 12-channel analog multiplexer can sample any one of 11 inputs or an internal *self-test* voltage, and the sample and hold is started under microprocessor control. At the end of conversion, the end-of-conversion (EOC) output pin goes high to indicate that conversion is complete.

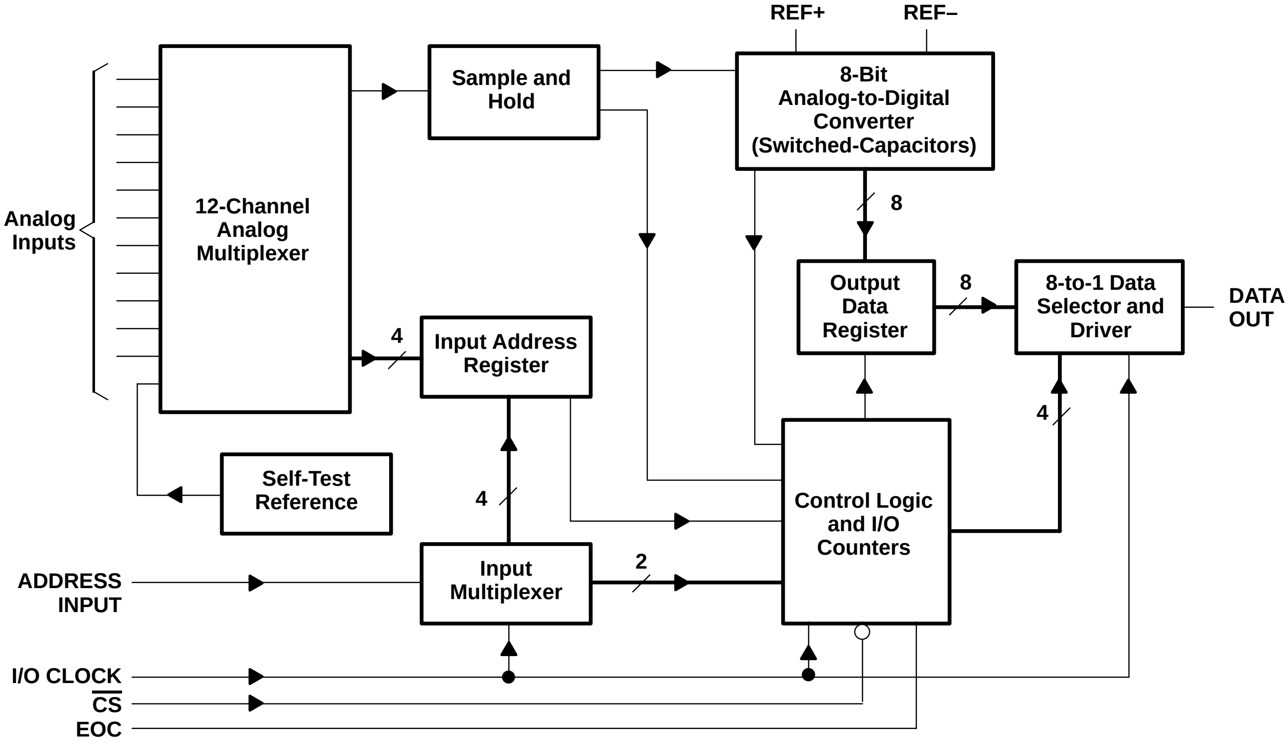
The converter incorporated in the TLC542 features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 20 µs over the full operating temperature range.

The TLC542C is characterized for operation from 0°C to 70°C and the TLC542I is characterized for operation from −40°C to 85°C.

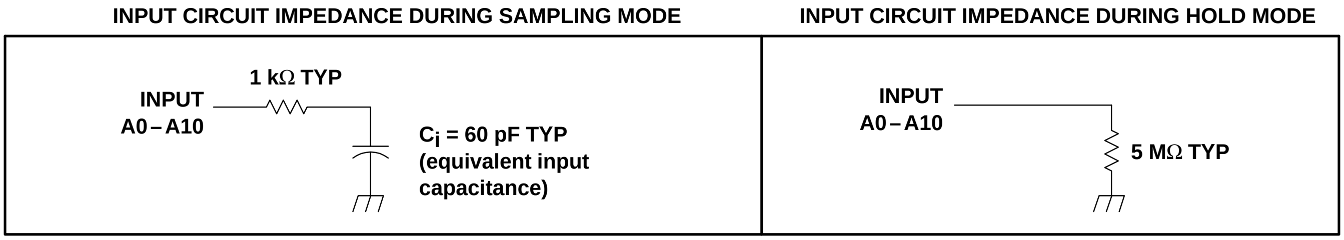
AVAILABLE OPTIONS

T_A	PACKAGE		
	CHIP CARRIER (FN)	PLASTIC DIP (N)	SMALL OUTLINE (DW)
0°C to 70°C	—	TLC542CN	TLC542CDW
−40°C to 85°C	TLC542IFN	TLC542IN	TLC542IDW

functional block diagram

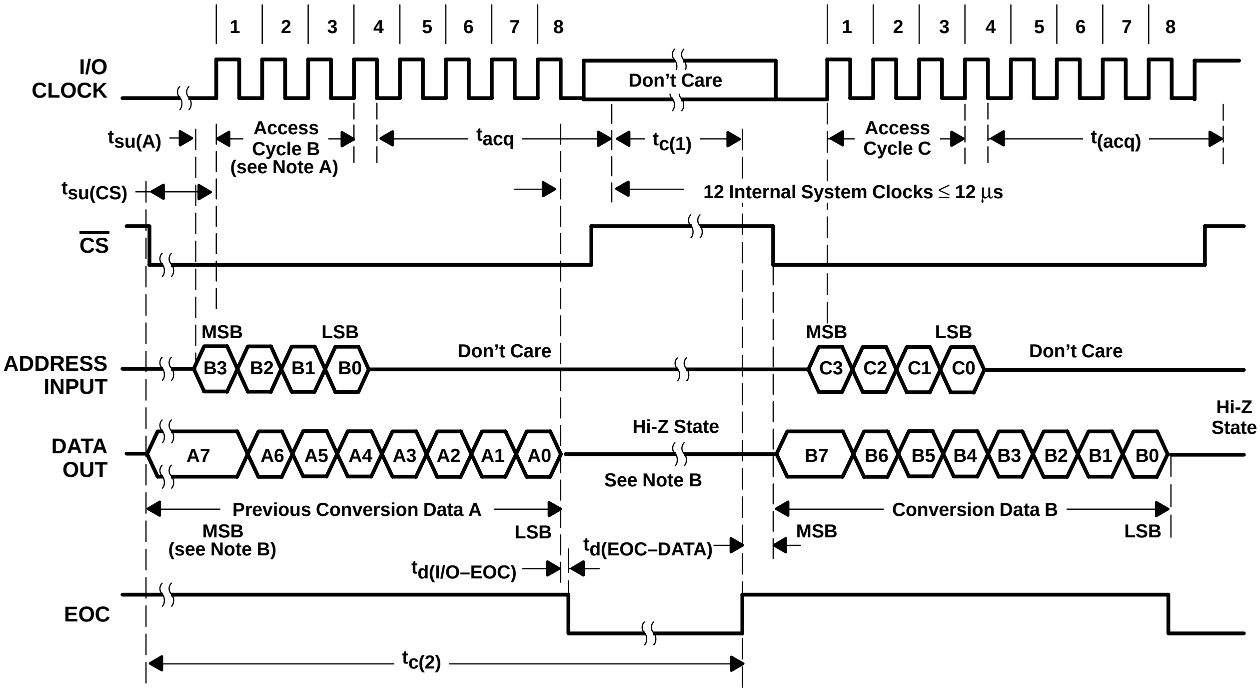


typical equivalent inputs


INPUT CIRCUIT IMPEDANCE DURING SAMPLING MODE

INPUT CIRCUIT IMPEDANCE DURING HOLD MODE

operating sequence



NOTES: A. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$↓ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(CS)}$ specifications. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

B. The output becomes 3-state on $\overline{CS}$ going high or on the negative edge of the eighth I/O clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	–0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O	–0.3 V to V_{CC} + 0.3 V
Peak input current range (any input), $I_{p-p)}$	±20 mA
Peak total input current (all inputs), I_P	±30 mA
Operating free-air temperature range: TLC542C	0°C to 70°C
TLC542I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds, T_C: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions, V_{CC} = 4.75 to 5.5 V

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{ref-}	V_{CC}	V_{CC} + 0.1	V
Negative reference voltage, V_{ref-} (see Note 2)		–0.1	0	V_{ref+}	V
Differential reference voltage, $V_{ref+} – V_{ref-}$ (see Note 2)		1	V_{CC}	V_{CC} + 0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	V
High-level control input voltage, V_{IH}		2			V
Low-level control input voltage, V_{IL}				0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$		400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$		0			ns
Hold time, $\overline{CS}$ low after 8th I/O CLOCK↑, $t_{h(CS)}$		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 4)		3.8			µs
Input/output clock frequency, $f_{(clock\ I/O)}$		0	1.1		MHz
Input/output clock high, $t_{w(H\ I/O)}$		404			ns
Input/output clock low, $t_{w(L\ I/O)}$		404			ns
I/O CLOCK transition time, t_t (see Note 3)	$f_{clock(I/O)} \le 525$ kHz			100	ns
	$f_{clock(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A	TLC542C	0		70	°C
	TLC542I	–40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF– convert as all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF–. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

4. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(CS)}$ specifications. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+}$ = 4.75 V to 5.5 V, $f_{(clock\ I/O)}$ = 1.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)		V_{CC} = 4.75 V, I_{OH} = –360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
	Off-state (high-impedance state) output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}			10	µA
			V_O = 0, $\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		$V_I = V_{CC}$		0.005	2	µA
I_{IL}	Low-level input current		V_I = 0		–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2	mA
	Selected channel leakage current		Selected channel at V_{CC} and unselected channel at 0 V			0.4	µA
			Selected channel at 0 V and unselected channel at V_{CC}			–0.4	
I_{ref}	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$, V_{ref-} = GND			10	µA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

† All typical values are at T_A = 25°C.

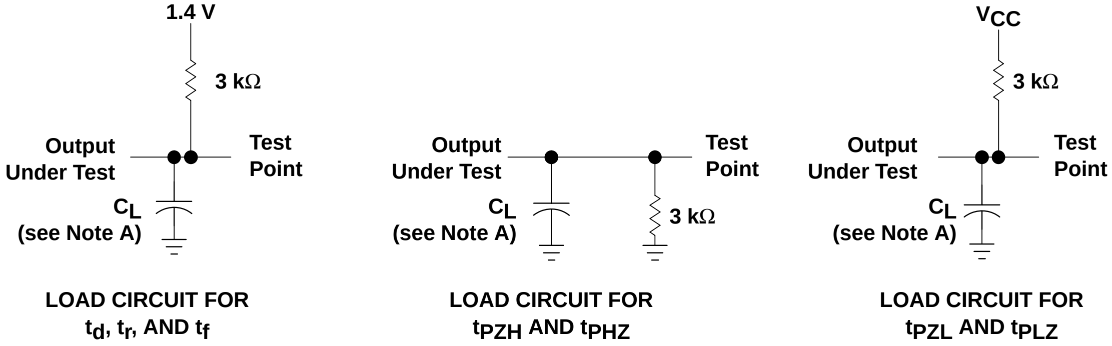
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.75$ to 5.5 V, $f_{(clock\ I/O)} = 1$ MHZ

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)				±0.5	LSB
E_{ZS}	Zero-scale error (see Note 6)	See Note 2			±0.5	LSB
E_{FS}	Full-scale error (see Note 6)	See Note 2			±0.5	LSB
	Total unadjusted error (see Note 7)				±0.5	LSB
	Self-test output code	Input A11 address = 1011, See Note 8	01111101 (126)	128	10000011 (130)	
$t_{c(1)}$	Conversion time	See operating sequence			20	μs
$t_{c(2)}$	Total access and conversion cycle time	See operating sequence			40	μs
$t_{(acq)}$	Channel acquisition time (sample cycle)	See operating sequence			16	μs
$t_{(v)}$	Time output data remains valid after I/O CLK↓	See Figure 5	10			ns
$t_{d(IO\text{-}DATA)}$	Delay time, I/O CLK↓ to data output valid	See Figure 5			400	ns
$t_{d(IO\text{-}EOC)}$	Delay time, 8th I/O CLK↓ to EOC↓	See Figure 6			500	ns
$t_{d(EOC\text{-}DATA)}$	Delay time, EOC↑ to data out (MSB)	See Figure 7			400	ns
t_{PZH}, t_{PZL}	Delay time, CS↓ to data out (MSB)	See Figure 2			3.4	μs
t_{PHZ}, t_{PLZ}	Delay time, CS↑ to data out (MSB)	See Figure 2			150	ns
$t_{r(EOC)}$	Rise time	See Figure 7			100	ns
$t_{f(EOC)}$	Fall time	See Figure 6			100	ns
$t_{r(bus)}$	Data bus rise time	See Figure 5			300	ns
$t_{f(bus)}$	Data bus fall time	See Figure 5			300	ns

† All typical values are at $T_A = 25°C$.

NOTES:
2. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF– convert to all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF–. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L = 50 pF

Figure 1. Load Circuits

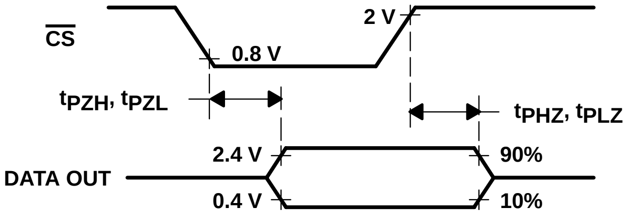


Figure 2. $\overline{CS}$ to Data Output Timing

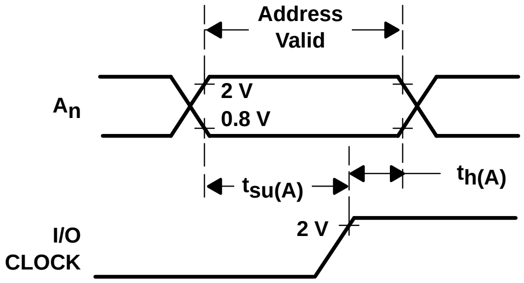


Figure 3. Address Timing

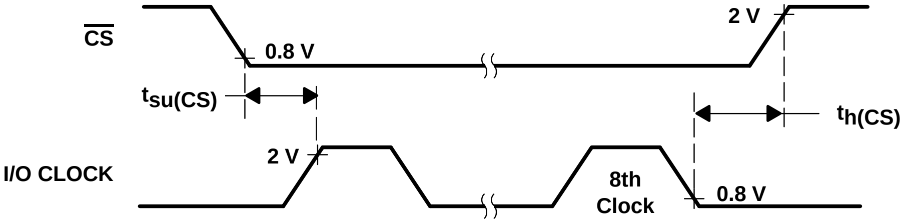


Figure 4. Figure 4. $\overline{CS}$ to I/O CLOCK Timing

PARAMETER MEASUREMENT INFORMATION

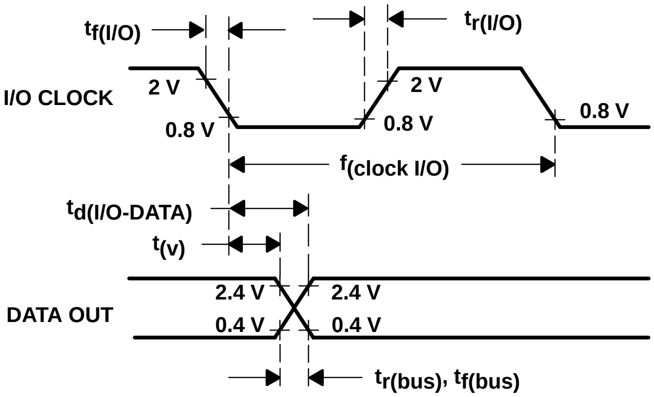


Figure 5. Data Output Timing

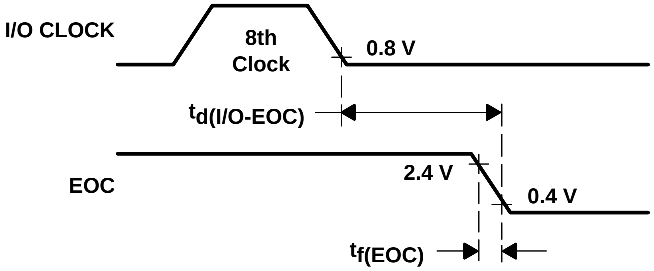


Figure 6. EOC Timing

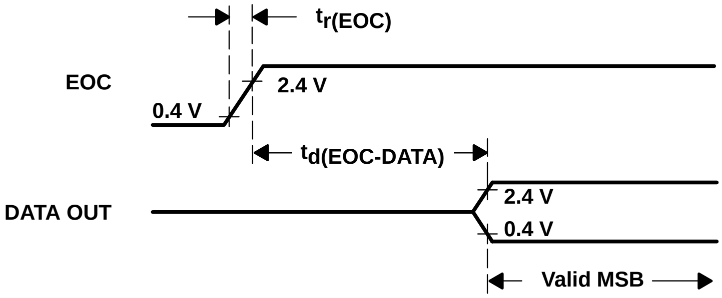


Figure 7. Data Output to EOC Timing

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 8, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/512) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{3}$$

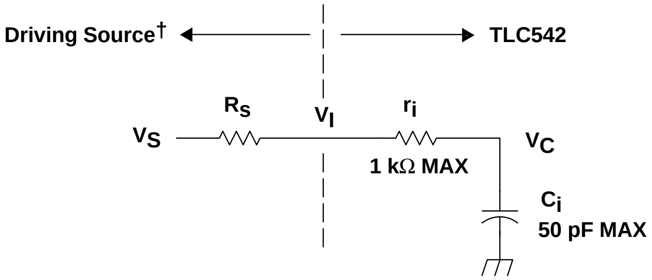
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(512) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_S + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0 – A10
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 8. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC542 is a complete data acquisition system on a single chip. The device includes such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. Three control inputs (I/O CLOCK, $\overline{\text{CS}}$ (chip select), and ADDRESS INPUT) are included for flexibility and access speed. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, the TLC542 can complete a conversion in 20 µs, while complete input-conversion-output cycles can be repeated every 40 µs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

When $\overline{\text{CS}}$ is high, the DATA OUT terminal is in a 3-state condition, and the ADDRESS INPUT and I/O CLOCK terminals are disabled. When additional TLC542 devices are used, this feature allows each of these terminals, with the exception of the $\overline{\text{CS}}$ terminal, to share a control logic point with their counterpart terminals on additional A/D devices. Thus, this feature minimizes the control logic terminals required when using multiple A/D devices.

The control sequence is designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is as follows:

1. $\overline{\text{CS}}$ is brought low. To minimize errors caused by noise at the $\overline{\text{CS}}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock before recognizing the low $\overline{\text{CS}}$ transition. The MSB of the result of the previous conversion automatically appears on the DATA OUT terminal.
2. On the first four rising edges of the I/O CLOCK, a new positive-logic multiplexer address is shifted in, with the MSB of this address shifted first. The negative edges of these four I/O CLOCK pulses shift out the second, third, fourth, and fifth most significant bits of the result of the previous conversion. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge of the I/O CLOCK. The sampling operation basically involves charging the internal capacitors to the level of the analog input voltage.
3. Three clock cycles are applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O CLOCK terminal. The falling edge of this clock cycle initiates a 12-system clock (≈ 12 µs) additional sampling period while the output is in the high-impedance state. Conversion is then performed during the next 20 µs. After this final I/O CLOCK cycle, $\overline{\text{CS}}$ must go high or the I/O CLOCK must remain low for at least 20 µs to allow for the conversion function.

$\overline{\text{CS}}$ can be kept low during periods of multiple conversion. If $\overline{\text{CS}}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{\text{CS}}$ causes a reset condition, which aborts the conversion process.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 20-µs conversion time has elapsed. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

The end-of-conversion (EOC) output goes low on the negative edge of the eighth I/O CLOCK. The subsequent low-to-high transition of EOC indicates the A/D conversion is complete and the conversion is ready for transfer.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLC542CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC542CNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC542IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC542IFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC542IFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC542IFNR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC542IFNRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC542IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC542INE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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