THE DATASHEET OF

TPS78330DDCT

TPS783xx 500-nA I_Q, 150-mA, Ultralow Quiescent Current Low-Dropout Linear Regulator

1 Features

- Input Voltage Range: 2.2 V to 5.5 V
- Low Quiescent Current (I_Q): 500 nA
- 150-mA, Low-Dropout Regulator
- Low-Dropout at 25°C, 130 mV at 150 mA
- Low-Dropout at 85°C, 175 mV at 150 mA
- 3% Accuracy Over Load, Line, and Temperature
- Stable with a 1.0-µF Ceramic Capacitor
- Thermal Shutdown and Overcurrent Protection
- CMOS Logic Level-Compatible Enable Pin
- DDC (SOT-5) Package

2 Applications

- TI MSP430 Attach Applications
- Wireless Handsets and Smartphones
- MP3 Players
- Battery-Operated Handheld Products

3 Description

The TPS783 family of low-dropout regulators (LDOs) offers the benefits of ultralow power and miniaturized packaging.

This LDO family is designed specifically for battery-powered applications where ultralow quiescent current is a critical parameter. The TPS783, with ultralow I_Q (500 nA), is ideal for microprocessors, microcontrollers, and other battery-powered applications.

The absence of pulldown circuitry at the output of the LDO provides the flexibility to use the regulator output capacitor as a temporary backup power supply (for example, during battery replacement).

The ultralow power and miniaturized packaging allow designers to customize power consumption for specific applications. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

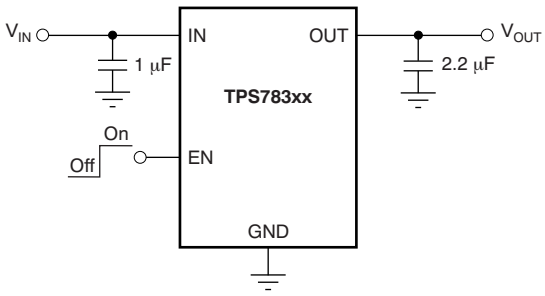
The TPS783 family is compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This device allows for minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS783 family also features thermal shutdown and current limit to protect the device during fault conditions. All packages have a specified operating temperature range of T_J = –40°C to 105°C.

Device Information(1)

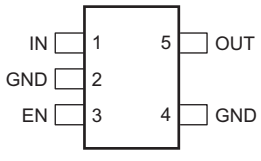
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS783xx	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Schematic



TPS783xxDDC
SOT-5
(Top View)



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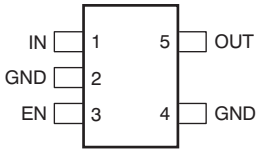
4 Revision History

Changes from Original (February 2010) to Revision A **Page**

- Changed document format to latest data sheet standards; added *Handling Ratings*, *Thermal Information*, *Recommended Operating Conditions*, *Power Supply Recommendations*, and *Device and Documentation Support* sections; moved existing sections ... 1
- Deleted factory programming feature bullet ... 1
- Added input voltage range feature bullet ... 1
- Deleted programmable mode application bullet ... 1
- Added simplified schematic to front page ... 1
- Changed *Pin Functions* table ... 3
- Changed operating junction temperature maximum value in *Absolute Maximum Ratings* table ... 4
- Deleted *Dissipation Ratings* table; see *Thermal Information* table ... 4
- Changed symbol and parameter names for clarity in *Electrical Characteristics* table ... 5
- Added footnote (2) to *Electrical Characteristics* table ... 5
- Changed Figure 7 y-axis title and measurement range ... 7
- Changed Figure 9 V_{EN} labels to match *Electrical Characteristics* table ... 7
- Changed Figure 10 y-axis title to match *Electrical Characteristics* table ... 7
- Deleted Figure 14 I_{OUT} condition ... 7
- Deleted Figure 15 I_{OUT} condition ... 7
- Changed Functional Block Diagram ... 9
- Changed Figure 18 ... 10
- Added reference for Table 1 in *Device Functional Modes* ... 10
- Changed Figure 19 ... 11
- Changed Table 2 format ... 14

5 Pin Configuration and Functions

DDC Package
SOT-5
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Drive this pin over 1.2 V to turn on the regulator. Drive this pin below 0.4 V to put the regulator into shutdown mode, reducing operating current to 18 nA, typical.
GND	2, 4	—	Ground pin. Tie all ground pins to ground for proper operation.
IN	1	I	Input pin. For stable operation, place a small, 0.1-µF capacitor from this pin to ground; typical input capacitor = 1.0 µF. Tie back both input and output capacitor grounds to the IC ground, with no significant impedance between them.
OUT	5	O	Regulated output voltage pin. Connect a small (1-µF or greater) ceramic capacitor from this pin to ground for stable operation. See the *Input and Output Capacitor Requirements* in the *Application and Implementation* section for more details.

6 Specifications

6.1 Absolute Maximum Ratings

At T_J = –40°C to 105°C (unless otherwise noted). All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.0	V
	EN pin	–0.3	V_{IN} + 0.3	V
	V_{OUT}	–0.3	V_{IN} + 0.3	V
Current	I_{OUT}	Internally limited		A
	Output short-circuit duration	Indefinite		
Temperature	Operating junction, T_J	–40	160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.2		5.5	V
V_{OUT}	Output voltage	1.8		4.2	V
V_{EN}	Enable voltage	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
T_J	Junction temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS783xx DDC (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	34.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

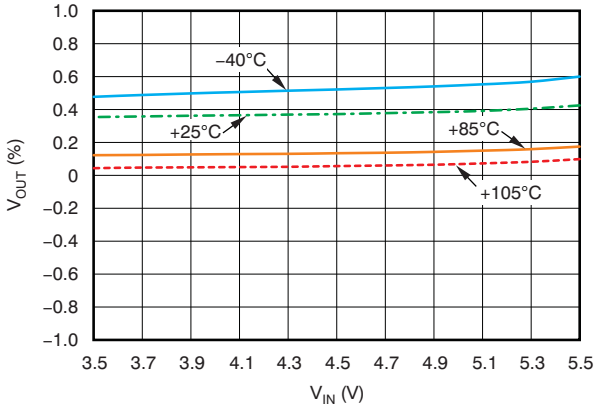
At T_J = –40°C to 105°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, and fixed V_{OUT} test conditions (unless otherwise noted). Typical values at T_J = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT}	DC output accuracy	Nominal	T_J = 25°C		–2%		2%	
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, 100 µA ≤ I_{OUT} ≤ 150 mA		–3.0%	±2.0%	3.0%	
$\Delta V_{O(\Delta VI)}$	Line regulation		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			±1.0%		
$\Delta V_{O(\Delta IO)}$	Load regulation		100 µA ≤ I_{OUT} ≤ 150 mA			±1.0%		
V_{DO}	Dropout voltage(1)		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 150 mA			130	250	mV
I_{LIM}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(nom)}$		150	230	400	mA
I_{GND}	GND pin current		I_{OUT} = 0 mA			420	800	nA
			I_{OUT} = 150 mA			8		µA
I_{EN}	EN pin current		V_{IN} = V_{EN} = 5.5 V			0.07	40	nA
$I_{SHDN(GND)}$	Shutdown current at GND pin		V_{EN} ≤ 0.4 V, $V_{IN(min)}$ ≤ V_{IN} < 5.5 V(2)			18	150	nA
$I_{SHDN(OUT)}$	Shutdown current at OUT pin (leakage)(3)		V_{IN} = open, V_{EN} = 0.4 V, V_{OUT} = $V_{OUT(nom)}$			137	500	nA
$V_{EN(HI)}$	Enable high-level voltage		V_{IN} = 5.5 V		1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low-level voltage		V_{IN} = 5.5 V		0		0.4	V
PSRR	Power-supply rejection ratio		V_{IN} = 4.3 V, V_{OUT} = 3.0 V, I_{OUT} = 150 mA	f = 10 Hz		40		dB
				f = 100 Hz		20		dB
				f = 1 kHz		15		dB
V_n	Output noise voltage		BW = 100 Hz to 100 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA			86		μV_{RMS}
t_{STR}	Startup time(4)		C_{OUT} = 1.0 µF, V_{OUT} = 10% $V_{OUT(nom)}$ to V_{OUT} = 90% $V_{OUT(nom)}$			500		µs
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		°C
T_J	Operating junction temperature				–40		125	°C

(1) V_{DO} is not measured for devices with $V_{OUT(nom)}$ ≤ 2.3 V because minimum V_{IN} = 2.2 V.
(2) $V_{IN(min)}$ = ($V_{OUT(nom)}$ + 0.5 V) or 2.2 V, whichever is greater.
(3) See *Shutdown* in the *Application and Implementation* section for more details.
(4) Time from V_{EN} = 1.2 V to V_{OUT} = 90% ($V_{OUT(nom)}$).

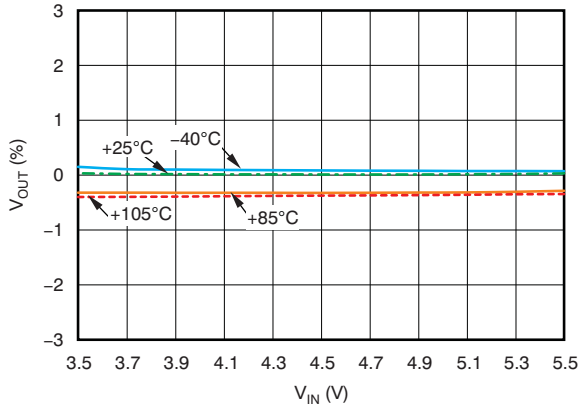
6.6 Typical Characteristics

At T_J = –40°C to 105°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF (unless otherwise noted).



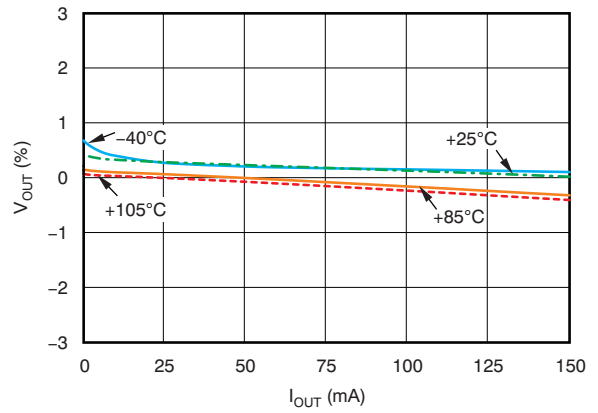
I_{OUT} = 5 mA, $V_{OUT(nom)}$ = 3.0 V

Figure 1. TPS78330 Line Regulation



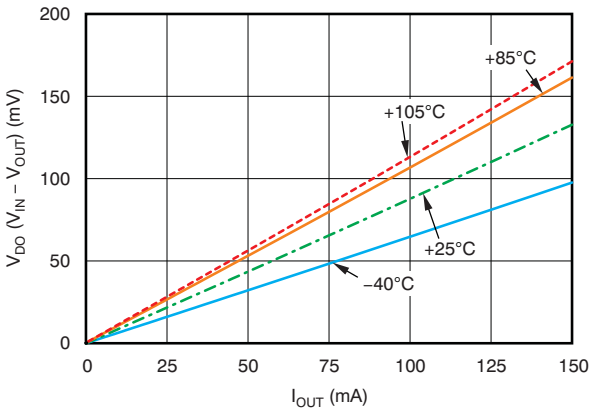
I_{OUT} = 150 mA, $V_{OUT(nom)}$ = 3.0 V

Figure 2. TPS78330 Line Regulation



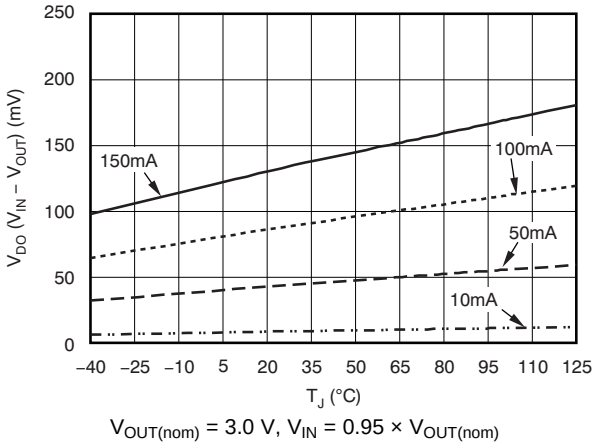
V_{IN} = 3.5 V, $V_{OUT(nom)}$ = 3.0 V

Figure 3. TPS78330 Load Regulation



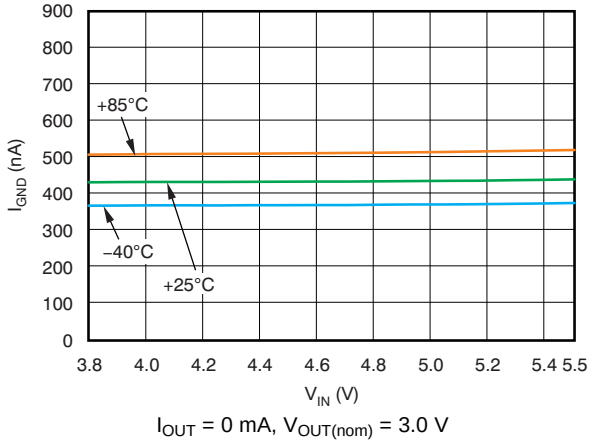
$V_{OUT(nom)}$ = 3.0 V, V_{IN} = 0.95 × $V_{OUT(nom)}$

Figure 4. TPS78330 Dropout Voltage vs Output Current



$V_{OUT(nom)}$ = 3.0 V, V_{IN} = 0.95 × $V_{OUT(nom)}$

Figure 5. TPS78330 Dropout Voltage vs Junction Temperature

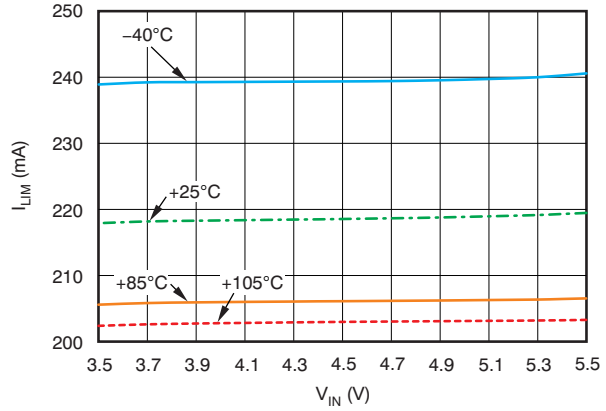


I_{OUT} = 0 mA, $V_{OUT(nom)}$ = 3.0 V

Figure 6. TPS78330 Ground Pin Current vs Input Voltage

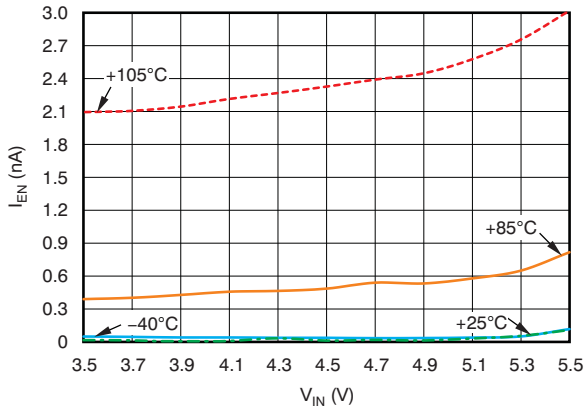
Typical Characteristics (continued)

At T_J = –40°C to 105°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF (unless otherwise noted).



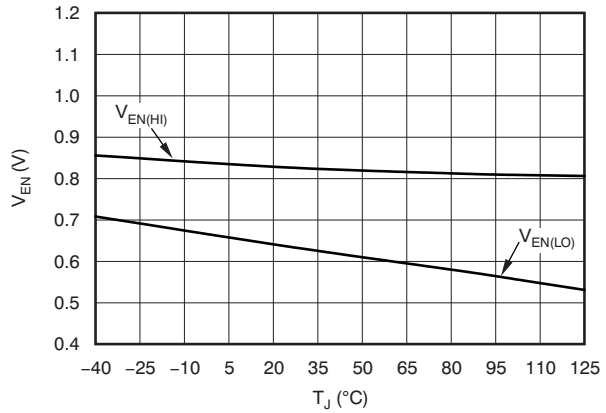
V_{OUT} = 95% $V_{OUT(nom)}$, $V_{OUT(nom)}$ = 3.0 V

Figure 7. TPS78330 Current Limit vs Input Voltage



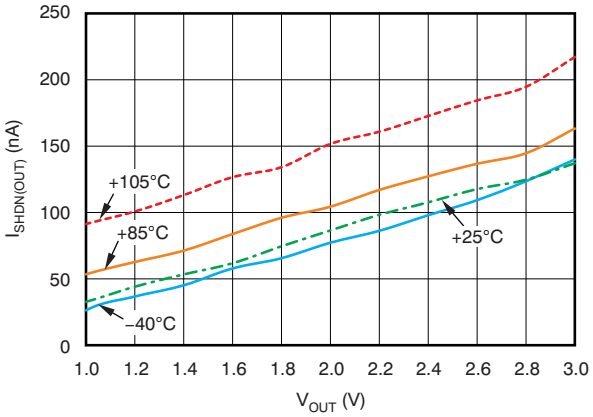
I_{OUT} = 100 µA, $V_{OUT(nom)}$ = 3.0 V

Figure 8. TPS78330 Enable Pin Current vs Input Voltage



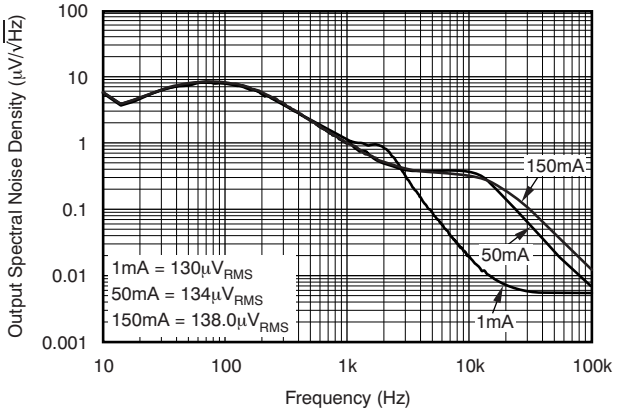
I_{OUT} = 1 mA, $V_{OUT(nom)}$ = 3.0 V

Figure 9. TPS78330 Enable Pin Hysteresis vs Junction Temperature



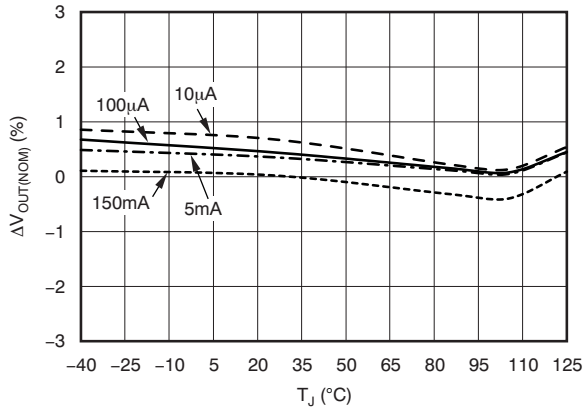
V_{OUT} = $V_{OUT(nom)}$ = 3.0 V, V_{EN} = 0.4 V

Figure 10. TPS78330 Output Current Leakage at Shutdown



C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = 3.5 V, $V_{OUT(nom)}$ = 3.0 V

Figure 11. TPS78330 Output Spectral Noise Density

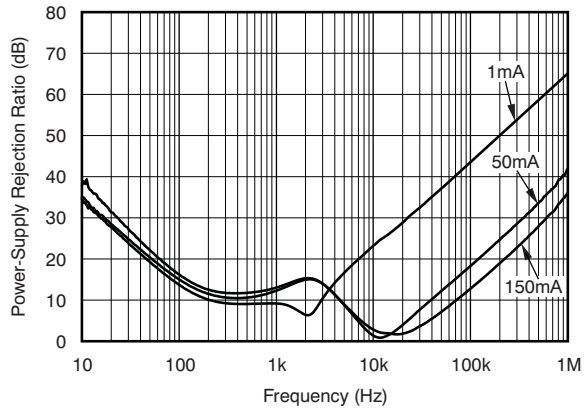


V_{IN} = 3.5 V, $V_{OUT(nom)}$ = 3.0 V

Figure 12. TPS78330 %ΔV_O vs Junction Temperature

Typical Characteristics (continued)

At T_J = –40°C to 105°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF (unless otherwise noted).



V_{IN} = 3.5 V, $V_{OUT(nom)}$ = 3.0 V, C_{OUT} = 2.2 µF

Figure 13. TPS78330 Ripple Rejection vs Frequency

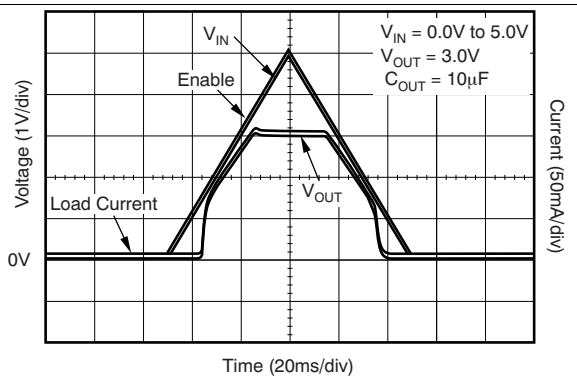


Figure 14. TPS78330 Input Voltage Ramp vs Output Voltage

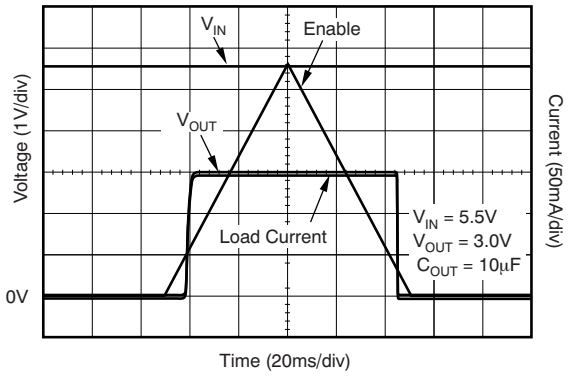


Figure 15. TPS78330 Output Voltage vs Enable (Slow Ramp)

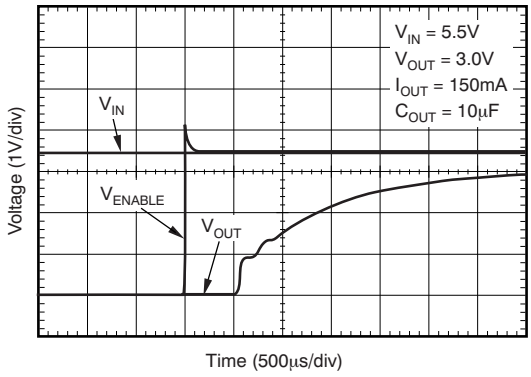


Figure 16. TPS78330 Input Voltage vs Delay to Output

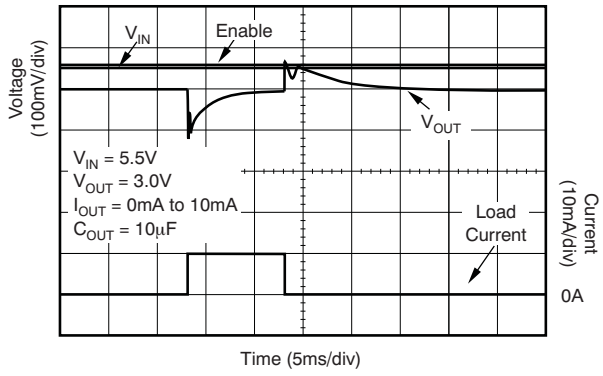


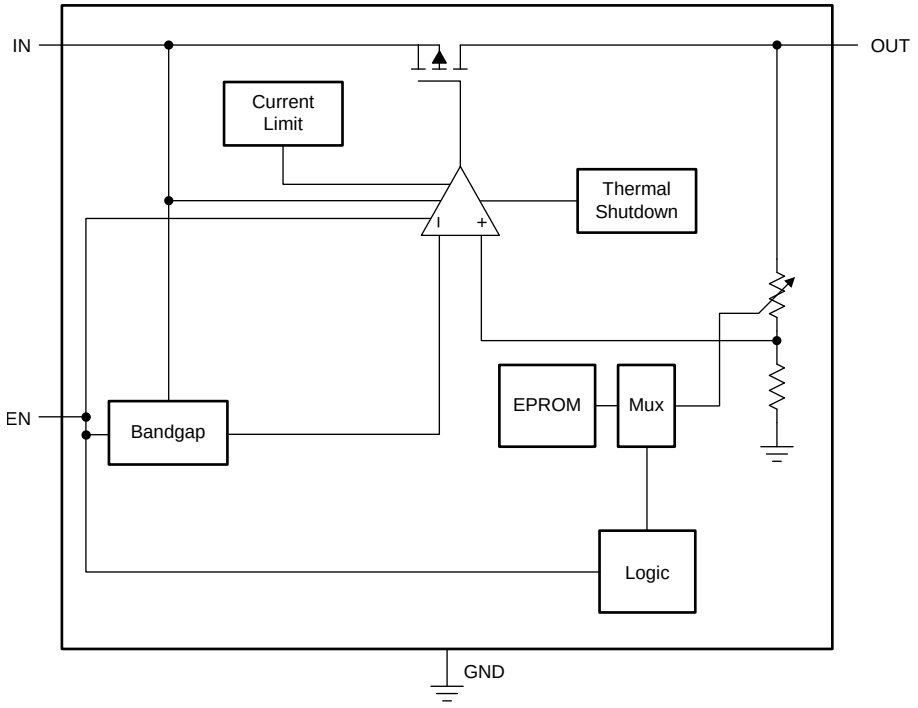
Figure 17. TPS78330 Load Transient Response

7 Detailed Description

7.1 Overview

The TPS783 family of low-dropout regulators (LDOs) designed specifically for battery-powered applications where ultralow quiescent current is a critical parameter. The absence of pulldown circuitry at the output of the LDO provides the flexibility to use the regulator output capacitor as a temporary backup power supply for a short period of time (for example, during battery replacement). The TPS783 family is compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This LDO family is stable with any output capacitor greater than 1.0 µF.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS783 is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS783 family has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting up to the maximum rated current for the device may be required.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, connect EN to the IN pin, as shown in Figure 18.

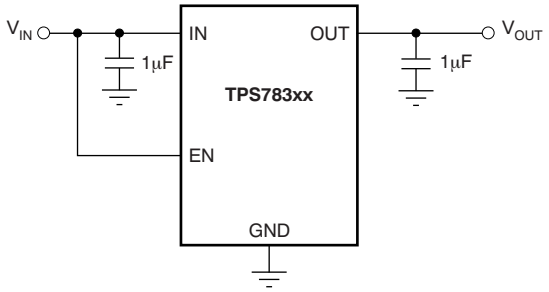


Figure 18. Circuit Showing EN Tied High When Shutdown Capability is Not Required

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > 160°C$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage ($V_{EN} > V_{EN(HI)}$) and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{LIM}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < 160°C$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage ($V_{EN} < V_{EN(LO)}$) or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > 160°C$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS783 family of LDOs is factory-programmable to have a fixed output. Note that during startup or steady-state conditions, do not allow the EN pin voltage to exceed V_{IN} + 0.3 V.

8.2 Typical Application

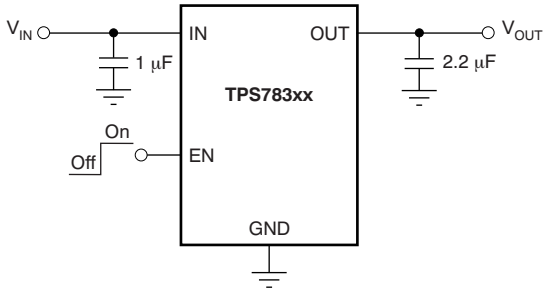


Figure 19. Providing a Low-Power Standby Rail

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

A 0.1-µF input capacitor is necessary for stable operation. Good analog design practice is to connect a 0.1-µF to 1.0-µF, low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source.

The TPS783 family is designed to be stable with standard ceramic capacitors with values of 1.0 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1.0 Ω. With tolerance and dc bias effects, the minimum capacitance for stable operation is 1 µF.

Typical Application (continued)

8.2.1.2 Dropout Voltage

The TPS783 family uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the *Typical Characteristics* section. Refer to application report SLVA207, *Understanding LDO Dropout*, available for download from www.ti.com.

8.2.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response. For more information, see Figure 17.

8.2.1.4 Minimum Load

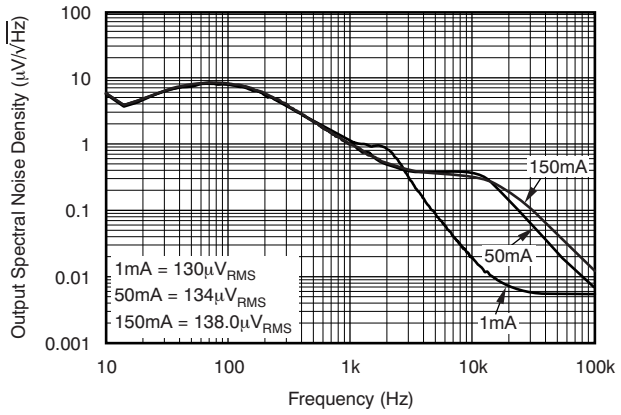
The TPS783 family is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS783 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See Figure 17 for the load transient response.

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

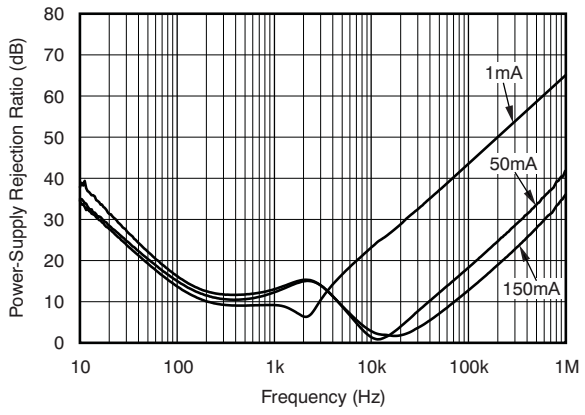
Provide an input supply with adequate headroom to account for dropout and output current to account for the GND pin current, and power the load. Select input and output capacitors based on application needs.

8.2.3 Application Curves



C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = 3.5 V, $V_{OUT(nom)}$ = 3.0 V

Figure 20. TPS78330 Output Spectral Noise Density



V_{IN} = 3.5 V, $V_{OUT(nom)}$ = 3.0 V, C_{OUT} = 2.2 µF

Figure 21. TPS78330 Ripple Rejection vs Frequency

8.3 System Examples

The TPS783 family is designed to be compatible with low-power microprocessors and microcontrollers such as the TI MSP430. In particular, the ultralow quiescent current allows for the TPS783 family to be used in battery-powered applications.

When the system is active, a voltage supervisor enables the regulator and puts the MSP430 into active mode when there is a battery installed and its voltage is above a certain threshold, as shown in Figure 22. The dashed red line indicates the ground current.

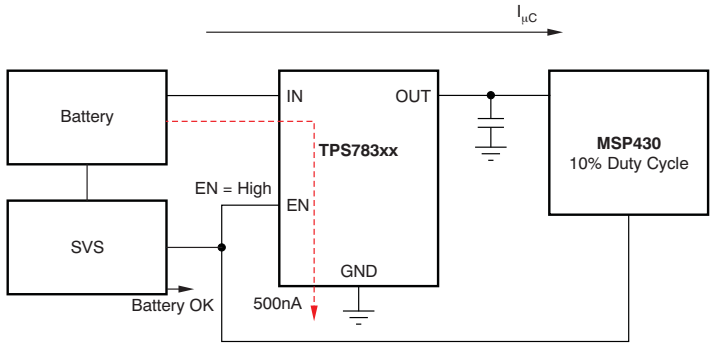


Figure 22. MSP430 Application in Active Mode

When the battery is depleted, the voltage supervisor signals to replace the system battery. After the battery is removed, the voltage supervisor disables the regulator and signals the MSP430 to go into low-power mode. At this moment, the output capacitor functions as a power supply for the MSP430 during the absence of the battery while it is being replaced, as Figure 23 illustrates. The dashed red line indicates the ground current.

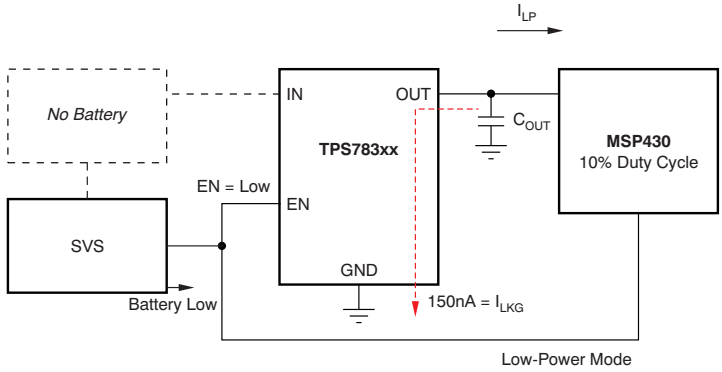


Figure 23. MSP430 Application While Battery is Replaced

Equation 1 shows how to find the required value of the output capacitor (C_{OUT}) to provide an appropriate voltage level to the MSP430 for a given amount of time. This time varies from a few seconds to a few minutes, depending on several factors.

$$C_{OUT} = \frac{t_{MAX}}{\left[\frac{V_{OUT(Nom)} - V_{MIN}}{I_{LKG} + I_{LP}}\right]} \quad (1)$$

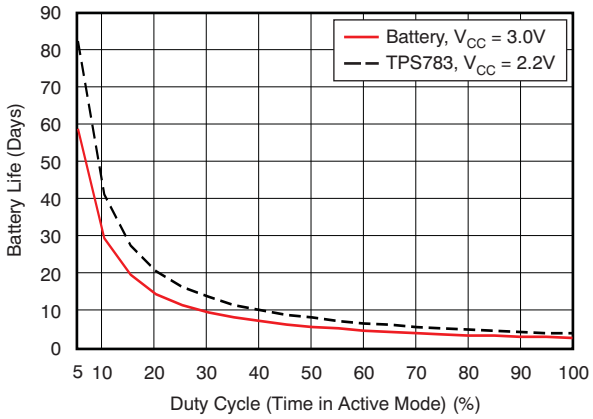
where

- t_{MAX} = maximum time to replace depleted battery
- $V_{OUT(nom)}$ = nominal regulator output equal to initial voltage of capacitor when regulator is disabled
- V_{MIN} = minimum voltage required by MSP430
- $I_{(LKG)}$ = leakage current into regulator output
- $I_{(LP)}$ = current demand from MSP430 in low-power mode

System Examples (continued)

8.3.1 Extending Battery Life in *Keep-Alive* Circuitry Applications for MSP430 and Other Low-Power Microcontrollers

One of the primary advantages of a low quiescent current LDO is the extremely low energy requirement. Counter-intuitively, this requirement enables a longer battery life compared to using only the battery as an unregulated voltage supply for low-power microcontrollers, such as the MSP430. Figure 24 illustrates the characteristic performance of an unregulated, 3.0-V battery supply versus a regulated TPS783 supply for a typical MSP430 application. Table 2 summarizes this comparison.



Calculated with an MSP430F model, operating at 6 MHz.

Figure 24. Battery Life Comparison vs Duty Cycle for MSP430 Application

Table 2. Battery Life Comparison vs Active Mode Time for MSP430 Application

ACTIVE DUTY CYCLE	TPS783xx (NO. OF DAYS)	BATTERY ONLY (NO. OF DAYS)	1-µA LDO (NO. OF DAYS)
Active mode, 1 sec/hour (0.028% duty cycle)	5742	6286	4373
Active mode, 10 sec/hour (0.28% duty cycle)	1320	998	1085
Active mode, 100 sec/hour (2.8% duty cycle)	151	106	148
Active mode, 1000 sec/hour (28% duty cycle)	15.4	10.7	15.4
Active mode, on all the time (100% duty cycle)	4.2	3.0	4.2
CONDITIONS			
Efficiency with V_{BAT} = 3.0 V and V_{CC} = 2.2 V (V_{OUT}/V_{IN})	73%	100%	73%
LDO quiescent current (I_Q)	0.5 µA	0	1 µA
MSP430 active current	2.19 mA	3.09 mA	2.19 mA
MSP430 low-power current	0.5 µA	0.6 µA	0.5 µA

8.3.2 Supercapacitor-Based Backup Power

The very-low leakage current at the LDO output provides a system with the flexibility to use the device output capacitor, or supercapacitor, as a temporary backup power supply. The leakage current going into the regulator output from the output capacitor when the LDO is disabled is typically 170 nA; see Figure 10.

8.4 Do's and Don'ts

Do place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND of the regulator.

Do not exceed the absolute maximum ratings.

9 Power-Supply Recommendations

For best performance, connect a low-output impedance power supply directly to the IN pin of the TPS783. Inductive impedances between the input supply and the IN pin create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the printed circuit board (PCB) with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the output capacitor must be as close as possible to the ground pin of the device to provide a common reference for regulation purposes. High ESR capacitors may degrade PSRR.

10.1.2 Package Mounting

Solder pad footprint recommendations for the TPS783 series are available from the Texas Instruments website at www.ti.com through the TPS783 family product folders.

10.1.3 Thermal Information

10.1.3.1 Thermal Protection

Thermal protection disables the device output when the junction temperature rises to approximately 160°C, allowing the device to cool. After the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 105°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TPS783 family is designed to protect against overload conditions. However, this circuitry is not intended to replace proper heatsinking. Continuously running the TPS783 series into thermal shutdown degrades device reliability.

Layout Guidelines (continued)

10.1.3.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

10.2 Layout Example

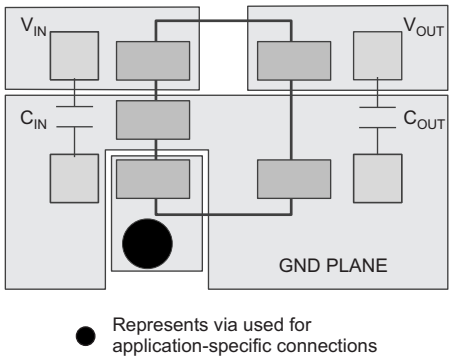


Figure 25. TPS783xx Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS783. The TPS782xxEVM evaluation modules (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS783 is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS783**xxyyyz**	**XX** is the nominal output voltage **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78318DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO	Samples
TPS78318DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO	Samples
TPS78319DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP	Samples
TPS78319DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP	Samples
TPS78326DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB	Samples
TPS78326DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB	Samples
TPS78330DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ	Samples
TPS78330DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ	Samples
TPS78342DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIQ	Samples
TPS78342DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

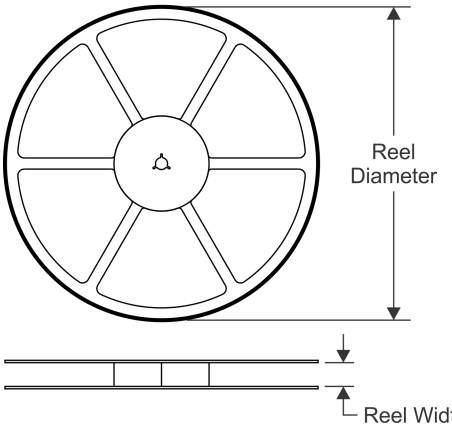
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

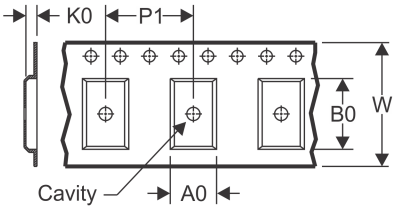
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

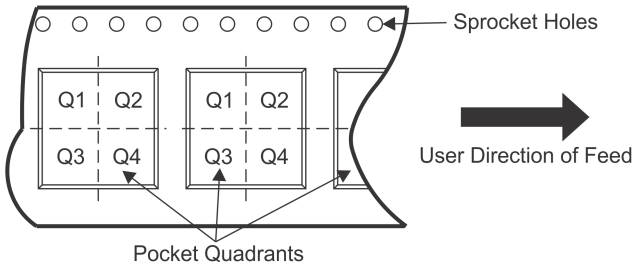


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

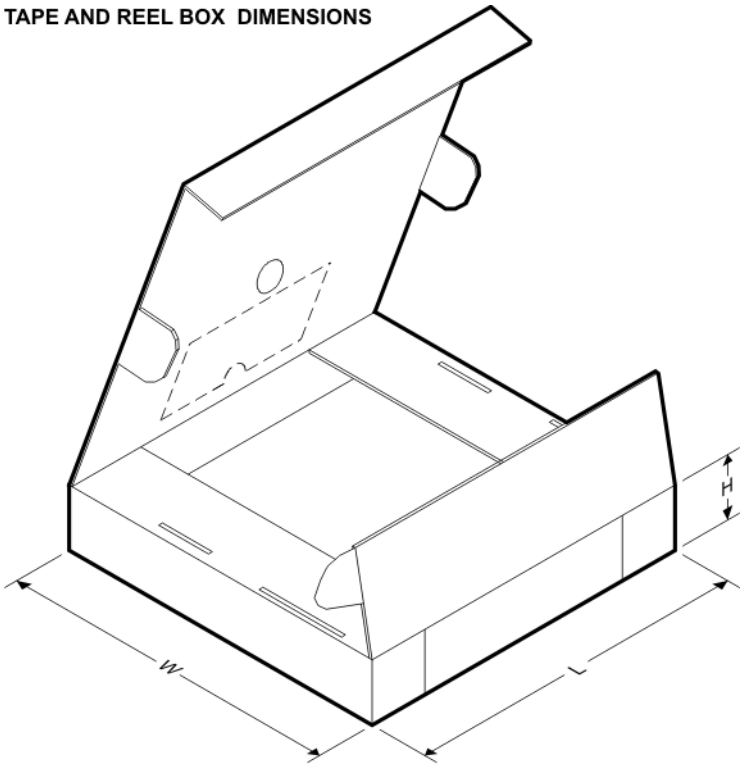
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78318DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78318DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78319DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78319DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78326DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78326DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78330DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78330DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78342DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78342DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

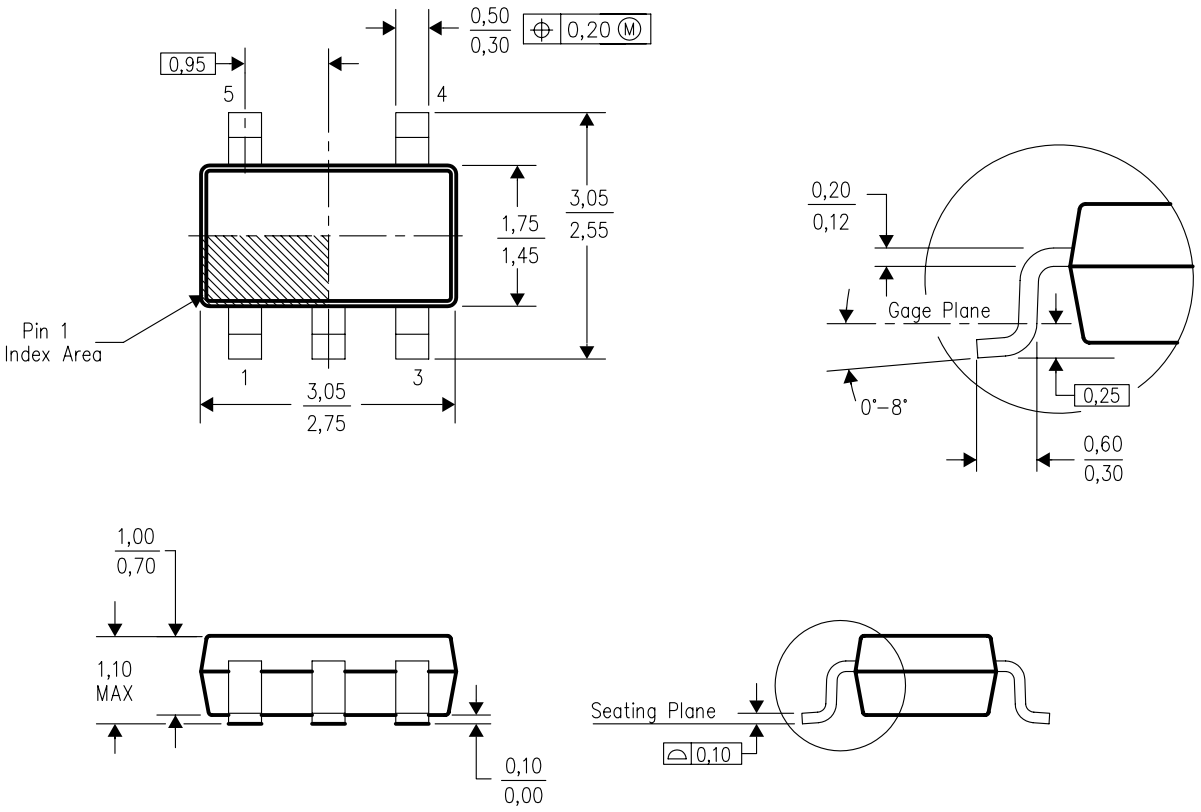
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78318DDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
TPS78318DDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
TPS78319DDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
TPS78319DDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
TPS78326DDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
TPS78326DDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
TPS78330DDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
TPS78330DDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
TPS78342DDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
TPS78342DDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0

DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

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