



THE DATASHEET OF AOD9T40P



General Description

- Trench Power AlphaMOS-II technology
- Low $R_{DS(ON)}$
- Low C_{iss} and C_{rss}
- High Current Capability
- RoHS and Halogen Free Compliant

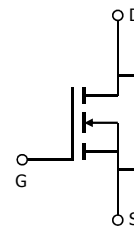
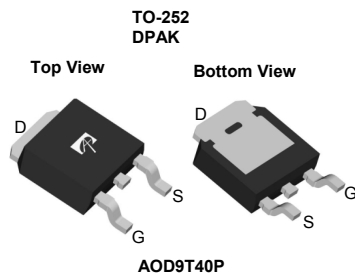
Applications

- General Lighting for LED and CCFL
- AC/DC Power supplies for Industrial, Consumer, and Telecom

Product Summary

$V_{DS} @ T_{j,max}$	500V
I_{DM}	26A
$R_{DS(ON),max}$	< 0.8 Ω
$Q_{g,typ}$	9nC
$E_{oss} @ 320V$	1.5 μ J

100% UIS Tested
 100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD9T40P	TO-252	Tape & Reel	2500

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	6.6
		$T_C=100^\circ\text{C}$	4.2
Pulsed Drain Current ^C	I_{DM}	26	A
Avalanche Current ^C L=1mH	I_{AR}	9	A
Repetitive avalanche energy ^C	E_{AR}	40	mJ
Single pulsed avalanche energy ^H	E_{AS}	252	mJ
MOSFET dv/dt ruggedness	dv/dt	50	V/ns
Peak diode recovery dv/dt		5	
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	83
		Derate above 25 $^\circ\text{C}$	0.7
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	40	50	$^\circ\text{C}/\text{W}$
Maximum Case-to-sink ^A	$R_{\theta CS}$	-	0.5	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case ^{D,F}	$R_{\theta JC}$	1.3	1.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	400			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		500		
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.39		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =400V, V _{GS} =0V			1	μA
		V _{DS} =320V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3	4	5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =4A		0.67	0.8	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =4A		5.5		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				6.6	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C				26	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		530		pF
C _{oss}	Output Capacitance				30	
C _{o(er)}	Effective output capacitance, energy related ^I	V _{GS} =0V, V _{DS} =0 to 320V, f=1MHz		29		pF
C _{o(tr)}	Effective output capacitance, time related ^J				51	
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		2.8		pF
R _g	Gate resistance	f=1MHz		2.3		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =320V, I _D =6.6A		9	18	nC
Q _{gs}	Gate Source Charge			4		nC
Q _{gd}	Gate Drain Charge			1.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =200V, I _D =6.6A, R _G =25Ω		21		ns
t _r	Turn-On Rise Time			26		ns
t _{D(off)}	Turn-Off DelayTime			26		ns
t _f	Turn-Off Fall Time			14		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =6.6A, dI/dt=100A/μs, V _{DS} =100V		233		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =6.6A, dI/dt=100A/μs, V _{DS} =100V		2.1		μC

A. The value of R_{qJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

H. L=60mH, I_{AS}=2.9A, V_{DD}=150V, R_G=10Ω, Starting T_J=25° C.

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

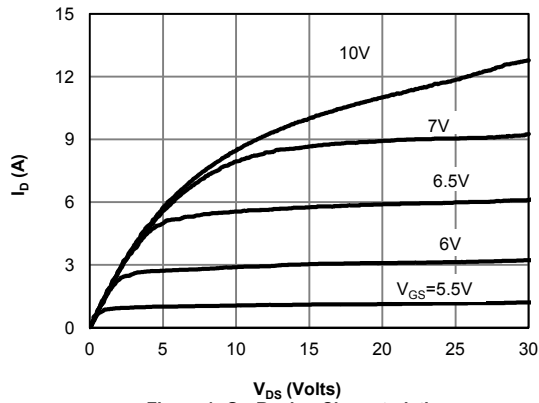


Figure 1: On-Region Characteristics

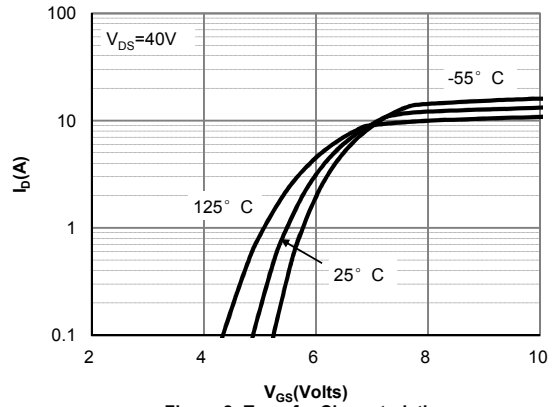


Figure 2: Transfer Characteristics

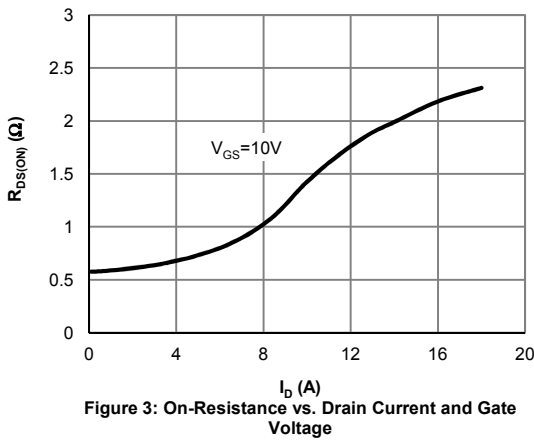


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

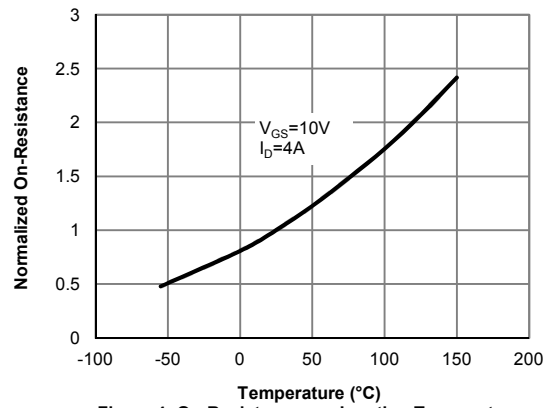


Figure 4: On-Resistance vs. Junction Temperature

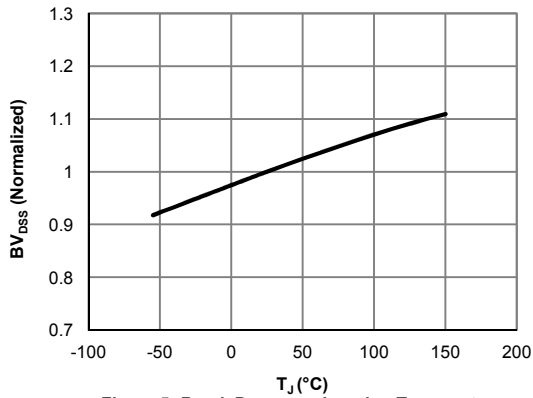


Figure 5: Break Down vs. Junction Temperature

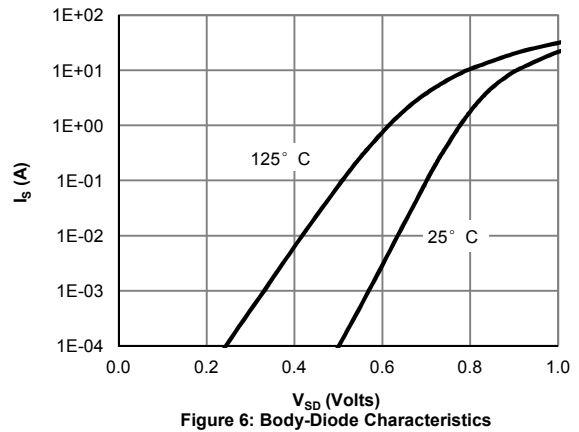


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

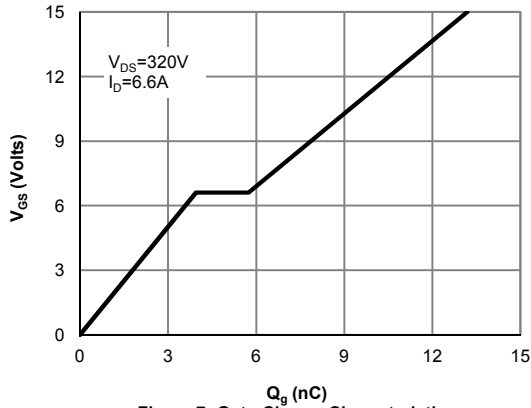


Figure 7: Gate-Charge Characteristics

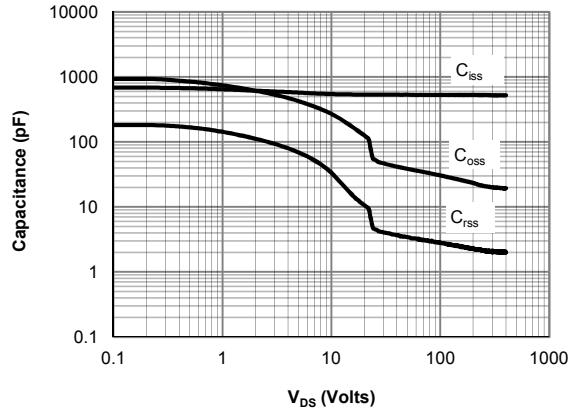


Figure 8: Capacitance Characteristics

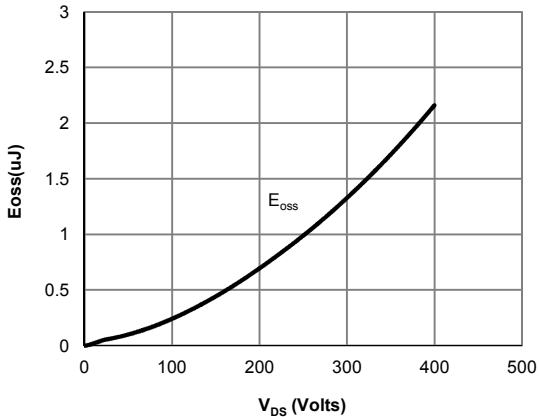


Figure 9: Coss stored Energy

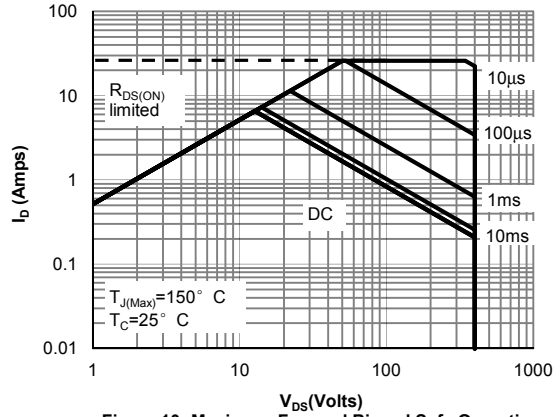


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

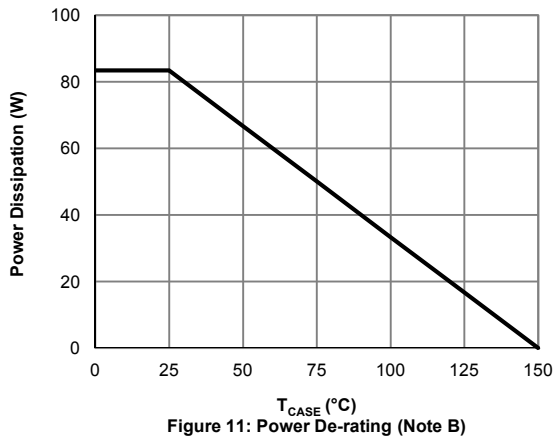


Figure 11: Power De-rating (Note B)

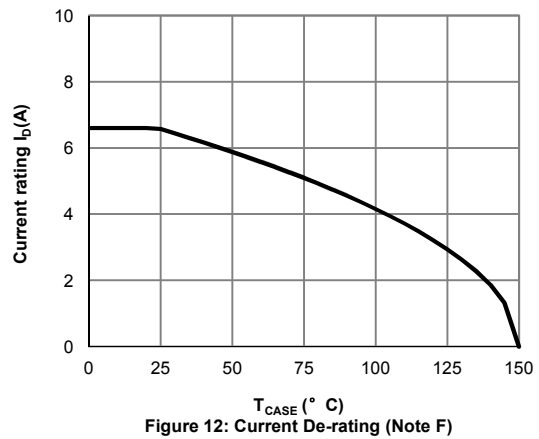


Figure 12: Current De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

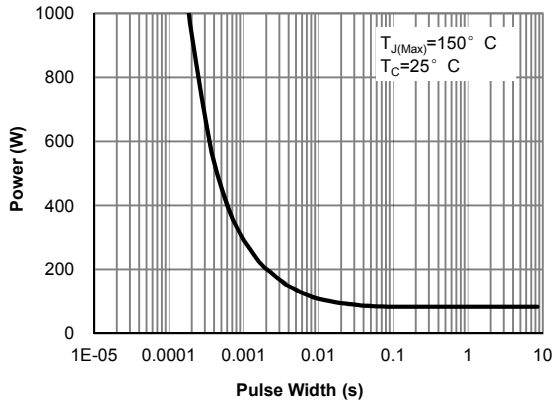


Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)

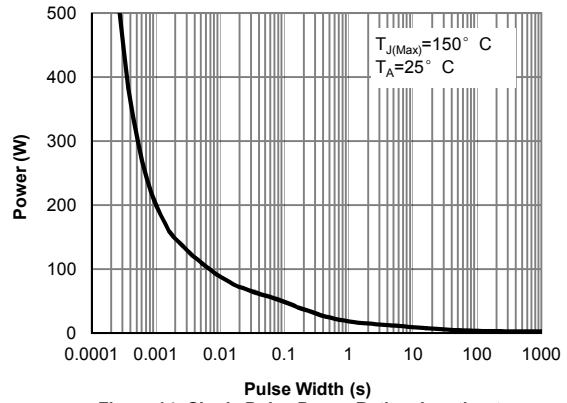


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

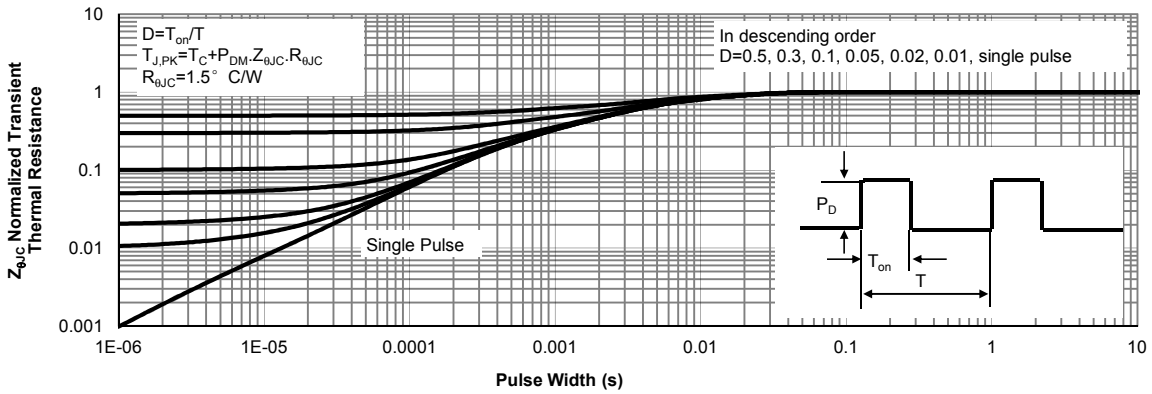


Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

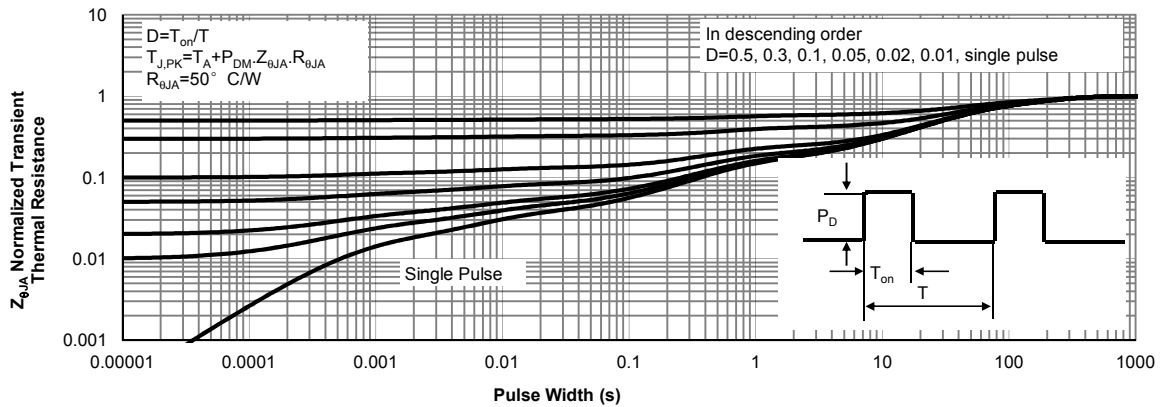
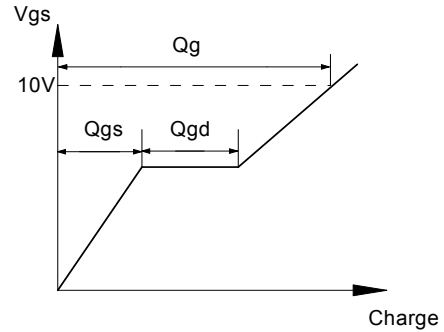
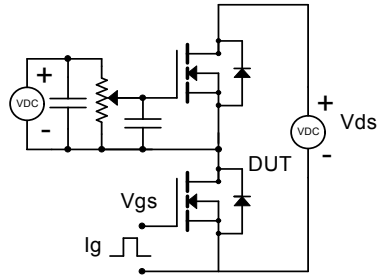
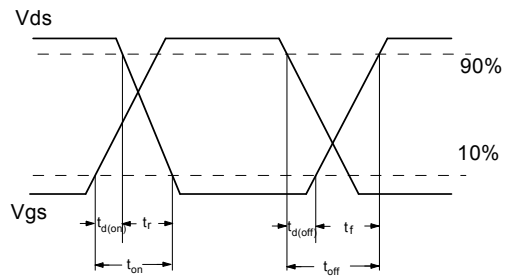
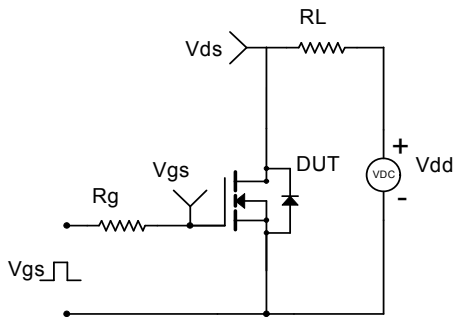


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

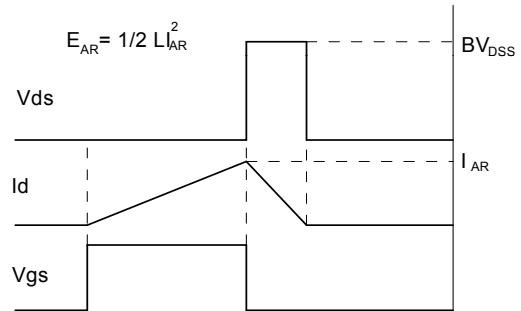
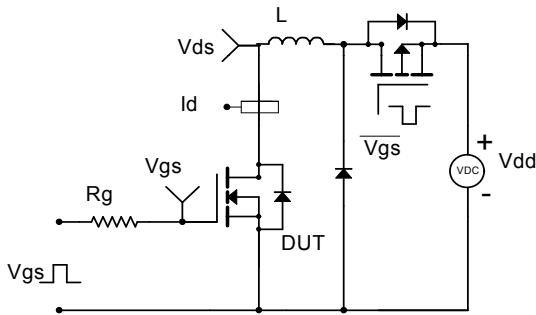
Gate Charge Test Circuit & Waveform



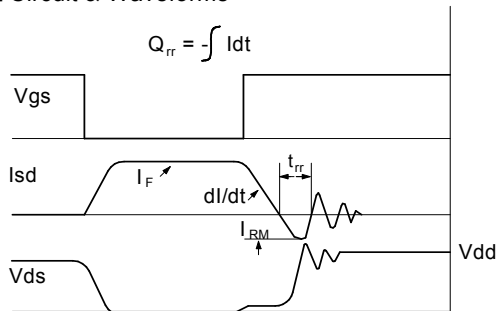
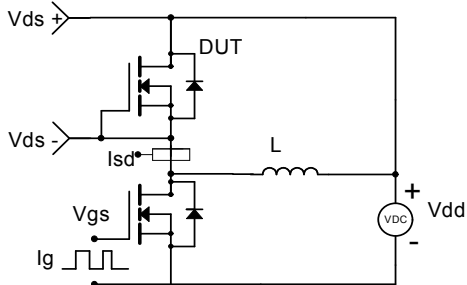
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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