



**THE DATASHEET OF
SI2303-TP**





Micro Commercial Components

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SI2303

P-Channel Enhancement Mode Field Effect Transistor

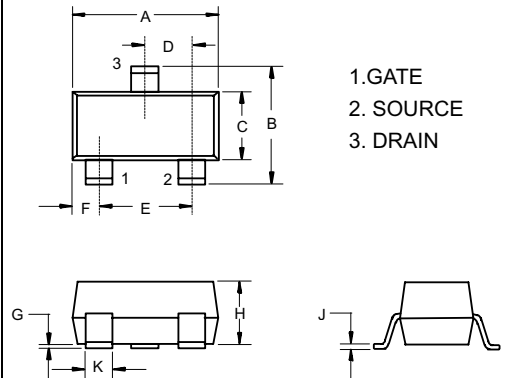
Features

- Halogen free available upon request by adding suffix "-HF"
- -30V, -2.6A, $R_{DS(ON)}=130m\Omega$ @ $V_{GS}=-10V$
- -30V, -2.0A, $R_{DS(ON)}=180m\Omega$ @ $V_{GS}=-4.5V$
- High dense cell design for extremely low $R_{DS(ON)}$
- Rugged and reliable
- Lead free product is acquired
- SOT-23 Package
- Marking Code: S3
- Epoxy meets UL 94 V-0 flammability rating
- Moisture Sensitivity Level 1

Maximum Ratings @ 25°C Unless Otherwise Specified

Symbol	Parameter	Rating	Unit
V_{DS}	Drain-source Voltage	-30	V
I_D	Drain Current-Continuous	-3	A
I_{DM}	Drain Current-Pulsed ^a	-10	A
V_{GS}	Gate-source Voltage	± 20	V
P_D	Total Power Dissipation	0.25	W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^b	500	$^{\circ}C/W$
T_J	Operating Junction Temperature	-55 to +150	$^{\circ}C$
T_{STG}	Storage Temperature	-55 to +150	$^{\circ}C$

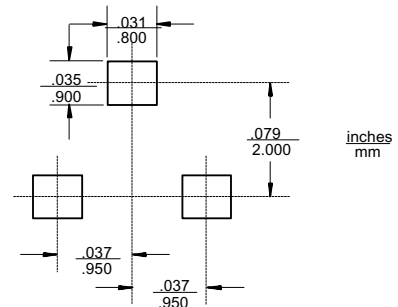
SOT-23



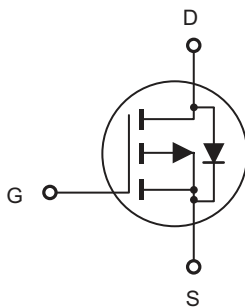
DIMENSIONS

DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.120	2.80	3.04	
B	.083	.104	2.10	2.64	
C	.047	.055	1.20	1.40	
D	.035	.041	.89	1.03	
E	.070	.081	1.78	2.05	
F	.018	.024	.45	.60	
G	.0005	.0039	.013	.100	
H	.035	.044	.89	1.12	
J	.003	.007	.085	.180	
K	.015	.020	.37	.51	

Suggested Solder Pad Layout



Internal Block Diagram



**Electrical Characteristics** $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -10\mu A$	-30			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$			-1	μA	
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA	
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA	
On Characteristics^c							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V	
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -2.6A$			130	m Ω	
		$V_{GS} = -4.5V, I_D = -2.0A$			180	m Ω	
Forward Transconductance	g_{FS}	$V_{DS} = -10V, I_D = -1.7A$		2.4		S	
Dynamic Characteristics^d							
Input Capacitance	C_{iss}	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		226		pF	
Output Capacitance	C_{oss}				87		pF
Reverse Transfer Capacitance	C_{rss}				19		pF
Switching Characteristics^d							
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -1A,$ $V_{GEN} = -10V, R_G = 6\Omega,$ $R_L = 15\Omega$		9	20	ns	
Turn-On Rise Time	t_r			9	20	ns	
Turn-Off Delay Time	$t_{d(off)}$			18	35	ns	
Turn-Off Fall Time	t_f			6	20	ns	
Total Gate Charge	Q_g	$V_{DS} = -15V, I_D = -1.7A,$ $V_{GS} = -10V$		5.8	10	nC	
Gate-Source Charge	Q_{gs}			0.8		nC	
Gate-Drain Charge	Q_{gd}			1.5		nC	
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -1.25A$			-1.2	V	

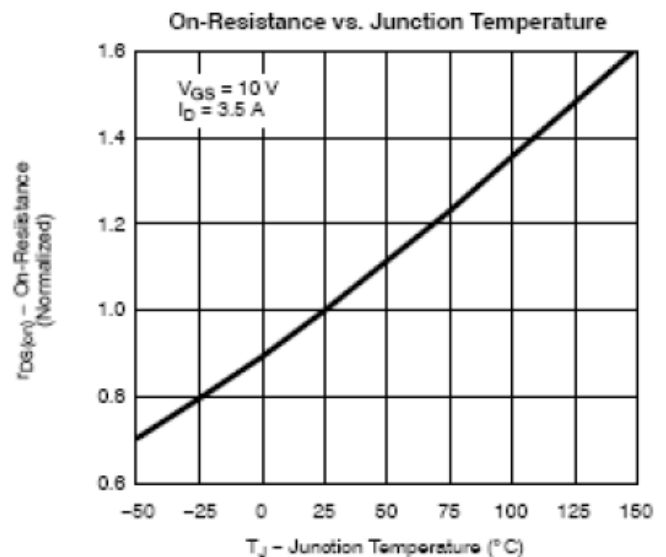
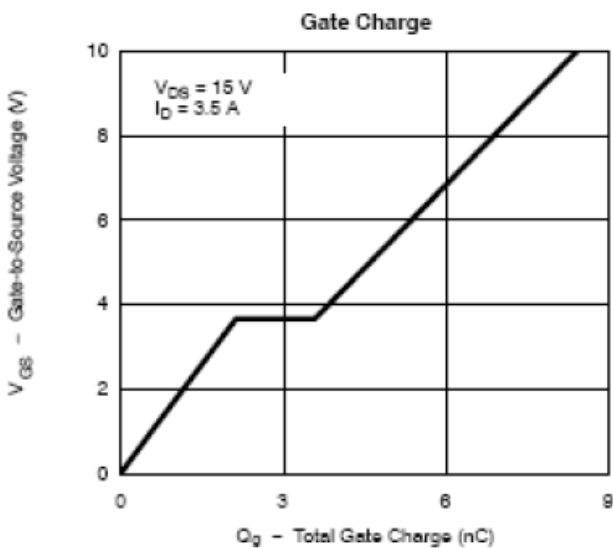
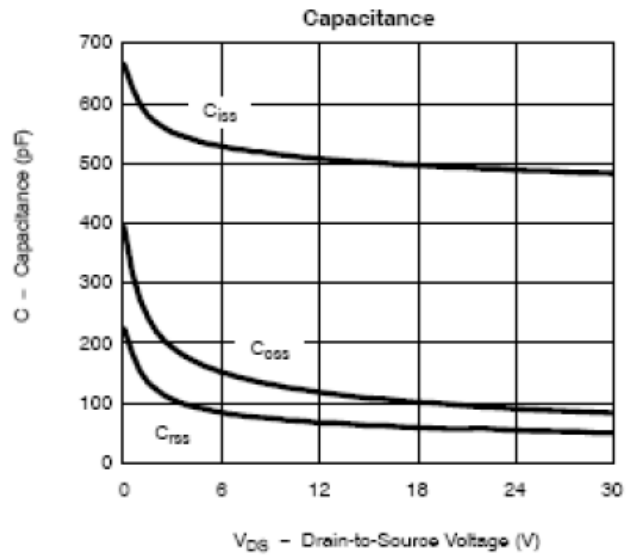
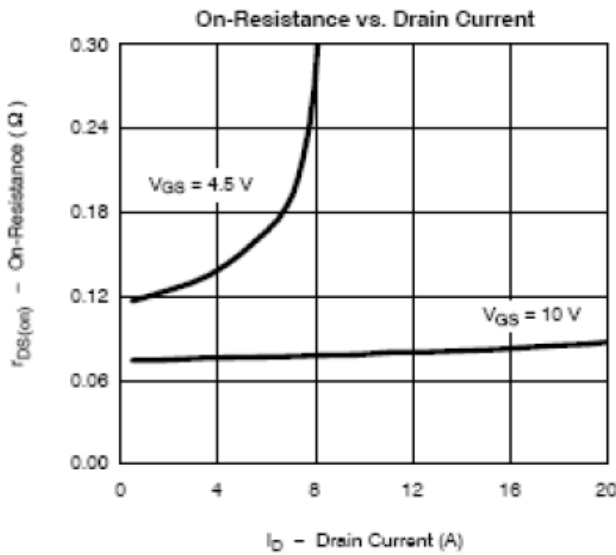
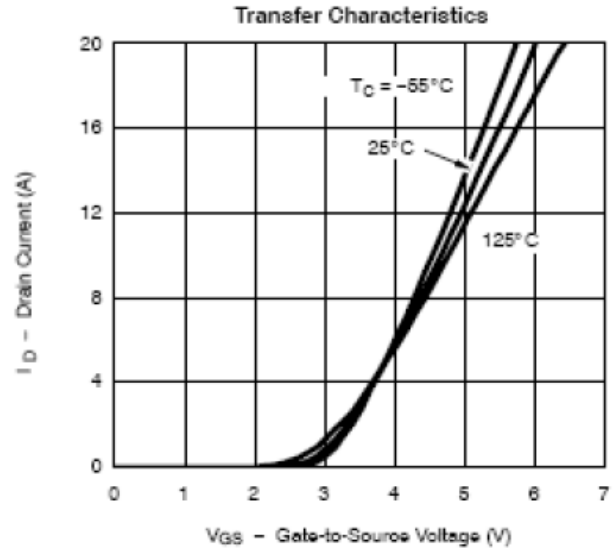
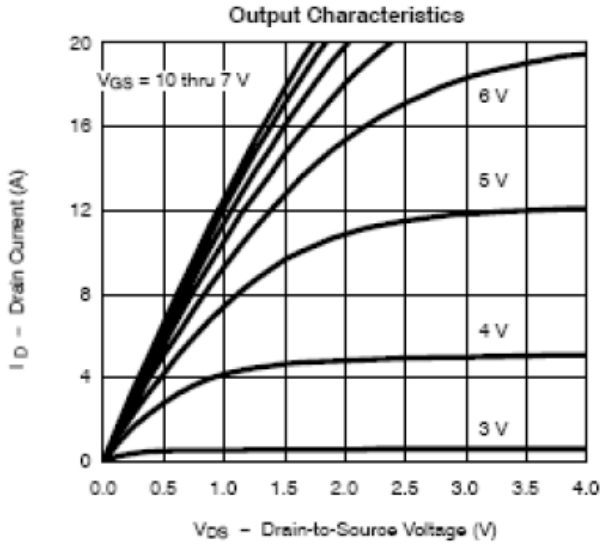
Notes :

a. Repetitive Rating : Pulse width limited by maximum junction temperature.

b. Surface Mounted on FR4 Board, $t < 10\text{ sec.}$ c. Pulse Test : Pulse Width $< 300\mu s$, Duty Cycle $< 2\%$.

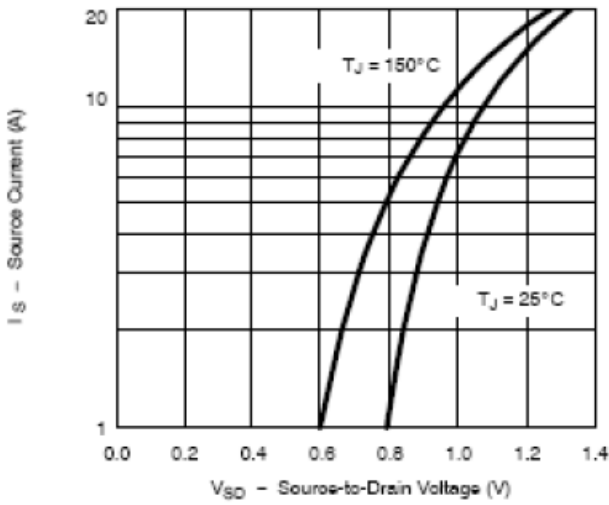
d. Guaranteed by design, not subject to production testing.

Typical characteristics

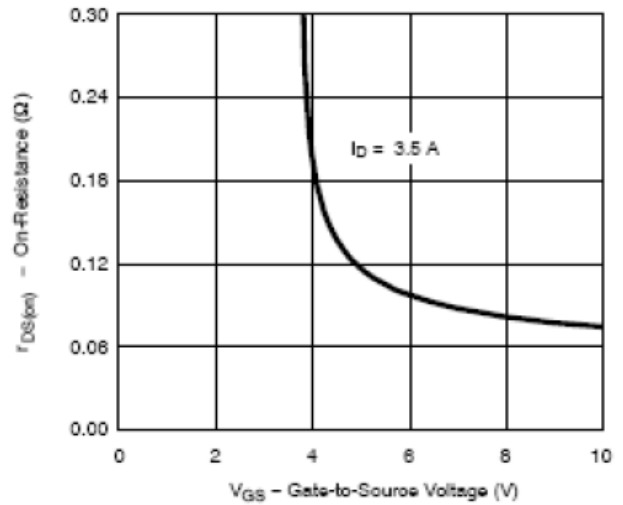


Typical characteristics

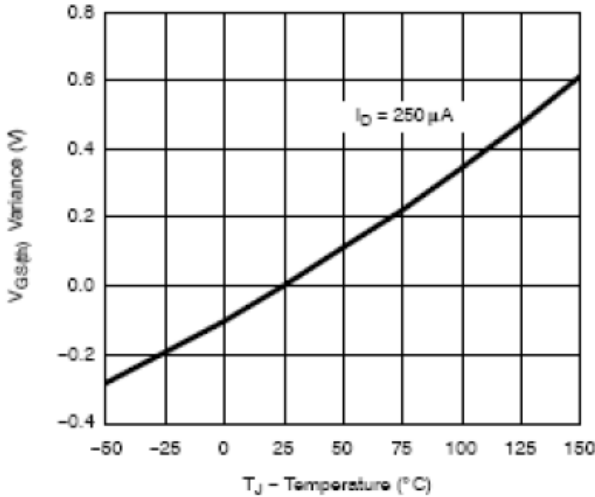
Source-Drain Diode Forward Voltage



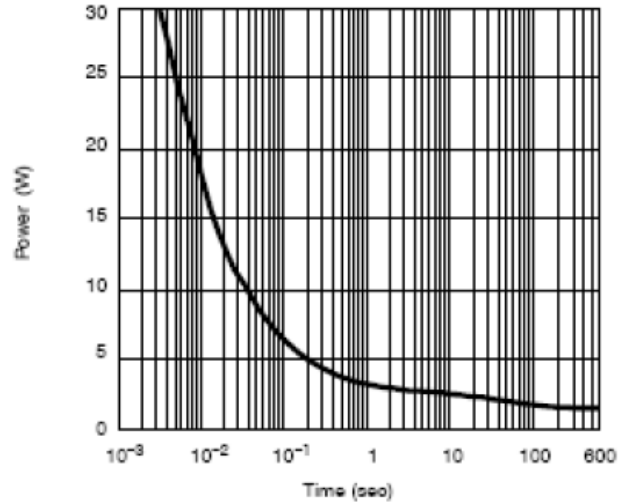
On-Resistance vs. Gate-to-Source Voltage



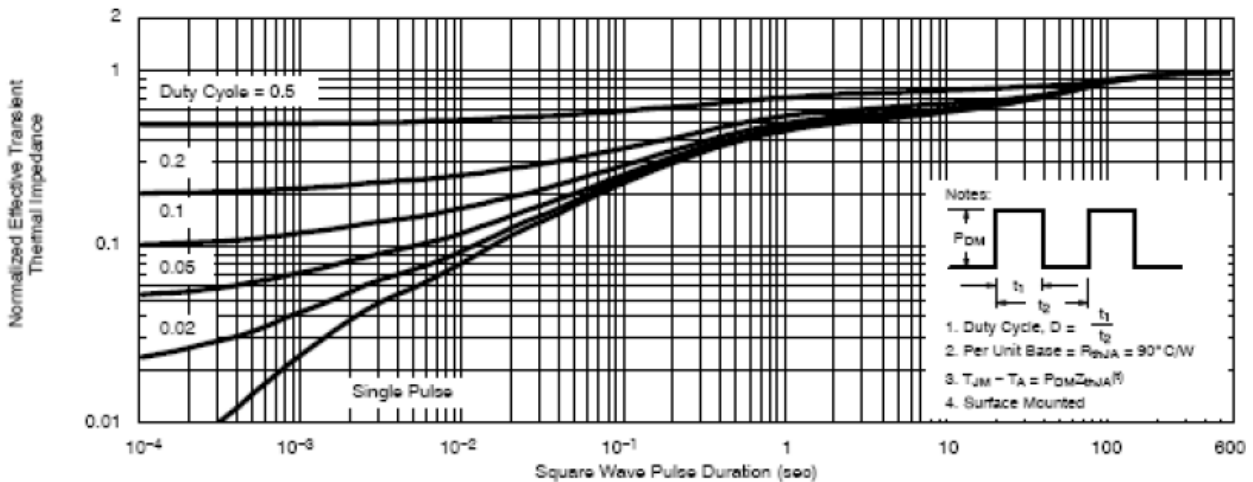
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient





TM

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Ordering Information :

Device	Packing
Part Number-TP	Tape&Reel: 3Kpcs/Reel

Note : Adding "-HF" suffix for halogen free, eg. Part Number-TP-HF

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