



**THE DATASHEET OF  
AP3421DNTR-G1**



**1.3MHz, Dual 1.0A Synchronous Step-down Converters**
**AP3421/A/B**

## General Description

The AP3421/A/B is a fully integrated dual output voltage regulator. The two converters are current mode and internally compensated. The converters include integrated control and synchronous rectifier switches. The outputs are both rated for up to 1A. Both outputs are adjustable using external resistors.

The step-down converters operate at 1.3MHz fixed switching frequency under normal load and in a pulse skipping mode for light loads. The switching clock is shifted 180° for SW2. The E/S pin provides an enable function and allows the converter to be synchronized to an external clock. With E/S held low, the AP3421/A/B draws less than 10µA current.

In the start-up sequence, the VO1 output is designed to precede the VO2 output. The two outputs have controlled start-up sequence.

Power On Reset (POR) function is provided by means of an open-drain output present on the POR pin. The POR function monitors V<sub>MON</sub>, FB1 and FB2, and pulls low if any of these begin to drop out. The POR is internally deglitched and provides a delayed recovery/reset time.

The AP3421/A/B provides peak over-current protection, short circuit protection and thermal shutdown. Discharge-Before-Turn-On discharges the outputs completely before soft-starting to always bring them up in the proper sequence at start-up or after a POR (For AP3421/A only).

The AP3421/A/B is available in DFN-3×3-10 package.

## Features

- V<sub>O1</sub>=1.8 to 3.6V at 1A
- V<sub>O2</sub>=1.0 to 3.6V at 1A
- Switching Frequency: 1.3MHz
- 180° Phase Shifted Switching
- No Rectifier Diode Required
- Optional External Clocking (2× Clock Required)
- Light Load Pulse Skipping
- Enable/Sleep State
- Internal Soft-start
- Open-drain Power On Reset Monitors Input and Outputs
- Discharge-Before-Turn-On (For AP3421/A)
- Pre-bias Function (For AP3421B)
- Peak Over Current Protection
- Short Circuit Protection
- Over Temperature Shutdown

## Applications

- Hard Disk Drivers
- Set Top Boxes

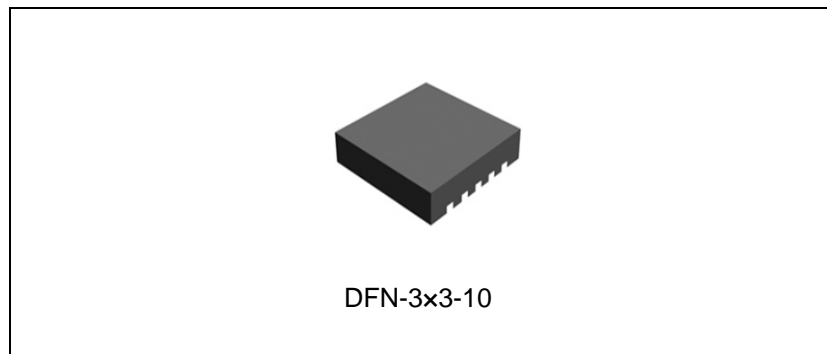


Figure 1. Package Type of AP3421/A/B

## Pin Configuration

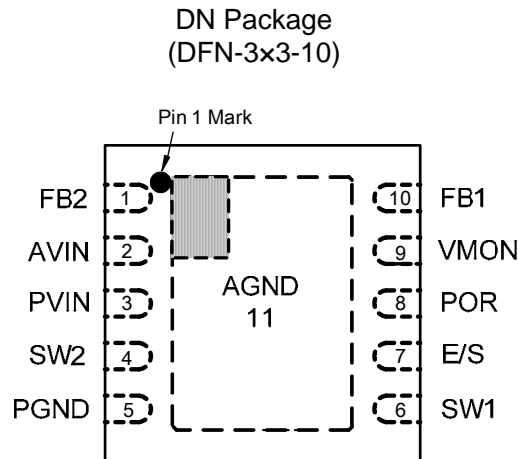


Figure 2. Pin Configuration of AP3421/A/B (Top View)

## Pin Description

Pin Number	Pin Name	Function
1	FB2	Feedback from VO2. Connect voltage divider to the load side of VO2 output inductor-capacitor filter
2	AVIN	Analog power input. Connect a 1 $\mu$ F ceramic capacitor between this pin and AGND
3	PVIN	Control MOSFET switch power input. Connect a 10 $\mu$ F ceramic capacitor between this pin and PGND, as close to the IC as possible
4	SW2	VO2 synchronous buck switching output. Connect to VO2 inductor
5	PGND	Power ground connection. Synchronous rectifier MOSFET source. Provide a star connection between this pin, VO1, VO2 filter capacitor returns, VIN input capacitor return, and AGND. Keep the star connection as close to the IC as possible
6	SW1	VO1 synchronous buck switching output. Connect to VO1 inductor
7	E/S	Enable/Synchronization. Pulling this pin high statically enables the IC and pulling the pin low statically will shut down the IC. Applying a pulse to this pin will synchronize SW1 and SW2 switching frequency to $\frac{1}{2}$ the external clock frequency

**1.3MHz, Dual 1.0A Synchronous Step-down Converters      AP3421/A/B****Pin Description (Continued)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Function</b>
8	POR	Power on reset output pin. Monitors FB1, FB2 output voltage levels and $V_{IN}$ . POR is pulled low if an output voltage drop is detected on FB1 or FB2 or $V_{IN}$ , and is Hi-Z during normal operation
9	VMON	Voltage monitor-supervisor for one external voltage (could be input voltage). The POR output is triggered if this output falls below the VMON threshold
10	FB1	Feedback from VO1. Connect voltage divider to the load side of VO1 output inductor-capacitor filter
11	AGND	Signal ground connection. Provide a star connection between this pin and PGND pin

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**Functional Block Diagram**

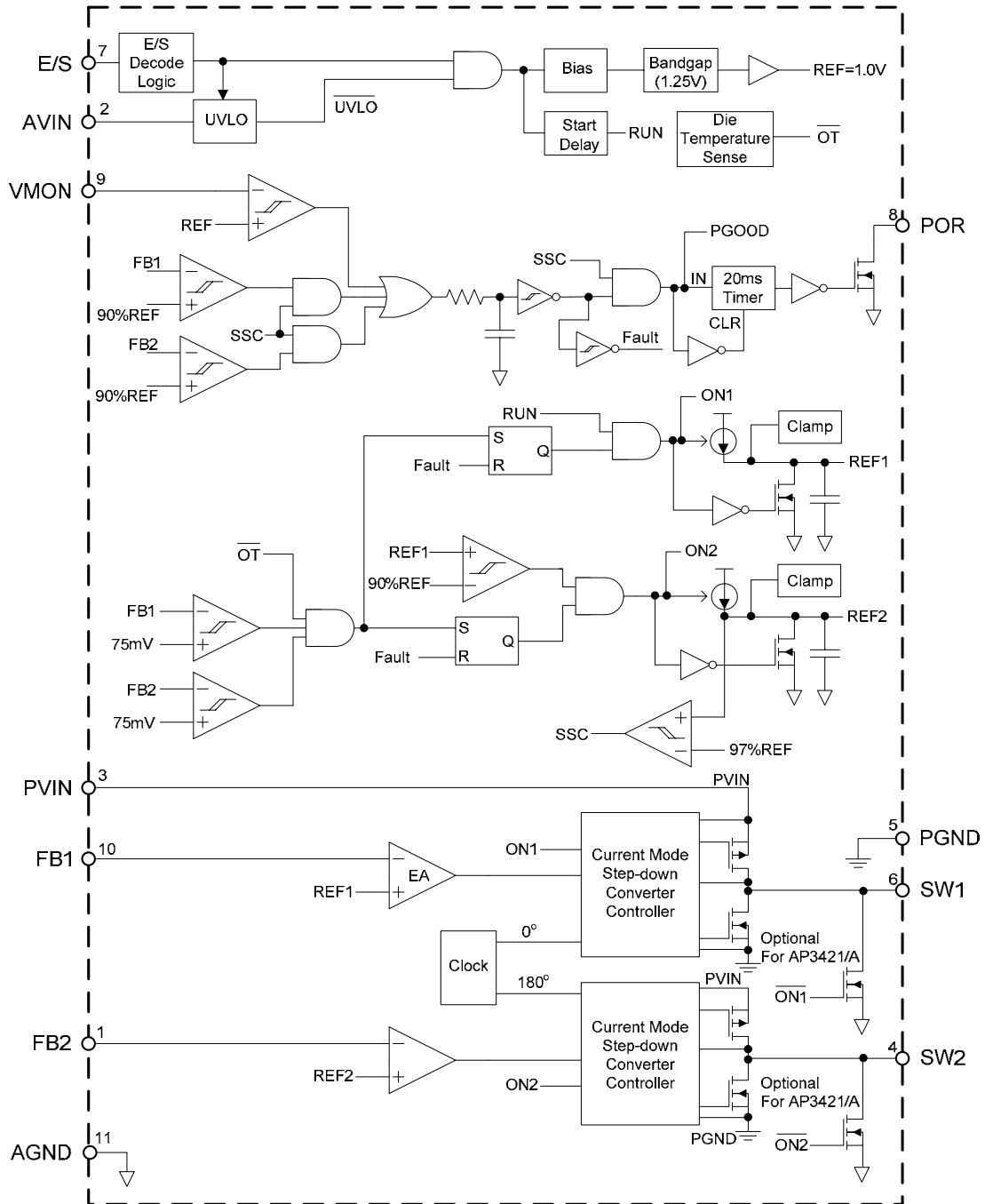


Figure 3. Functional Block Diagram of AP3421/A/B





**1.3MHz, Dual 1.0A Synchronous Step-down Converters AP3421/A/B**

**Electrical Characteristics**

$V_{IN}=V_{E/S}=5V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Operating Input Voltage	$V_{IN}$	AP3421	4.5	5.0	5.5	V	
		AP3421A/B	3.0	3.3	5.5		
Supply Current	$I_{CC}$	$V_{FB1}=V_{FB2}=1.2V$			1.0	mA	
Shutdown Supply Current	$I_{SHDN}$	$V_{E/S}=0V, V_{IN}=5.0V$			10	$\mu A$	
Under Voltage Lockout Threshold		Rising Edge	AP3421	3.0	3.5	4.0	V
			AP3421A/B	2.4	2.7	3.0	
Under Voltage Lockout Hysteresis	$V_{HUVLO}$			300		mV	
POR Threshold V <sub>MON</sub>	$V_{VMON\_POR}$	$V_{VMON}$ Falling	0.97	1.00	1.03	V	
Feedback Voltage	$V_{FB1}, V_{FB2}$		0.975	1.0	1.025	V	
Switch Current Limit	$I_{LIM1}$		1.2	1.6		A	
	$I_{LIM2}$		1.2	1.6			
Oscillator Frequency	$f_{OSC1}, f_{OSC2}$		1.0	1.30	1.60	MHz	
Soft-start Time	$t_{SS\_FB1}$		0.5	1.0	2.0	ms	
POR Threshold FB1	$V_{FB1\_POR}$	FB11Falling1	86	89	92	% $V_{FB1}$	
POR Threshold FB2	$V_{FB2\_POR}$	FB21Falling1	86	89	92	% $V_{FB2}$	
Discharge Complete Threshold (AP3421/A)	$V_{FB1\_DCT}$	FB1 Level Where Discharge Cycle Is Terminated	50	75	100	mV	
E/S Pin Threshold	$V_{EN\_L}$		0.6			V	
	$V_{EN\_H}$				1.5		
Frequency Lock-in Range	$f_{E/S\_MIN}$	$f_{SWITCHING}=50\% \times f_{E/S}$ When Externally Clocked			1.5	MHz	
	$f_{E/S\_MAX}$		3.0				
POR Assert Delay Time	$t_{POR\_DELAY}$	Fault Flag Set to POR Pull Low	10	25	40	$\mu s$	
POR Release Delay Time	$t_{POR\_HOLD}$	Fault Flag Reset to POR Hi-Z State	10	20	30	ms	
POR Low Voltage	$V_{POR\_LOW}$	POR Sinking 4mA			300	mV	
VO2 Start Threshold (AP3421/A)	$V_{FB1\_ST}$	FB1 Rising Voltage for FB2 to Initiate Soft-start	86	89	92	% $V_{FB1}$	
SW1, SW2 Discharge Resistance	$R_{STOP\_SW1,2}$	Discharge Resistance for SW1, SW2	15	30	45	$\Omega$	
Internal MOSFET on Resistance	AP3421, AP3421A/B	$R_{DS\_SW1\_U}$	$V_{IN}=5.0V$		277	m $\Omega$	
		$R_{DS\_SW2\_U}$	$I_{SW}=100mA$		260		
		$R_{DS\_SW1\_L}$	$V_{IN}=5.0V$		249		
		$R_{DS\_SW2\_L}$	$I_{SW}=-100mA$		160		
	AP3421A/B	$R_{DS\_SW1\_U}$	$V_{IN}=3.3V$		300		
		$R_{DS\_SW2\_U}$	$I_{SW}=100mA$		280		
		$R_{DS\_SW1\_L}$	$V_{IN}=3.3V$		260		
		$R_{DS\_SW2\_L}$	$I_{SW}=-100mA$		180		
Thermal Shutdown Threshold	$T_{OTSD}$			160		$^{\circ}C$	
Thermal Shutdown Hysteresis	$T_{HYS}$		10	20	30	$^{\circ}C$	



**1.3MHz, Dual 1.0A Synchronous Step-down Converters**      **AP3421/A/B**

**Typical Performance Characteristics**

$V_{IN}=V_{E/S}=5V$ ,  $V_{O1}=2.5V$ ,  $V_{O2}=1.2V$ ,  $L1=L2=3.3\mu H$ ,  $C1=C3=10\mu F$ ,  $C2=C2'=10\mu F$ ,  $T_A=25^\circ C$ , unless otherwise specified.

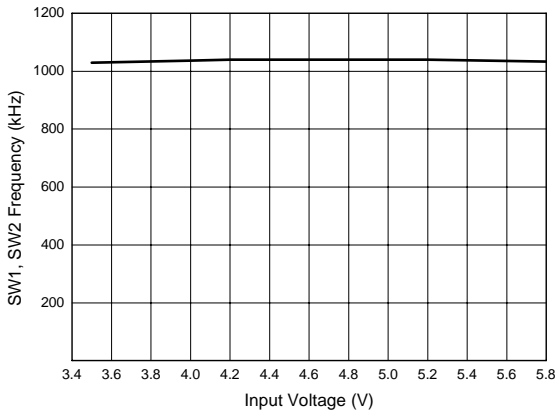


Figure 4. SW1, SW2 Frequency vs. Input Voltage

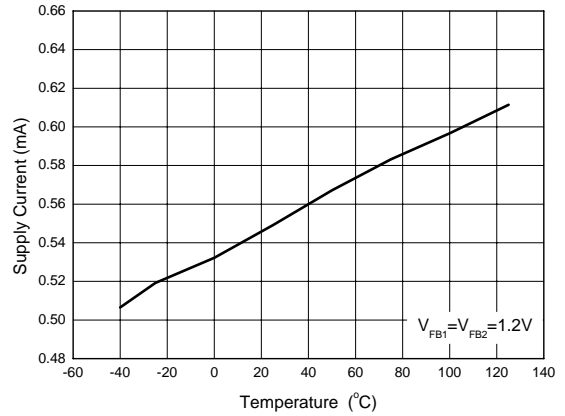


Figure 5. Supply Current vs. Temperature

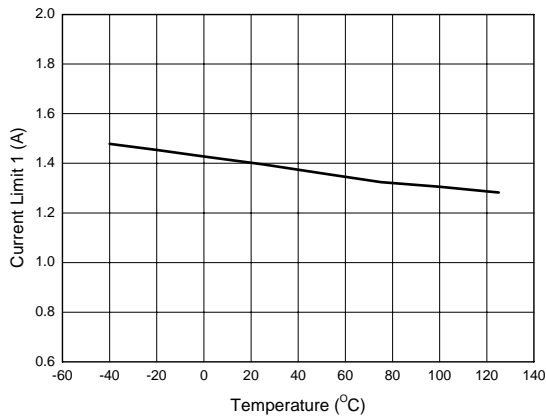


Figure 6. Current Limit 1 vs. Temperature

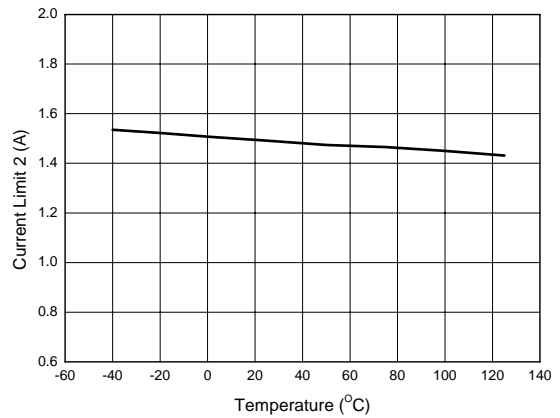


Figure 7. Current Limit 2 vs. Temperature



**1.3MHz, Dual 1.0A Synchronous Step-down Converters AP3421/A/B**

**Typical Performance Characteristics (Continued)**

$V_{IN}=V_{E/S}=5V$ ,  $V_{O1}=2.5V$ ,  $V_{O2}=1.2V$ ,  $L1=L2=3.3\mu H$ ,  $C1=C3=10\mu F$ ,  $C2=C2'=10\mu F$ ,  $T_A=25^\circ C$ , unless otherwise specified.

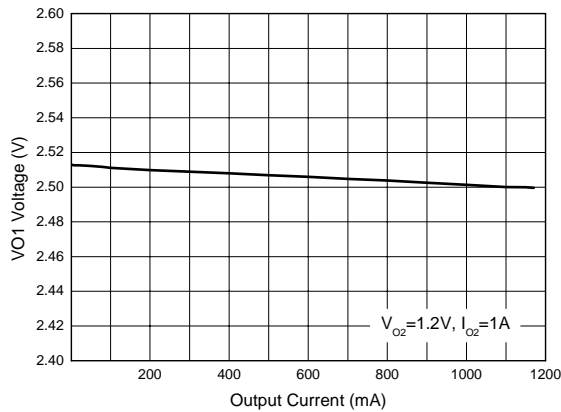


Figure 8. VO1 Voltage vs. Output Current

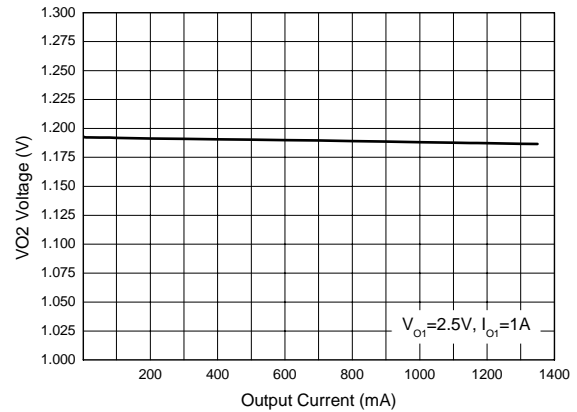


Figure 9. VO2 Voltage vs. Output Current

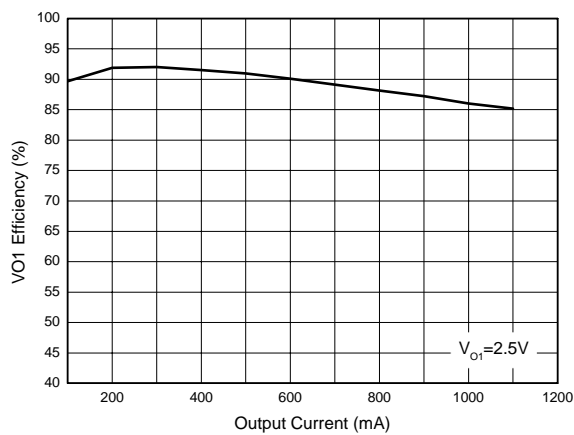


Figure 10. VO1 Efficiency vs. Output Current

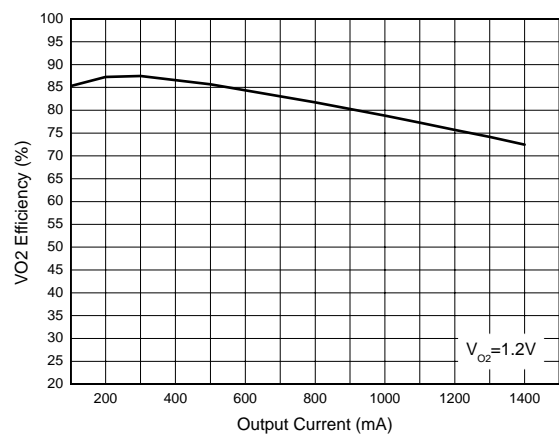


Figure 11. VO2 Efficiency vs. Output Current

**1.3MHz, Dual 1.0A Synchronous Step-down Converters**
**AP3421/A/B**
**Typical Performance Characteristics (Continued)**

$V_{IN}=V_{E/S}=5V$ ,  $V_{O1}=2.5V$ ,  $V_{O2}=1.2V$ ,  $L1=L2=3.3\mu H$ ,  $C1=C3=10\mu F$ ,  $C2=C2'=10\mu F$ ,  $T_A=25^\circ C$ , unless otherwise specified.



Time 4ms/div

Figure 12. Start-up from VIN

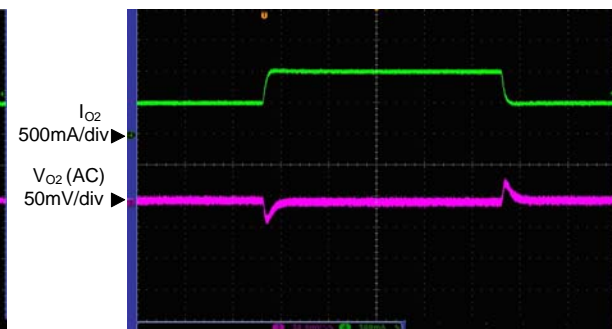


Time 400µs/div

Figure 13. Power-down from VIN



Time 100µs/div

 Figure 14. Load Transient  
 ( $V_O=2.5V$   $I_O=0.5A$  to  $1.0A$ )


Time 100µs/div

 Figure 15. Load Transient  
 ( $V_O=1.2V$   $I_O=0.5A$  to  $1.0A$ )

**1.3MHz, Dual 1.0A Synchronous Step-down Converters**
**AP3421/A/B**
**Typical Performance Characteristics (Continued)**

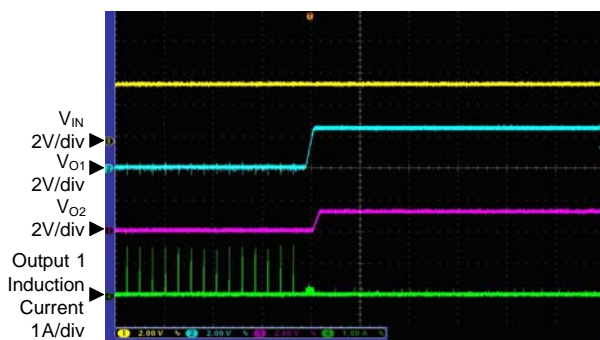
$V_{IN}=V_{E/S}=5V$ ,  $V_{O1}=2.5V$ ,  $V_{O2}=1.2V$ ,  $L1=L2=3.3\mu H$ ,  $C1=C3=10\mu F$ ,  $C2=C2'=10\mu F$ ,  $T_A=25^\circ C$ , unless otherwise specified.


 Time 40 $\mu$ s/div

Figure 16. Short Protection for Output 1

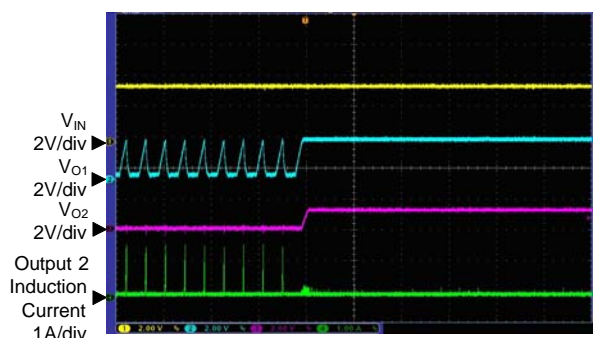

 Time 40 $\mu$ s/div

Figure 17. Short Protection for Output 2



Time 10ms/div

Figure 18. Output 1 Short Recovery



Time 10ms/div

Figure 19. Output 2 Short Recovery



## Application Information

### 1. Operation

The DC-DC converters are current-mode buck converters with a synchronous rectifier and internal compensation. They are designed to be stable with a 1.5 $\mu$ H to 6.8 $\mu$ H inductor value and 10 $\mu$ F to 22 $\mu$ F output capacitor. Both output voltages are resistor programmable. The switching frequency of the converter is fixed and the switches turn on at alternating 180° phase intervals.

The converter operates in 2 possible modes: Continuous Mode (CM), and Pulse Skipping Mode (PSM). CM is the default mode under normal loading. Under light loads, PSM mode occurs, where switching cycles are skipped if the current demand is low.

### 2. Soft-start

The DC-DC converter contains a soft-start function that brings the output voltages up in a slowly increasing ramp with any resistive load from open circuit to 1A (resistive) and any capacitor from 10 $\mu$ F to 22 $\mu$ F. During soft-start, the peak inductor current shall not exceed 750mA until the output voltage reaches 25% of its final value. Current limit shall be active but not trip during soft-start into a rated resistive load. Overshoot voltage during soft-start is limited to 1%.

### 3. Power Sequencing and Enable

When power is applied and if E/S input is asserted (High) or is toggling, the DC-DC converters will enter RUN mode after a short settling period. If the E/S pin is a static low, the IC will enter a SLEEP state where it draws very little input current.

When in RUN mode, if there is no fault condition, the VO1 output (SW1) will be the first output to begin soft-start. When the reference voltage for FB1 reaches approximately 90% of the final value, the VO2 output (SW2) will begin soft-start.

### 4. POR

Under voltage comparators are provided to monitor the output voltages and VMON which could be the input voltage. If any of these voltages falls below its POR threshold, a POR open drain output will turn on which pulls the POR pin low. After the POR condition is cleared, there is a delay of 20ms before

the POR output transistor is turned off; when off the POR pin is high-Z and may be pulled up high with a resistor. The POR function has built-in deglitching. Once the POR is detected, the power supply outputs will be discharged prior to restart using the soft-start/sequencing routine.

### 5.1 Over Current and Short Circuit Protection

The DC-DC converters shall have over current and short circuit protection. Under any load condition, at any time, any value of load resistor (including 0 $\Omega$ ) can be applied to the DC-DC outputs instantaneously and held in place indefinitely without the switch current exceeding the peak current limit and without the IC suffering any permanent damage or loss of performance. The output voltage is allowed to drop under over current or short circuit conditions. Recovery to output voltage regulation is required within 10ms of the instant the loading is reduced to maximum allowable rated load; the output voltage shall not exceed the dynamic load excursion limits ( $\pm 5\%$  excursion) upon recovery. Over current shall not be triggered by a sudden rate of load current change provided the loading does not exceed the output load rating of 1A.

### 6. E/S Function

Enable/Synchronization function. Pulling this pin high statically enables the AP3421/A/B while pulling the pin low statically for longer than 4 $\mu$ s will shut down the AP3421/A/B. Applying a pulse to this pin will synchronize SW1 and SW2 switching frequency to  $\frac{1}{2}$  the external clock frequency. The external frequency lock-in ranges from 1.5MHz to 3.0MHz.

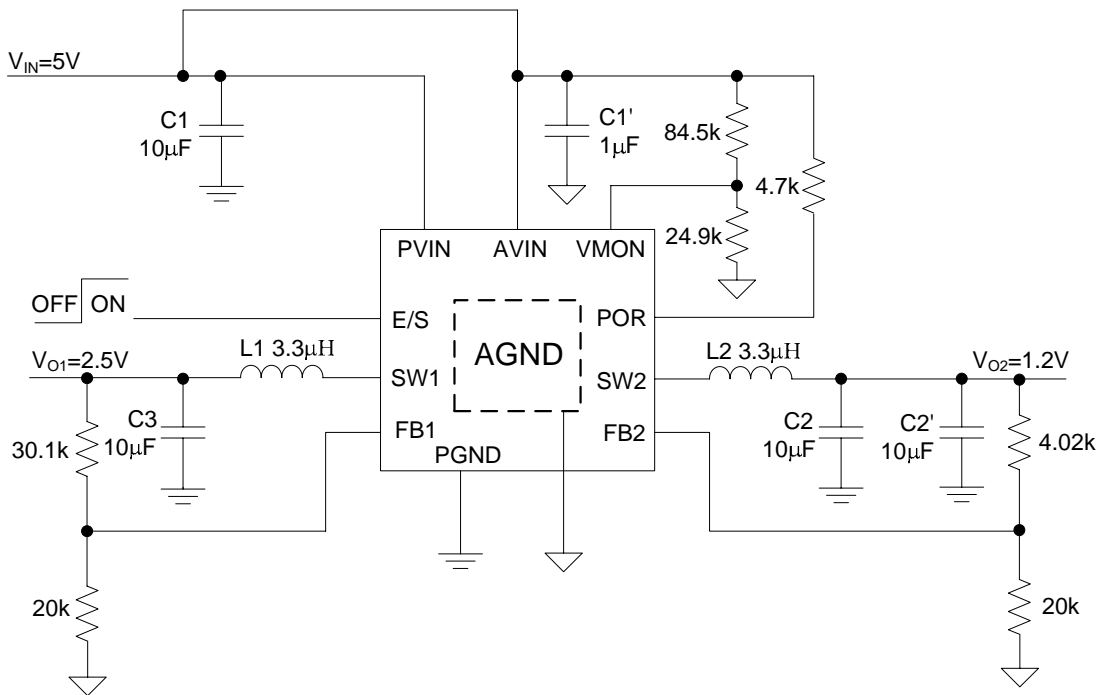
**Typical Application**


Figure 20. Typical Application Circuit of AP3421 (Note 2)

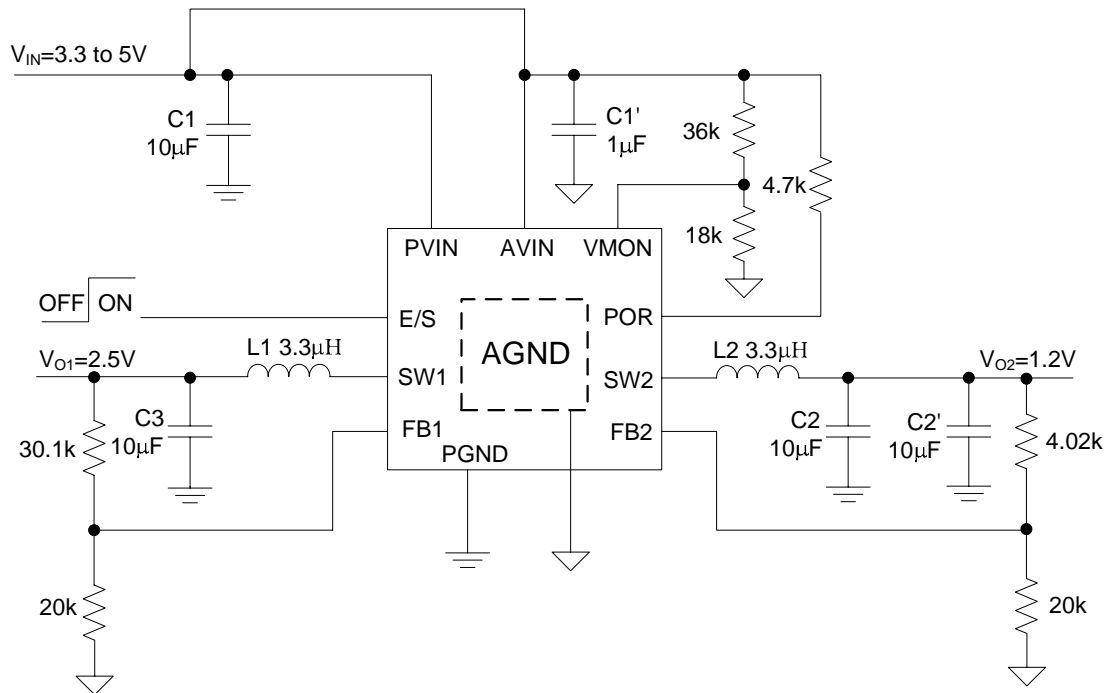
**Typical Application (Continued)**


Figure 21. Typical Application Circuit of AP3421A/B (Note 2)

Note 2: AVIN and PVIN pin should not be connected together directly to avoid disturbance between them in PCB layout:

- 1) Place a 1.0 $\mu$ F capacitor between AVIN pin and AGND for power filtering.
- 2) Place a 10 $\mu$ F capacitor between PVIN pin and PGND for power filtering.



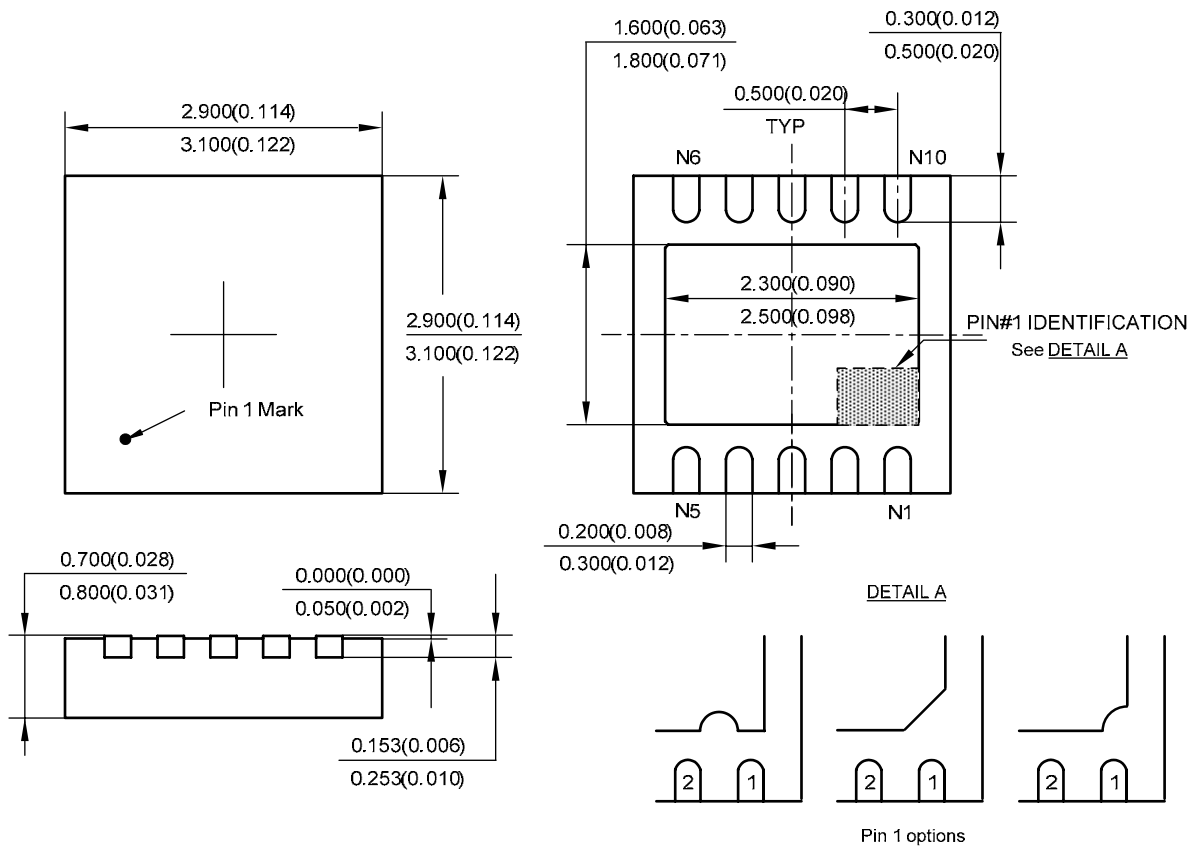
1.3MHz, Dual 1.0A Synchronous Step-down Converters

AP3421/A/B

Mechanical Dimensions

DFN-3x3-10

Unit: mm(inch)





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