



THE DATASHEET OF PMN40UPE,115



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Kind regards,

Team Nexperia

PMN40UPE

20 V, single P-channel Trench MOSFET

13 August 2012

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low threshold voltage
- Fast switching
- Trench MOSFET technology
- 4 kV ESD protection

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

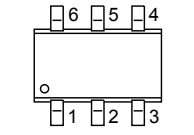
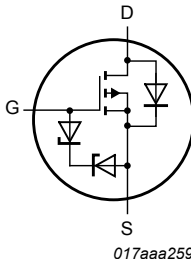
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|---|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_J = 25\text{ °C}$ | - | - | -20 | V |
| V_{GS} | gate-source voltage | | -8 | - | 8 | V |
| I_D | drain current | $V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$ | [1] | - | -6 | A |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = -4.5\text{ V}; I_D = -3\text{ A}; T_J = 25\text{ °C}$ | - | 37 | 43 | m Ω |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|---|--|
| 1 | D | drain |  <p>TSOP6 (SOT457)</p> |  <p>017aaa259</p> |
| 2 | D | drain | | |
| 3 | G | gate | | |
| 4 | S | source | | |
| 5 | D | drain | | |
| 6 | D | drain | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PMN40UPE | TSOP6 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMN40UPE | WD |

5. Limiting values

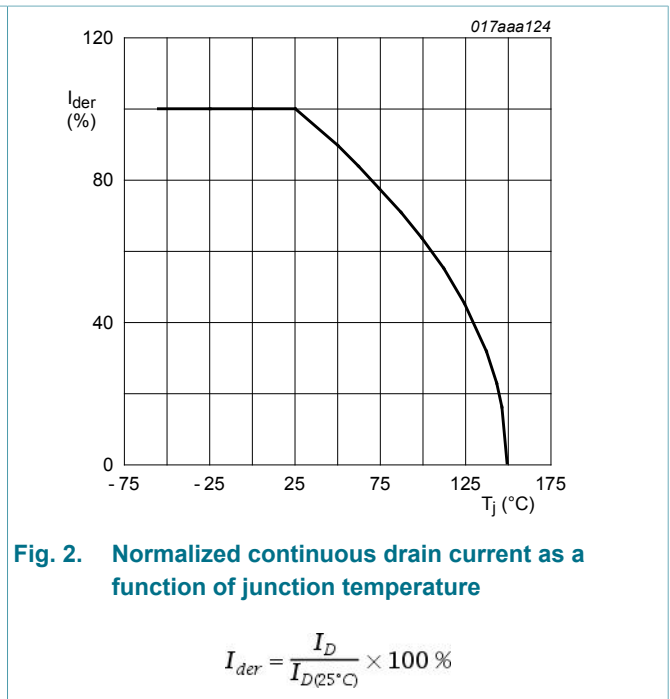
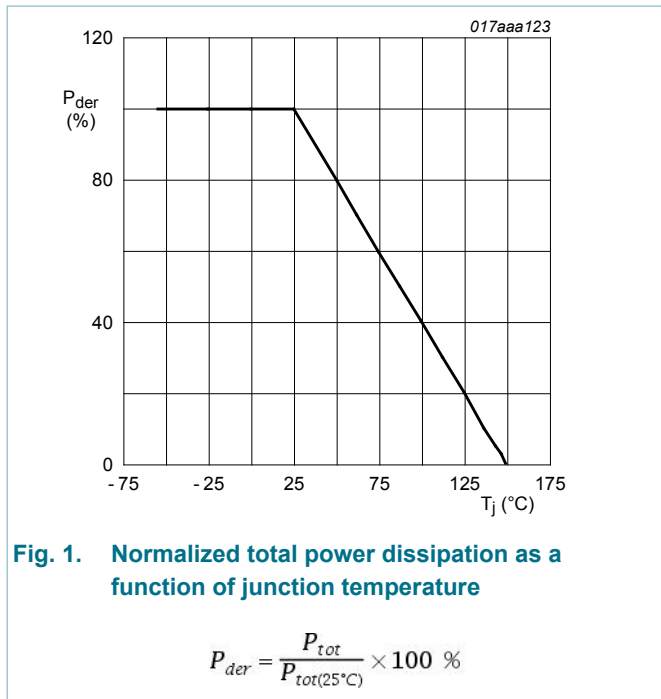
Table 5. Limiting values

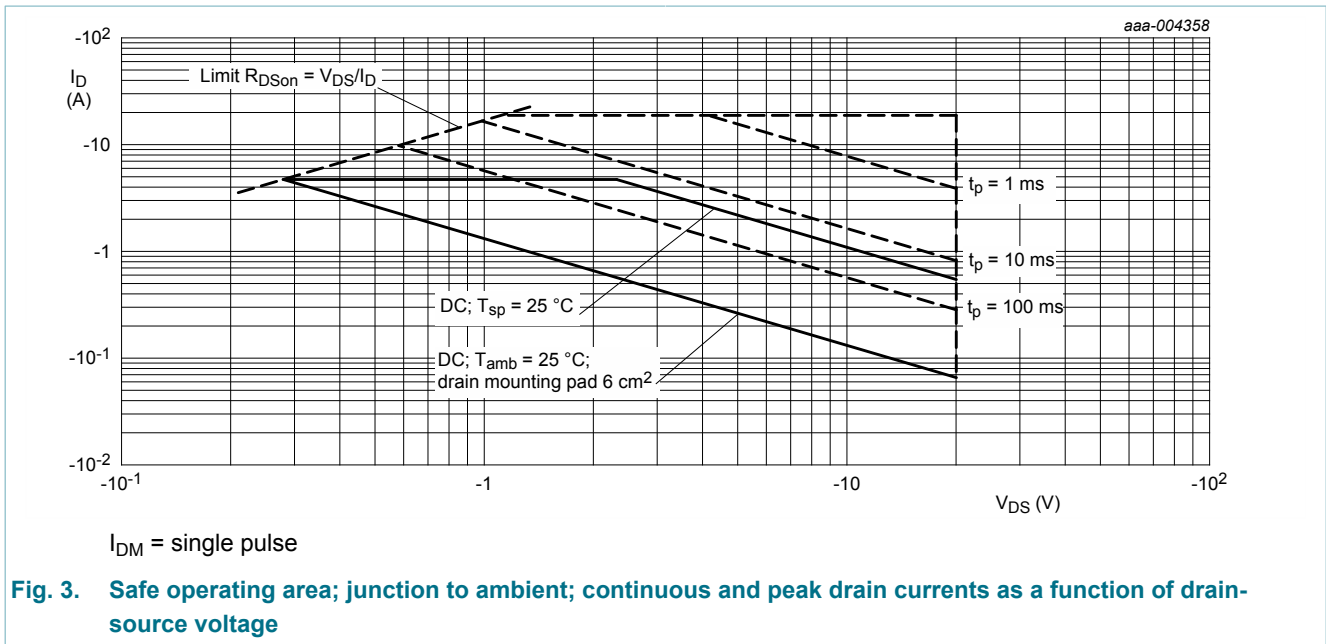
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------|-------------------------|---|-----|-----|------|------|
| V_{DS} | drain-source voltage | $T_j = 25\text{ }^\circ\text{C}$ | | - | -20 | V |
| V_{GS} | gate-source voltage | | | -8 | 8 | V |
| I_D | drain current | $V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}; t \leq 5\text{ s}$ | [1] | - | -6 | A |
| | | $V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$ | [1] | - | -4.7 | A |
| | | $V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ }^\circ\text{C}$ | [1] | - | -3.5 | A |
| I_{DM} | peak drain current | $T_{amb} = 25\text{ }^\circ\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$ | | - | -16 | A |
| P_{tot} | total power dissipation | $T_{amb} = 25\text{ }^\circ\text{C}$ | [2] | - | 500 | mW |
| | | | [1] | - | 1220 | mW |
| | | $T_{sp} = 25\text{ }^\circ\text{C}$ | | - | 8330 | mW |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---------------------------|---------------------------------|--------------------------|-----|-----|------|------|
| T _j | junction temperature | | | -55 | 150 | °C |
| T _{amb} | ambient temperature | | | -55 | 150 | °C |
| T _{stg} | storage temperature | | | -65 | 150 | °C |
| Source-drain diode | | | | | | |
| I _s | source current | T _{amb} = 25 °C | [1] | - | -1.3 | A |
| ESD maximum rating | | | | | | |
| V _{ESD} | electrostatic discharge voltage | HBM | [3] | - | 4000 | V |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





6. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|----------------|--|----------------------------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | 216 | 250 | K/W |
| | | | [2] | - | 83 | 95 | K/W |
| | | in free air; $t \leq 5\text{ s}$ | [2] | - | 51 | 60 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | 10 | 15 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

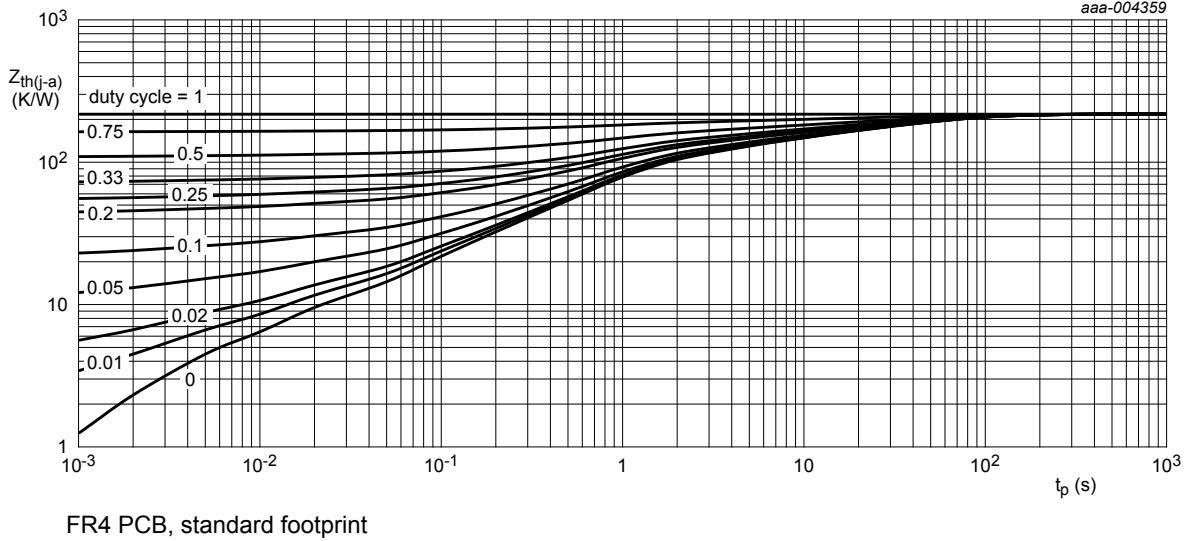


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

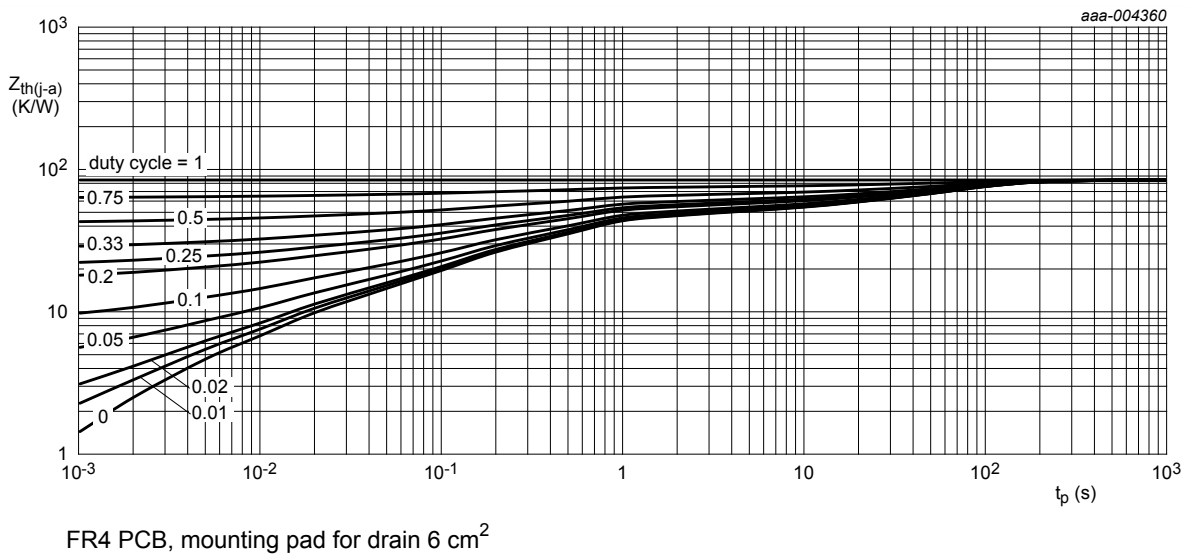


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------|--|-------|------|-------|---------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | -20 | - | - | V |
| V_{GSth} | gate-source threshold voltage | $I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ | -0.45 | -0.7 | -0.95 | V |
| I_{DSS} | drain leakage current | $V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | -1 | μA |
| | | $V_{DS} = -20 V; V_{GS} = 0 V; T_{amb} = 150 \text{ }^\circ C$ | - | - | -15 | μA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|------|
| I _{GSS} | gate leakage current | V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C | - | - | -10 | μA |
| | | V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C | - | - | -10 | μA |
| R _{DSon} | drain-source on-state resistance | V _{GS} = -4.5 V; I _D = -3 A; T _j = 25 °C | - | 37 | 43 | mΩ |
| | | V _{GS} = -4.5 V; I _D = -3 A; T _j = 150 °C | - | 51 | 59 | mΩ |
| | | V _{GS} = -2.5 V; I _D = -3 A; T _j = 25 °C | - | 45 | 55 | mΩ |
| | | V _{GS} = -1.8 V; I _D = -3 A; T _j = 25 °C | - | 59 | 72 | mΩ |
| g _{fs} | forward transconductance | V _{DS} = -10 V; I _D = -4 A; T _j = 25 °C | - | 15 | - | S |
| Dynamic characteristics | | | | | | |
| Q _{G(tot)} | total gate charge | V _{DS} = -10 V; I _D = -4.4 A; V _{GS} = -4.5 V; T _j = 25 °C | - | 15.6 | 23 | nC |
| Q _{GS} | gate-source charge | | - | 2.5 | - | nC |
| Q _{GD} | gate-drain charge | | - | 2.8 | - | nC |
| C _{iss} | input capacitance | V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C | - | 1820 | - | pF |
| C _{oss} | output capacitance | | - | 207 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 146 | - | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = -10 V; I _D = -4 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C | - | 8 | - | ns |
| t _r | rise time | | - | 21 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 50 | - | ns |
| t _f | fall time | | - | 34 | - | ns |
| Source-drain diode | | | | | | |
| V _{SD} | source-drain voltage | I _S = -1.2 A; V _{GS} = 0 V; T _j = 25 °C | - | -0.7 | -1.2 | V |

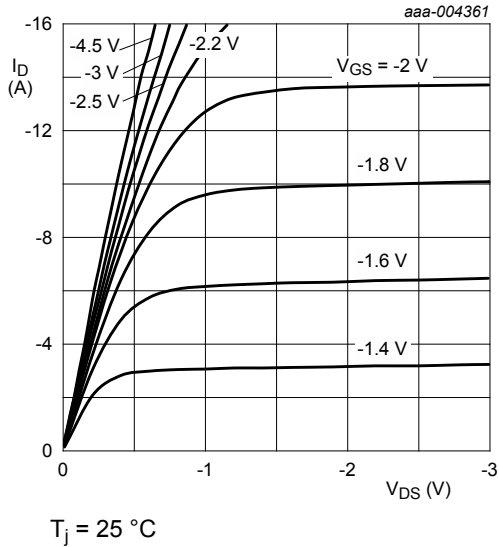


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

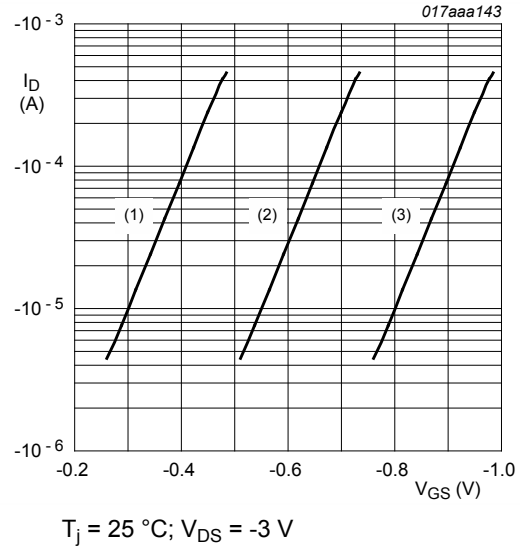


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

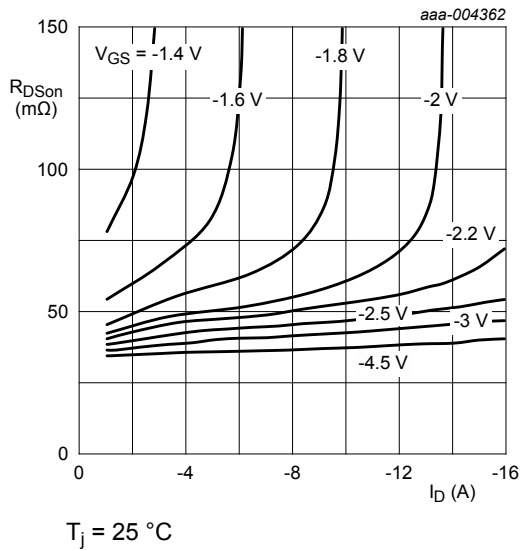


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

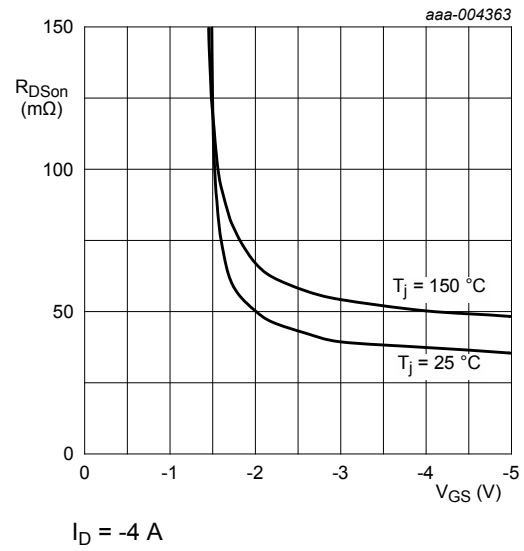


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

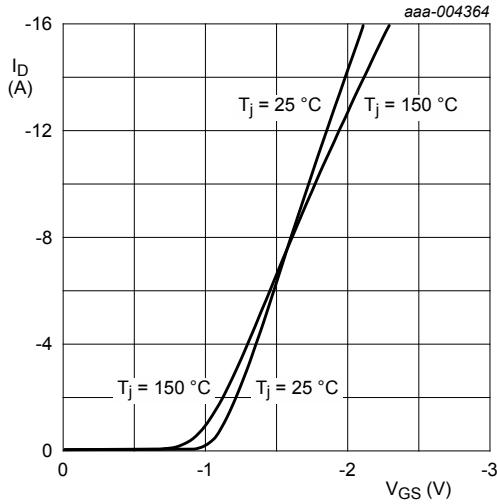


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

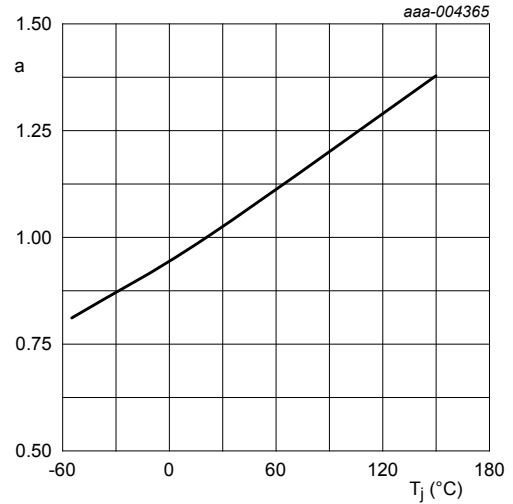


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

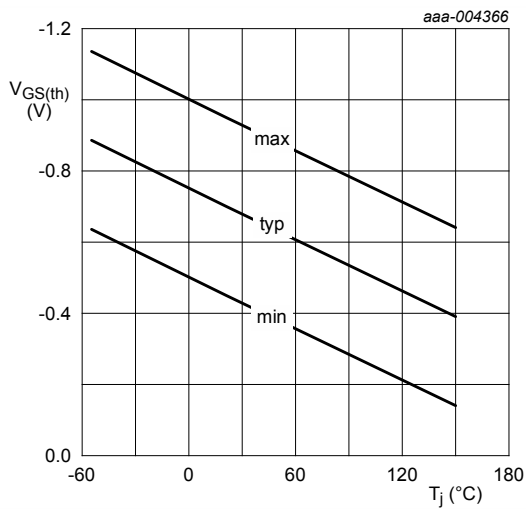


Fig. 12. Gate-source threshold voltage as a function of junction temperature

$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$

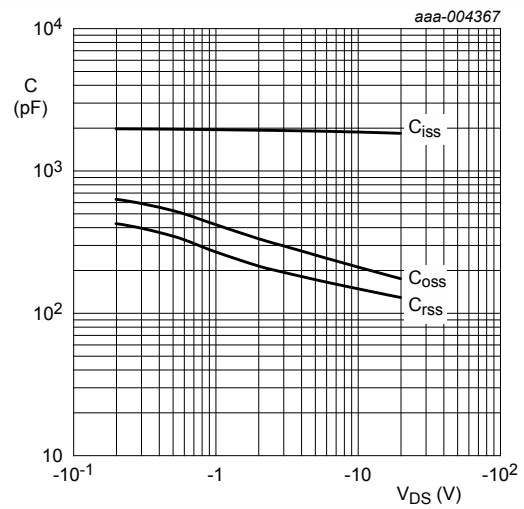
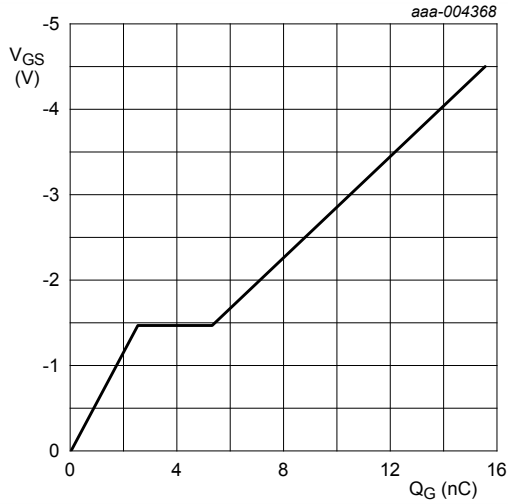


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$



$I_D = -4$ A; $V_{DS} = -10$ V; $T_{amb} = 25$ °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

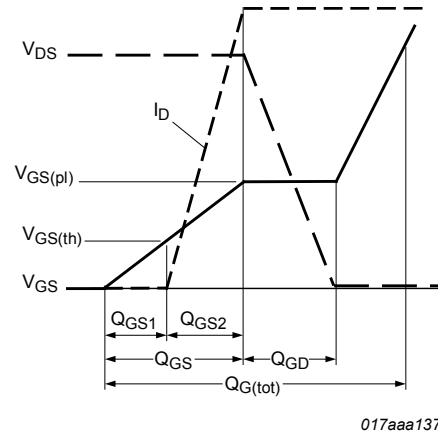
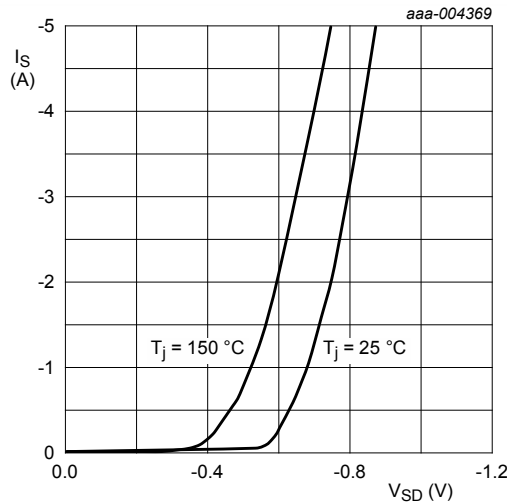


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. Source current as a function of source-drain voltage; typical values

8. Test information

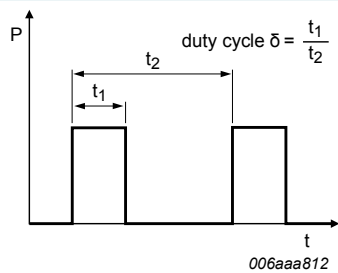


Fig. 17. Duty cycle definition

9. Package outline

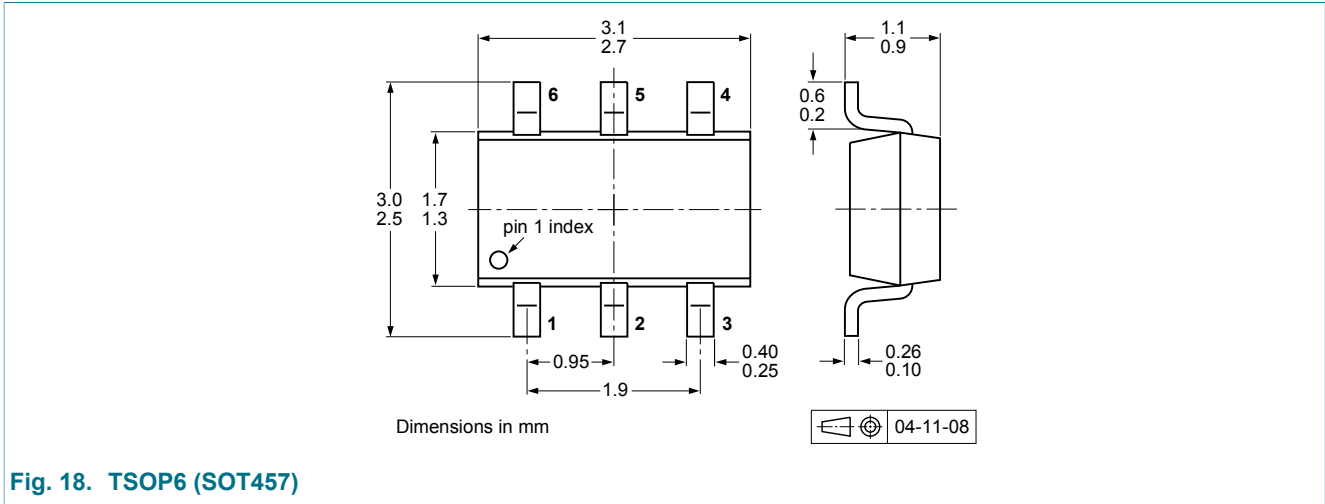


Fig. 18. TSOP6 (SOT457)

10. Soldering

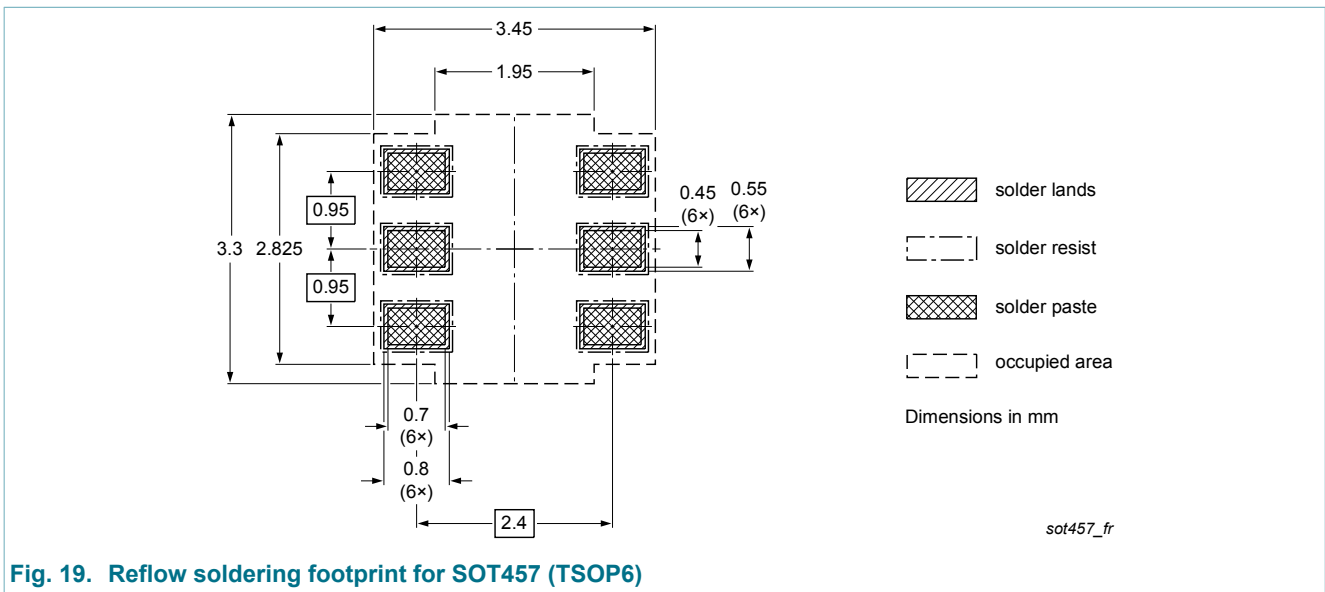


Fig. 19. Reflow soldering footprint for SOT457 (TSOP6)

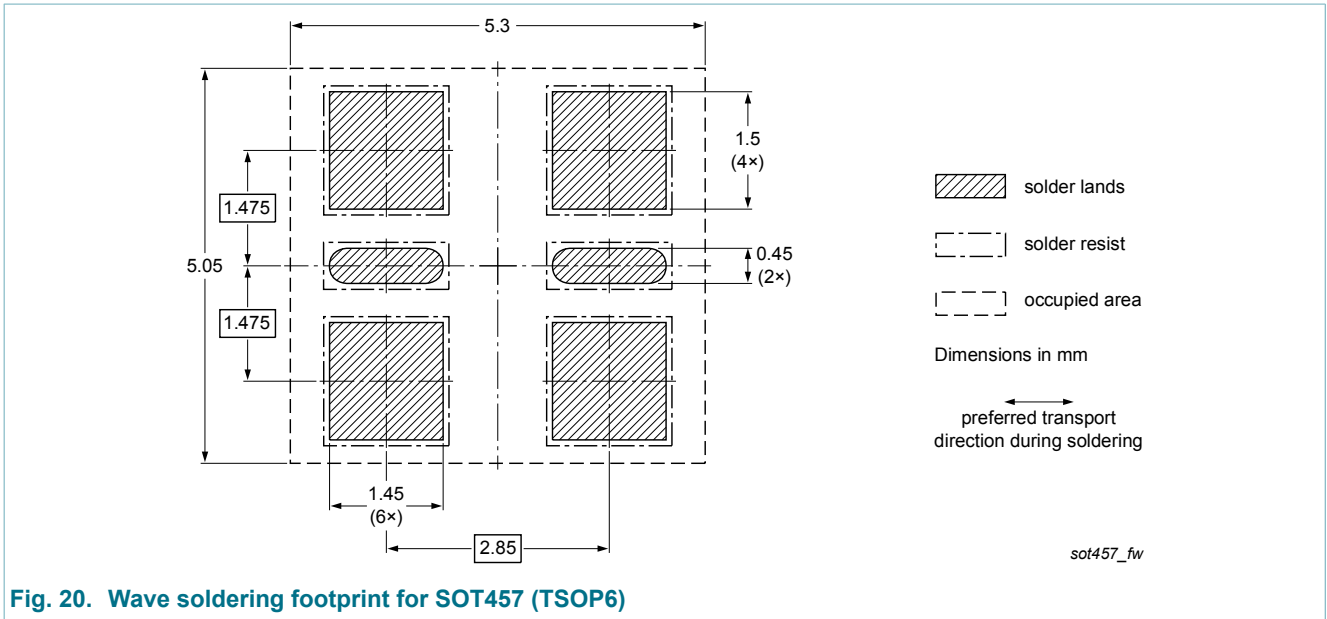


Fig. 20. Wave soldering footprint for SOT457 (TSOP6)

11. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| PMN40UPE v.1 | 20120813 | Product data sheet | - | - |

12. Legal information

12.1 Data sheet status

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|--------------------------------|--------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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13. Contents



| | | |
|-----------|--------------------------------------|-----------|
| 1 | Product profile | 1 |
| 1.1 | General description | 1 |
| 1.2 | Features and benefits | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| 2 | Pinning information | 2 |
| 3 | Ordering information | 2 |
| 4 | Marking | 2 |
| 5 | Limiting values | 2 |
| 6 | Thermal characteristics | 4 |
| 7 | Characteristics | 5 |
| 8 | Test information | 9 |
| 9 | Package outline | 10 |
| 10 | Soldering | 10 |
| 11 | Revision history | 11 |
| 12 | Legal information | 12 |
| 12.1 | Data sheet status | 12 |
| 12.2 | Definitions | 12 |
| 12.3 | Disclaimers | 12 |
| 12.4 | Trademarks | 13 |

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Date of release: 13 August 2012

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