THE DATASHEET OF

TLC254ACN

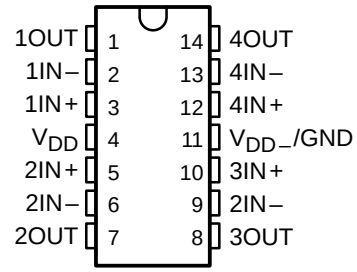
www.win-source.net 0086-755-83957316

LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

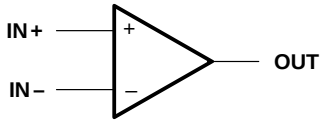
SLOS003G – JUNE 1983 – REVISED MARCH 2001

- **A-Suffix Versions Offer 5-mV V_{IO}**
- **B-Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 25 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz (High-Bias Version)**

D, N, OR PW PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC254, TLC254A, TLC254B, TLC25L4, TLC254L4A, TLC254L4B, TLC25M4, TLC25M4A and TL25M4B are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input-offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for these devices include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices.

Available options

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	10 mV	TLC254CD	TLC254CN	TLC254CPW	TLC254Y
	5 mV	TLC254ACD	TLC254ACN	—	—
	2 mV	TLC254BCD	TLC254BCN	—	—
	10 mV	TLC25L4CD	TLC25L4CN	TLC25L4CPW	TLC25L4Y
	5 mV	TLC25L4ACD	TLC25L4ACN	—	—
	2 mV	TLC25L2BCD	TLC25L4BCN	—	—
	10 mV	TLC25M4CD	TLC25M4CN	TLC25M4CPW	TLC25M4Y
	5 mV	TLC25M4ACD	TLC25M4ACN	—	—
	2 mV	TLC25M4BCD	TLC25M4BCN	—	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC254CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2001, Texas Instruments Incorporated

description (continued)

General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with these devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. These devices are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic dip and the small-outline packages. The device is also available in chip form.

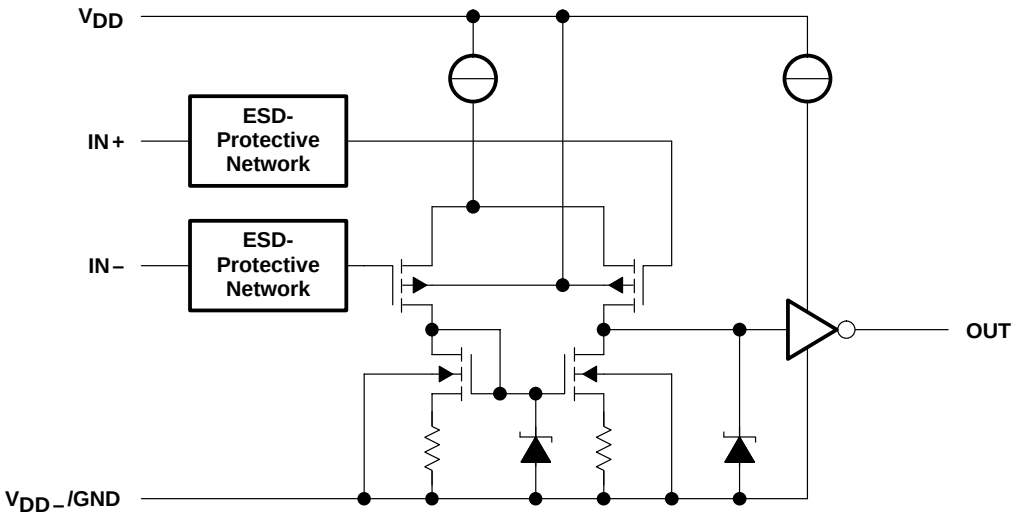
These devices are characterized for operation from 0°C to 70°C.

DEVICE FEATURES

PARAMETER	TLC25L4_C (LOW BIAS)	TLC25M4_C (MEDIUM BIAS)	TLC254_C (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μA	0.6 V/μA	4.5 V/μA
Input offset voltage (Max) TLC254C, TLC25L4C, TLC25M4C TLC254AC, TLC25L4AC, TLC25M4AC TLC254BC, TLC25L4BC, TLC25M4BC	 10 mV 5 mV 2 mV	 10 mV 5 mV 2 mV	 10 mV 5 mV 2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

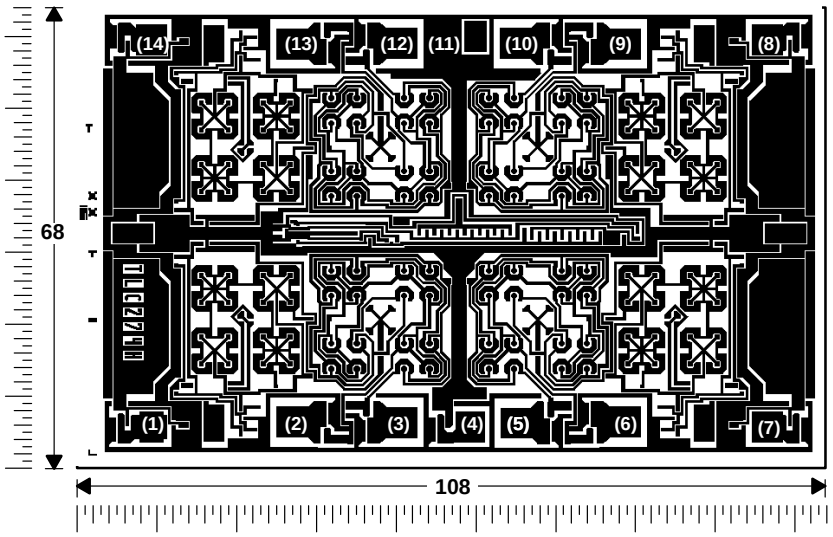
equivalent schematic (each amplifier)

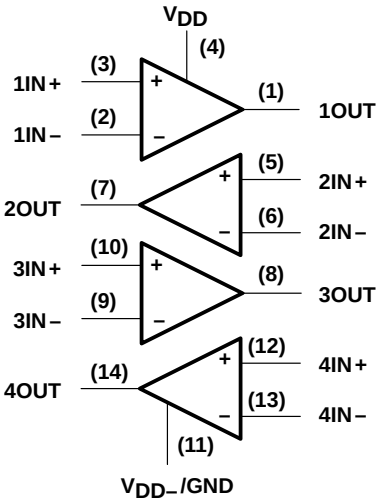


chip information

These chips, when properly assembled, display characteristics similar to the TLC25_4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . –0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+, with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
N	1050 mW	9.2 mW/°C	736 mW
PW	700 mW	5.6 mW/°C	448 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0	0.2	V
	V_{DD} = 5 V	–0.2	4	
	V_{DD} = 10 V	–0.2	9	
	V_{DD} = 16 V	–0.2	14	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	T_A	TLC254_C			TLC25L4_C			T
					MIN	TYP	MAX	MIN	TYP	MAX	MIN
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10	
				0°C to 70°C			12			12	
		TLC25_4AC		25°C			5			5	
				0°C to 70°C			6.5			6.5	
		TLC25_4BC		25°C			2			2	
				0°C to 70°C			3			3	
a_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1		
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1	60		1	60	
				0°C to 70°C			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1	60		1	60	
				0°C to 70°C			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 t 0.2
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		45
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20		
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR}min	25°C	60	77		60	77		6
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C		600	750		50	68	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise no connected from the output to ground and has the following value: for low bias, R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10

‡ The output swings to the potential of V_{DD-}/GND.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			T
			MIN	TYP	MAX	MIN	TYP	MAX	MIN
SR	Slew rate at unity gain	See Figure 1		0.1			0.001		
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω, See Figure 1		12			12		
	Overshoot factor	See Figure 1		30%			35%		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC254, TLC254AC, TLC254BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC254C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC254AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC254BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.34	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	0°C	3	3.8		V
					25°C	3.2	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	0°C	4	27		V/mV
					25°C	5	23		
					70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		0°C	60	84		dB
					25°C	65	80		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	94		dB
					25°C	65	95		
					70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	0°C		3.1	7.2	mA
					25°C		2.7	6.4	
					70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC254C, TLC254AC, TLC254BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC254C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC254AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC254BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.39	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	0°C	7.8	8.5		V
					25°C	8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	0°C	7.5	42		V/mV
					25°C	10	36		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		0°C	60	88		dB
					25°C	65	85		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	94		dB
					25°C	65	95		
					70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	0°C		4.5	8.8	mA
					25°C		3.8	8	
					70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			T_A	TLC254C, TLC254AC, TLC254BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, See Figure 1	C_L = 20 pF,	$V_{I(PP)}$ = 1 V	0°C		4		V/μs
					25°C		3.6		
				$V_{I(PP)}$ = 1 V	70°C		3		
				$V_{I(PP)}$ = 2.5 V	0°C		3.1		
					25°C		2.9		
					70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 10 kΩ,	0°C		340		kHz
					25°C		320		
					70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 1	0°C		2		MHz
					25°C		1.7		
					70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,	0°C		47°		
					25°C		46°		
					70°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			T_A	TLC254C, TLC254AC, TLC254BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, See Figure 1	C_L = 20 pF,	$V_{I(PP)}$ = 1 V	0°C		5.9		V/μs
					25°C		5.3		
					70°C		4.3		
				$V_{I(PP)}$ = 5.5 V	0°C		5.1		
					25°C		4.6		
					70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 10 kΩ,	0°C		220		kHz
					25°C		200		
					70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 1	0°C		2.5		MHz
					25°C		2.2		
					70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,	0°C		50°		
					25°C		49°		
					70°C		46°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC25L4C, TLC25L4AC, TLC25L4BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.24	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	0°C	3	4.1		V
					25°C	3.2	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	0°C	50	680		V/mV
					25°C	50	520		
					70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		0°C	60	95		dB
					25°C	65	94		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	97		dB
					25°C	70	98		
					70°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	0°C		48	84	μA
					25°C		40	68	
					70°C		31	56	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC25L4C, TLC25L4AC, TLC25L4BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.26	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} =.5 V	25°C		0.7	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	0°C	7.8	8.9		V
					25°C	8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	0°C	50	1025		V/mV
					25°C	50	870		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		0°C	60	97		dB
					25°C	65	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	97		dB
					25°C	70	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	0°C		72	132	µA
					25°C		57	92	
					70°C		44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			T_A	TLC25L4C, TLC25L4AC, TLC25L4BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, See Figure 1	C_L = 20 pF,	$V_{I(PP)}$ = 1 V	0°C		0.04		V/μs
					25°C		0.03		
					70°C		0.03		
				$V_{I(PP)}$ = 2.5 V	0°C		0.03		
					25°C		0.03		
					70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 1 MΩ,	0°C		6		kHz
					25°C		5		
					70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 1	0°C		100		kHz
					25°C		85		
					70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,	0°C		36°		
					25°C		34°		
					70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			T_A	TLC25L4C, TLC25L4AC, TLC25L4BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, See Figure 1	C_L = 20 pF,	$V_{I(PP)}$ = 1 V	0°C		0.05		V/μs
					25°C		0.05		
					70°C		0.04		
				$V_{I(PP)}$ = 5.5 V	0°C		0.05		
					25°C		0.04		
					70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 1 MΩ,	0°C		1.3		kHz
					25°C		1		
					70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 1	0°C		125		kHz
					25°C		110		
					70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,	0°C		40°		
					25°C		38°		
					70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC25M4C, TLC25M4AC, TLC25M4BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25M4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.25	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 t0 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	0°C	3	3.9		V
					25°C	3.2	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	0°C	15	200		V/mV
					25°C	25	170		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		0°C	60	91		dB
					25°C	65	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	92		dB
					25°C	70	93		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	0°C		500	1280	µA
					25°C		420	1120	
					70°C		340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC25M4C, TLC25M4AC, TLC25M4BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25M4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.26	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	0°C	7.8	8.7		V
					25°C	8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	0°C	15	320		V/mV
					25°C	25	275		
					70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		0°C	60	94		dB
					25°C	65	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	92		dB
					25°C	70	93		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	0°C		690	1600	μA
					25°C		570	1200	
					70°C		440	1120	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			T_A	TLC25M4C, TLC25M4AC, TLC25M4BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, See Figure 1	C_L = 20 pF,	$V_{I(PP)}$ = 1 V	0°C		0.46		V/µs
					25°C		0.43		V/µs
					70°C		0.36		V/µs
				$V_{I(PP)}$ = 2.5 V	0°C		0.43		
					25°C		0.40		
					70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 100 kΩ,	0°C		60		kHz
					25°C		55		
					70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 1	0°C		610		kHz
					25°C		525		
					70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,	0°C		41°		
					25°C		40°		
					70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			T_A	TLC25M4C, TLC25M4AC, TLC25M4BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, See Figure 1	C_L = 20 pF,	$V_{I(PP)}$ = 1 V	0°C		0.67		V/µs
					25°C		0.62		
					70°C		0.51		
				$V_{I(PP)}$ = 5.5 V	0°C		0.61		
					25°C		0.56		
					70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 100 kΩ,	0°C		40		kHz
					25°C		35		
					70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 1	0°C		710		kHz
					25°C		635		
					70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,	0°C		44°		
					25°C		43°		
					70°C		42°		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, See Note 6		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage			1.8			1.1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.1	60		0.1	60		0.1	60	pA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.6	60		0.6	60		0.6	60	pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	3.2	3.8		3.2	4.1		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V, See Note 6	5	23		50	520		25	170		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	65	80		65	94		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	97		70	93		dB
I_{DD}	Supply current	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load		2.7	6.4		0.04	0.068		0.42	1.12	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. For low-bias mode, R_L = 1 MΩ, for medium-bias mode, R_L = 100 kΩ, and for high-bias mode, R_L = 10 kΩ.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	C_L = 20 pF, See Note 6	$V_{I(PP)}$ = 1 V		3.6			0.03			0.43		V/μs
			$V_{I(PP)}$ = 2.5 V		2.9			0.03			0.40		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω		2.5			70			32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ	C_L = 20 pF,		320			5			55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1.7			0.085			0.525		MHz
ϕ_m	Phase margin	f = B_1, C_L = 20 pF	V_I = 10 mV,		46°			34°			40°		

NOTE 6: For low-bias mode, R_L = 1 MΩ, for medium-bias mode, R_L = 100 kΩ, and for high-bias mode, R_L = 10 kΩ.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC25_4, TLC25_4A, and TLC25_4B are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

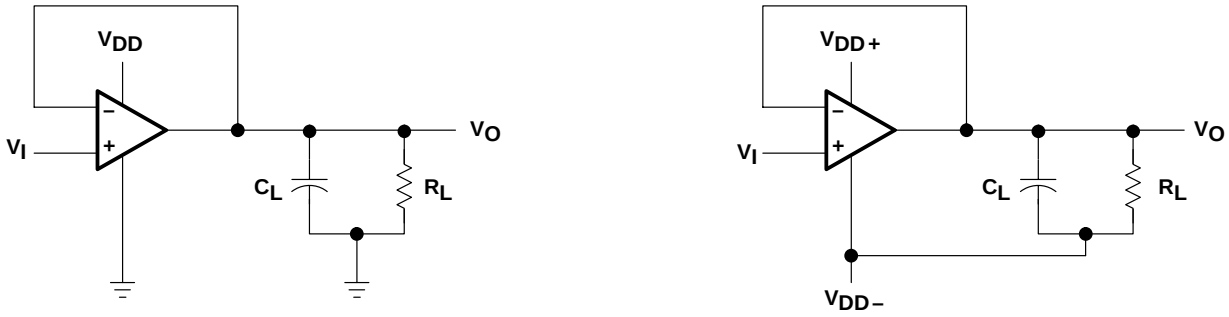


Figure 1. Unity-Gain Amplifier

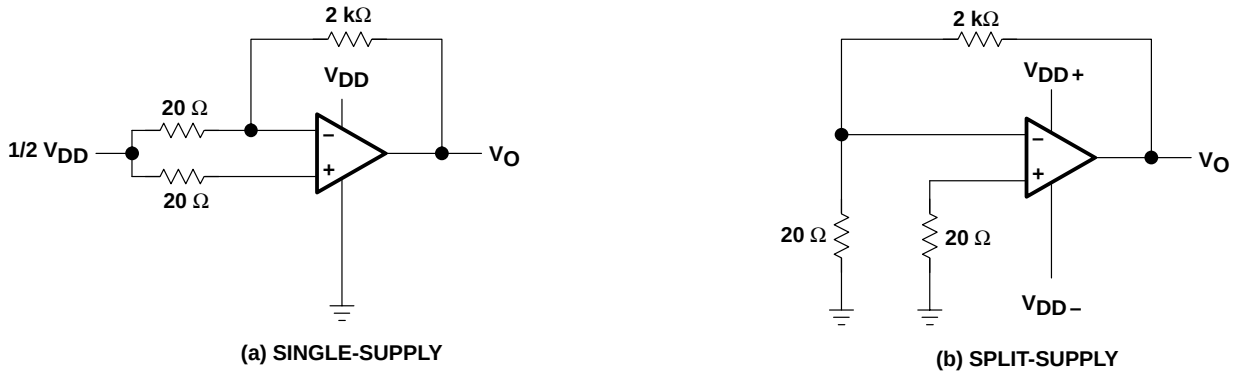


Figure 2. Noise-Test Circuit

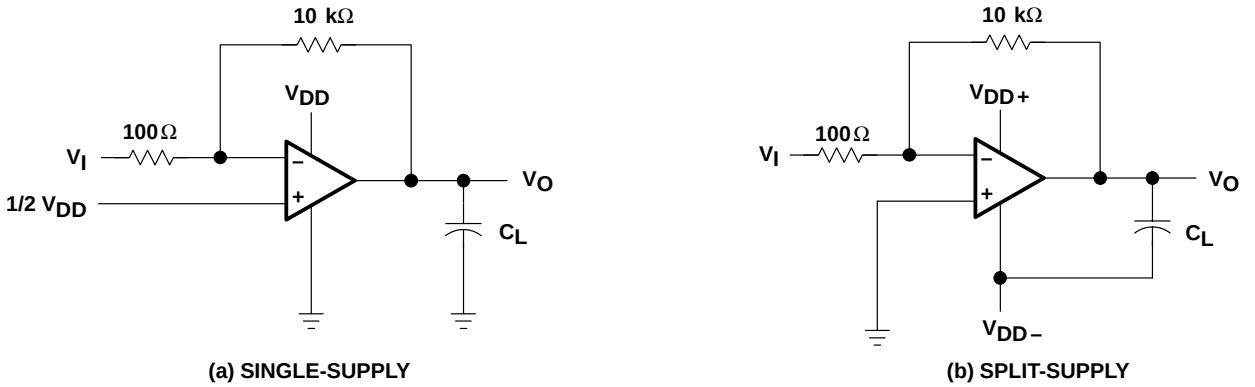


Figure 3. Gain-of-100 Inverting Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
I_{DD}	Supply current		vs Supply voltage vs Free-air temperature	4 5
A_{VD}	Large-signal differential voltage amplification	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8
	Phase shift	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8

SUPPLY CURRENT vs SUPPLY VOLTAGE

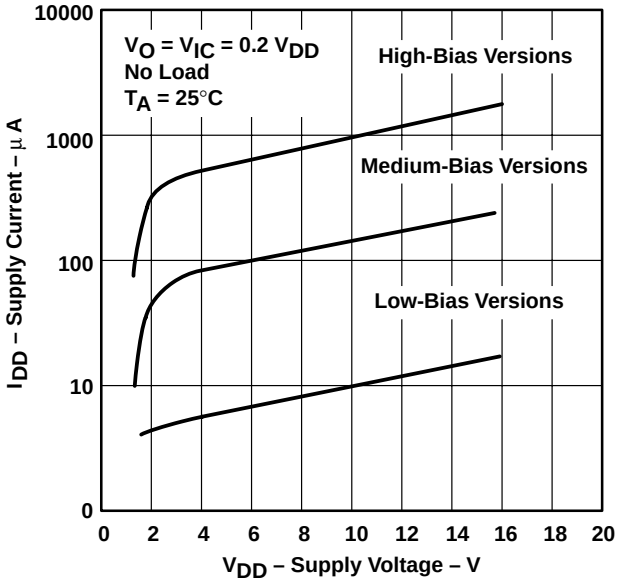


Figure 4

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

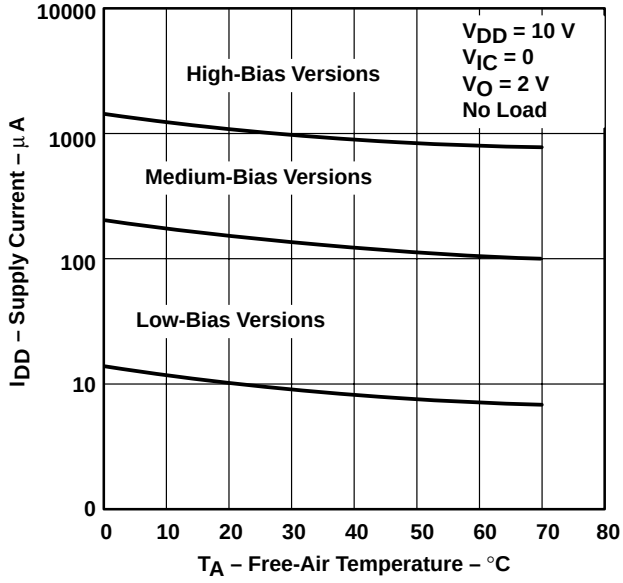


Figure 5

TYPICAL CHARACTERISTICS

LOW-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

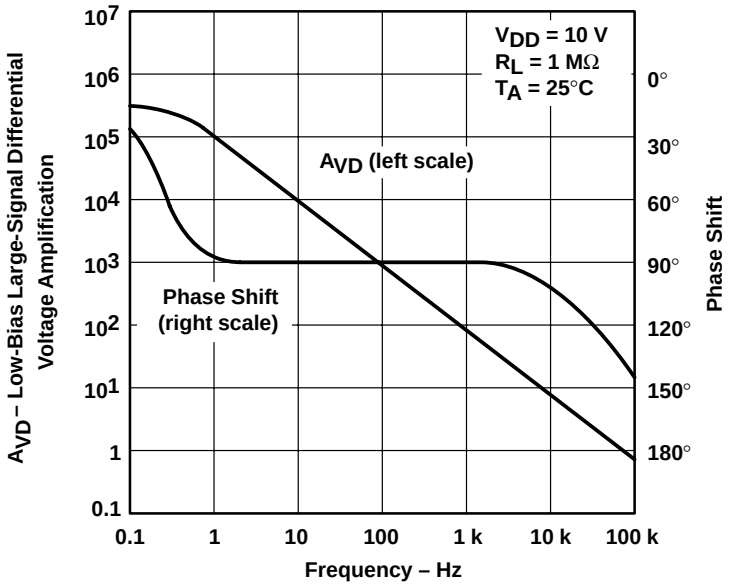


Figure 6

MEDIUM-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

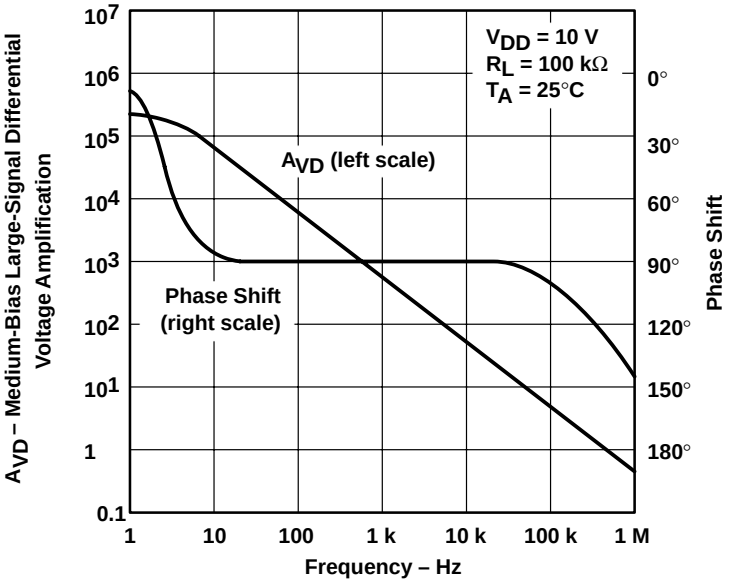


Figure 7

TYPICAL CHARACTERISTICS

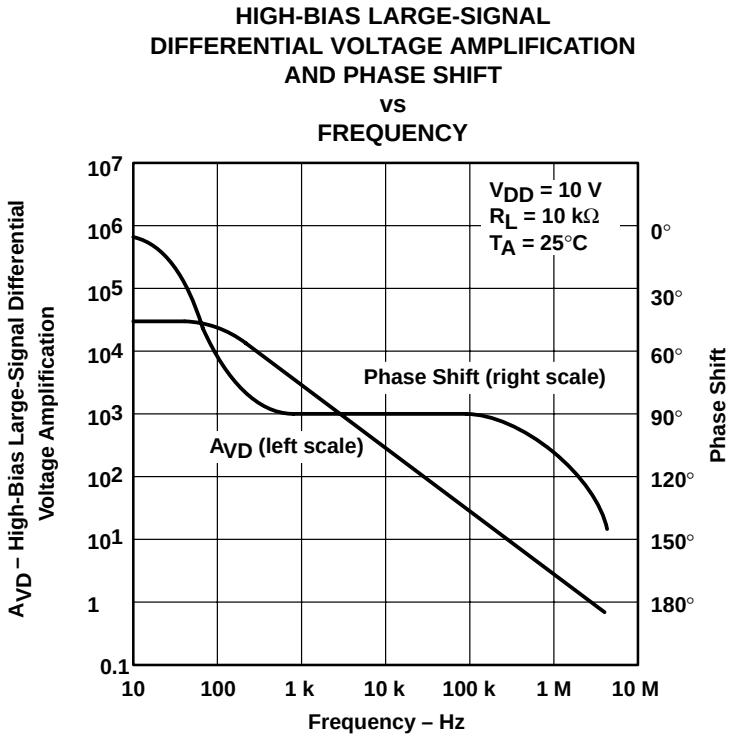


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifiers supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the potential of V_{DD-}/GND.

supply configurations

Even though the TLC25_4C series is are characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

Whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup as well as excessive dc leakages.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC254ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254AC	Samples
TLC254BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254BC	Samples
TLC254BCN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC254BCN	Samples
TLC254CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254C	Samples
TLC254CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254C	Samples
TLC254CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	Samples
TLC254CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	Samples
TLC25L4BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	25L4BC	Samples
TLC25L4BCN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC25L4BCN	Samples
TLC25L4CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25L4C	Samples
TLC25L4CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25L4C	Samples
TLC25M4CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25M4C	Samples
TLC25M4CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC25M4CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

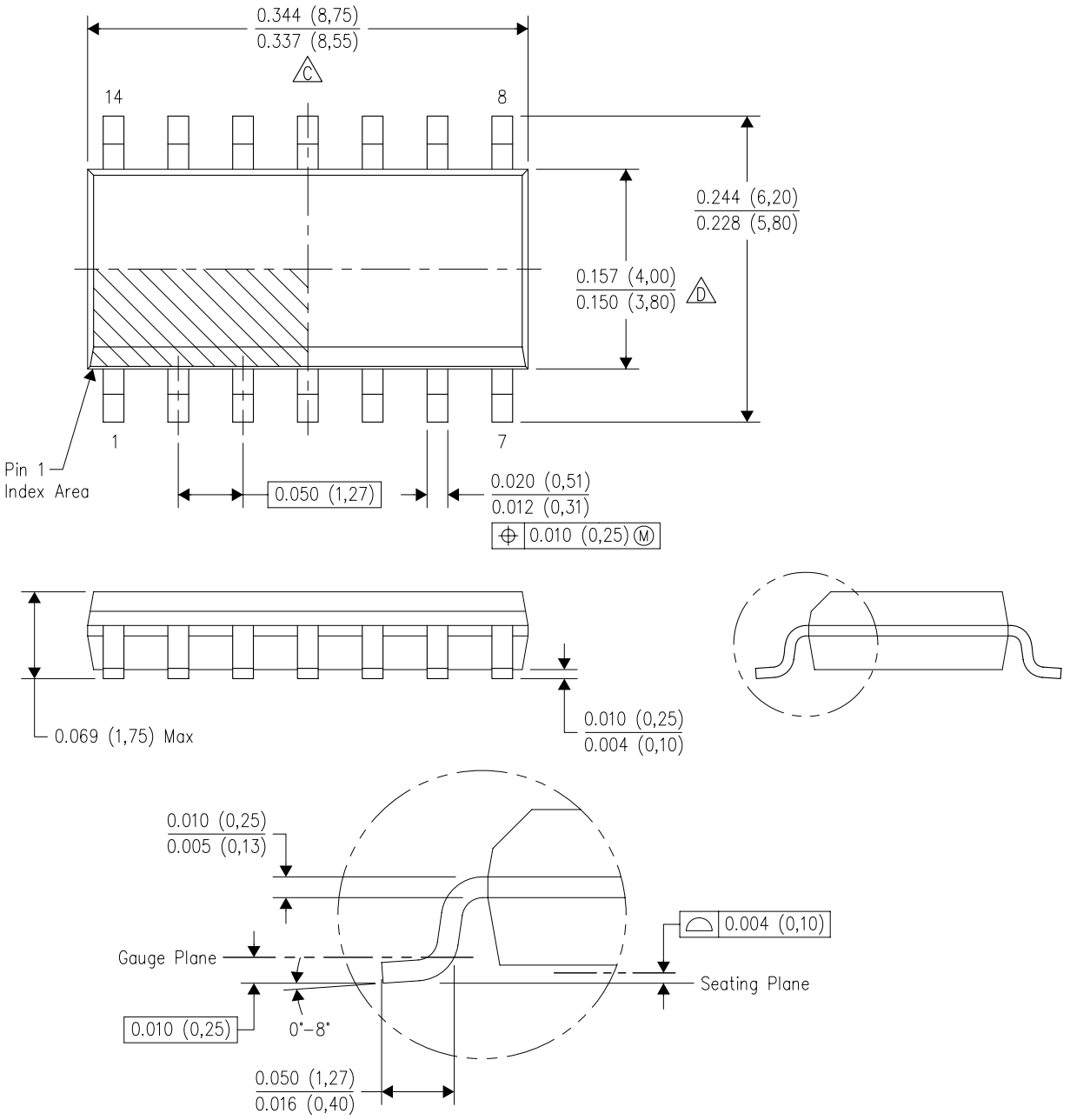
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

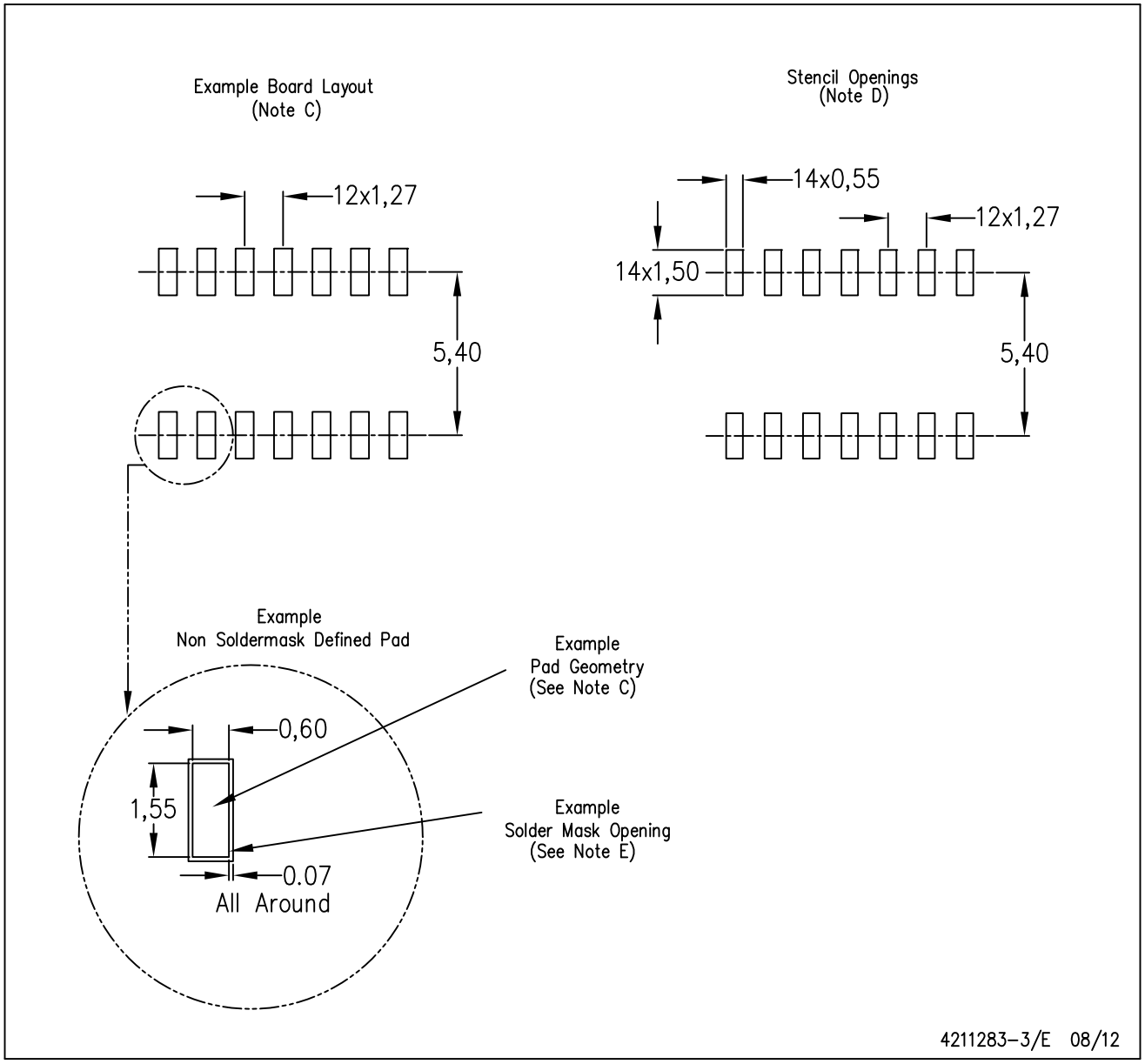
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

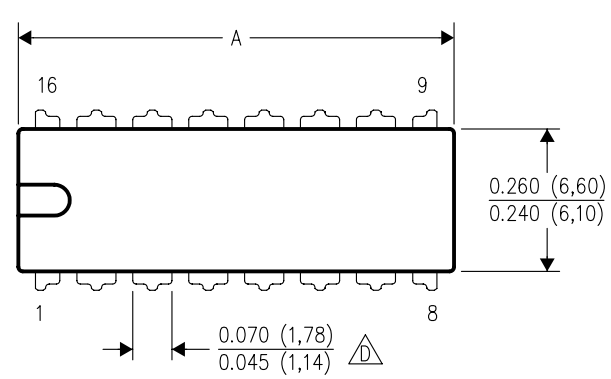


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

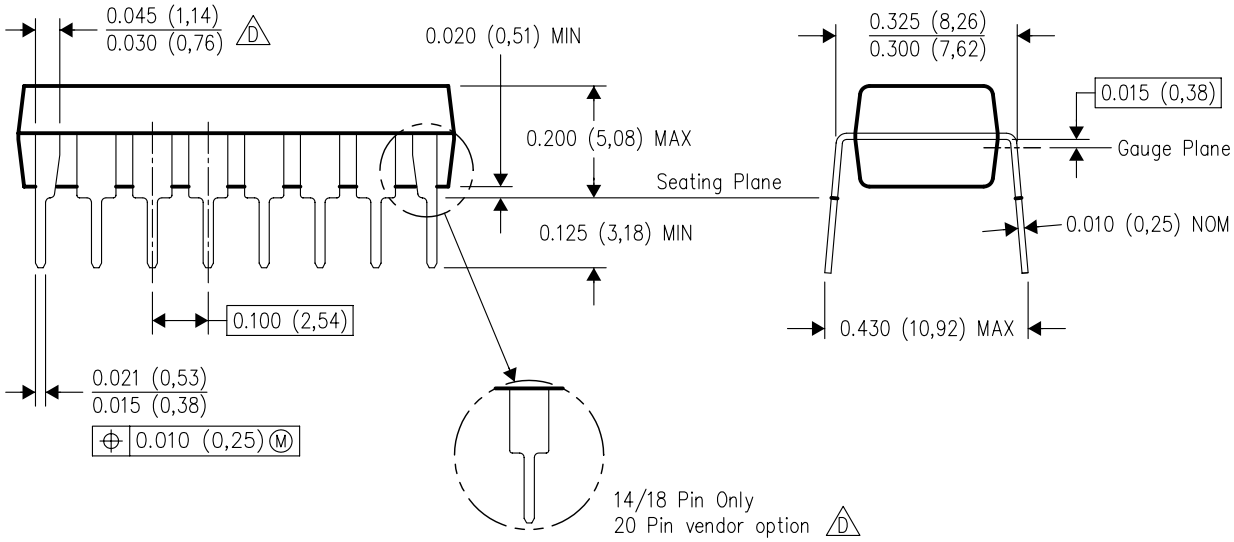
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TLC254ACN on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management