# THE DATASHEET OF

# CD74HCU04E

Data sheet acquired from Harris Semiconductor
SCHS127D

February 1998 - Revised May 2004

# High-Speed CMOS Logic Hex Inverter

## Features

- **Typical Propagation Delay: 6ns at $V_{CC}$ = 5V, $C_L$ = 15pF, $T_A$ = 25$^{O}$C, Fastest Part in QMOS Line**
- **Wide Operating Temperature Range . . . -55$^{O}$C to 125$^{O}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HCU Types**
  - **2-V to 6-V Operation**
  - **High Noise Immunity: $N_{IL}$ = 20%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

## Description

The CD74HCU04 unbuffered hex inverter utilizes silicon-gate CMOS technology to achieve operation speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. These devices especially are useful in crystal oscillator and analog applications.

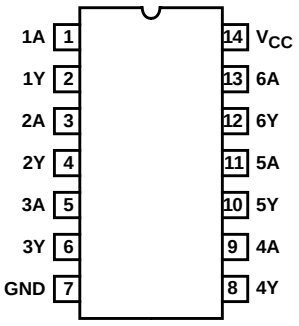
## Ordering Information

| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE |
|---|---|---|
| CD74HCU04E | -55 to 125 | 14 Ld PDIP |
| CD74HCU04M | -55 to 125 | 14 Ld SOIC |
| CD74HCU04MT | -55 to 125 | 14 Ld SOIC |
| CD74HCU04M96 | -55 to 125 | 14 Ld SOIC |
| CD74HCU04PWR | -55 to 125 | 14 Ld TSSOP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

## Pinout

**CD74HCU04**
**(PDIP, SOIC, TSSOP)**
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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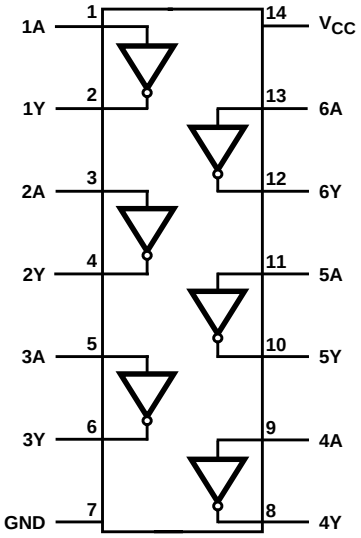
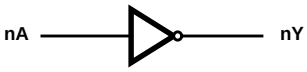
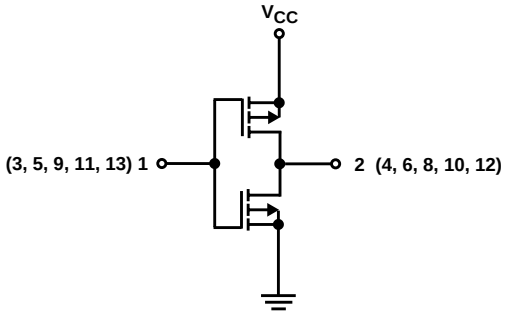
## Functional Diagram




## Logic Symbol




## Schematic Diagram



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$
Voltages Referenced to Ground . . . . . -0.5V to +7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Drain Current, per Output, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±50mA

## Thermal Information

Thermal Resistance (Typical, Note 1) $\theta_{JA}$ ($^oC/W$)
E (PDIP) Package . . . . . 80
M (SOIC) Package . . . . . 86
PW (TSSOP) Package . . . . . 113
Maximum Junction Temperature (Hermetic Package or Die) . . . $175^oC$
Maximum Junction Temperature (Plastic Package) . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range $T_A$ . . . . . $-55^oC$ to $125^oC$
Supply Voltage Range, $V_{CC}$ . . . . . 2V to 6V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.7 | - | 1.7 | - | 1.7 | - | V |
| | | | | 4.5 | 3.6 | - | 3.6 | - | 3.6 | - | V |
| | | | | 6 | 4.8 | - | 4.8 | - | 4.8 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | | | 4.5 | - | 0.8 | - | 0.8 | - | 0.8 | V |
| | | | | 6 | - | 1.1 | - | 1.1 | - | 1.1 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.8 | - | 1.8 | - | 1.8 | - | V |
| | | | -0.02 | 4.5 | 4 | - | 4 | - | 4 | - | V |
| | | | -0.02 | 6 | 5.5 | - | 5.5 | - | 5.5 | - | V |
| High Level Output Voltage TTL Loads | | $V_{CC}$ or GND | -4 | 4.5 | 3.98 | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | 0.2 | - | 0.2 | - | 0.2 | V |
| | | | 0.02 | 4.5 | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | 0.02 | 6 | - | 0.5 | - | 0.5 | - | 0.5 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $V_{CC}$ or GND | 5.2 | 6 | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | 2 | - | 20 | - | 40 | µA |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Propagation Delay, Input to Output Y (Figure 1) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 70 | - | 90 | - | 105 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 14 | - | 18 | - | 21 | ns |
| | | $C_L$ = 15pF | 5 | - | 5 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 12 | - | 15 | - | 18 | ns |
| Transition Times (Figure 1) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | 18 | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | $C_I$ | - | See Figure 3 | | | | | | | | pF |
| Power Dissipation Capacitance (Notes 2, 3) | $C_{PD}$ | - | 5 | - | 14 | - | - | - | - | - | pF |

NOTES:

2. $C_{PD}$ is used to determine the dynamic power consumption, per inverter.
3. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = input frequency, $C_L$ = output load capacitance, $V_{CC}$ = supply voltage.

## *Test Circuits and Waveforms*

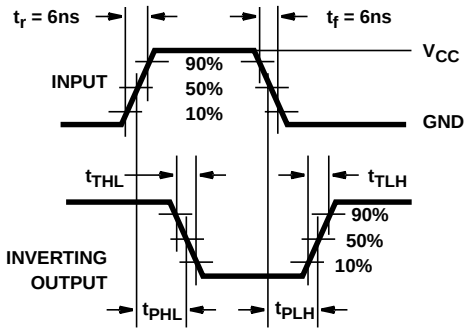



**FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

## *Typical Performance Curves*

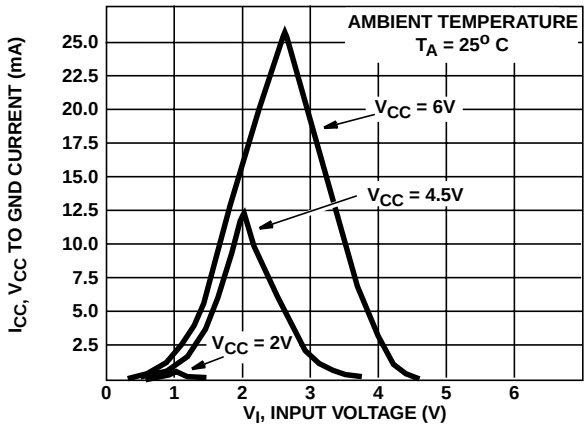



**FIGURE 2. TYPICAL INVERTER SUPPLY CURRENT AS FUNCTION OF INPUT VOLTAGE**

## Typical Performance Curves (Continued)

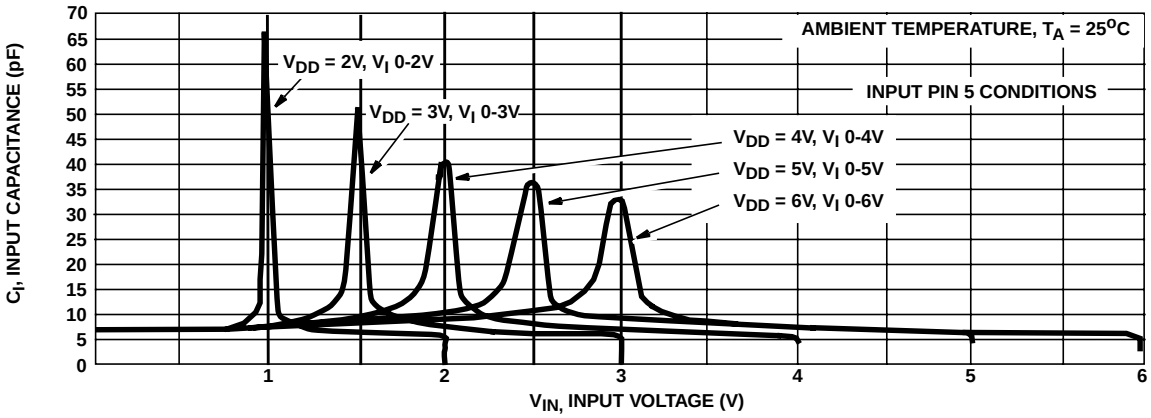



**FIGURE 3. INPUT CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HCU04E | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCU04E | Samples |
| CD74HCU04EE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCU04E | Samples |
| CD74HCU04M | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCU04M | Samples |
| CD74HCU04M96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCU04M | Samples |
| CD74HCU04M96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCU04M | Samples |
| CD74HCU04M96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCU04M | Samples |
| CD74HCU04PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJU04 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD74HCU04 :**

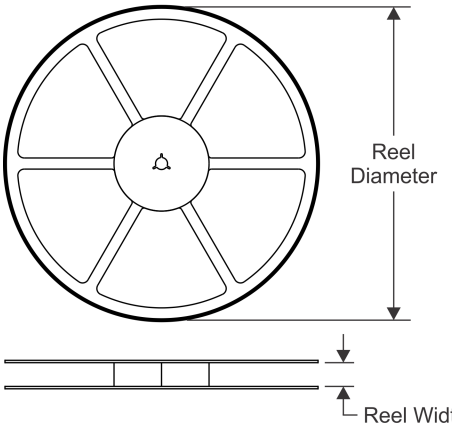
- Automotive: CD74HCU04-Q1

NOTE: Qualified Version Definitions:

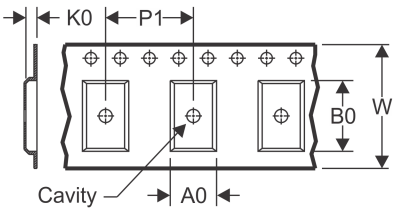
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

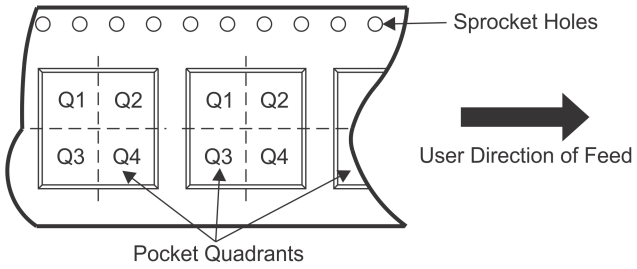



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

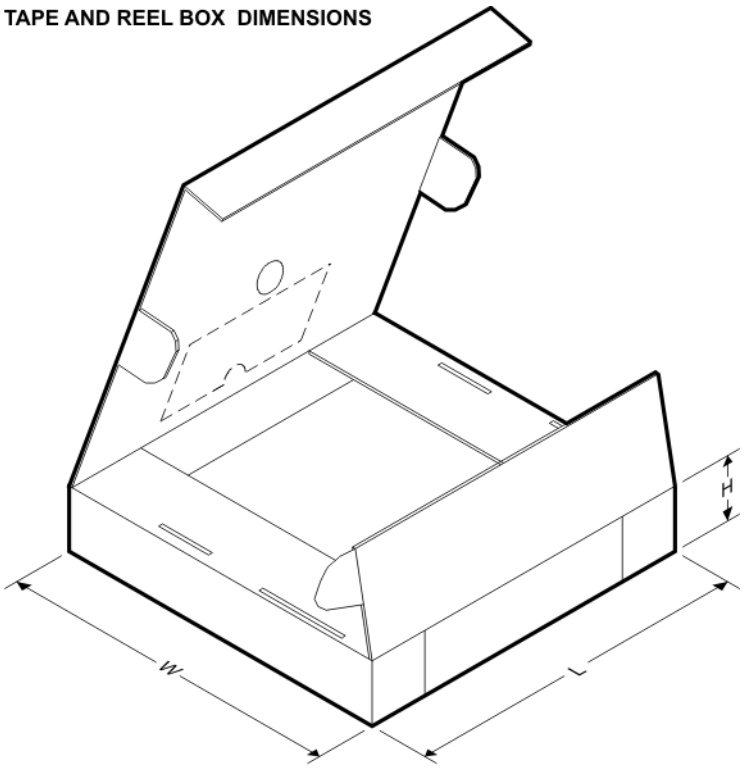
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HCU04M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCU04PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

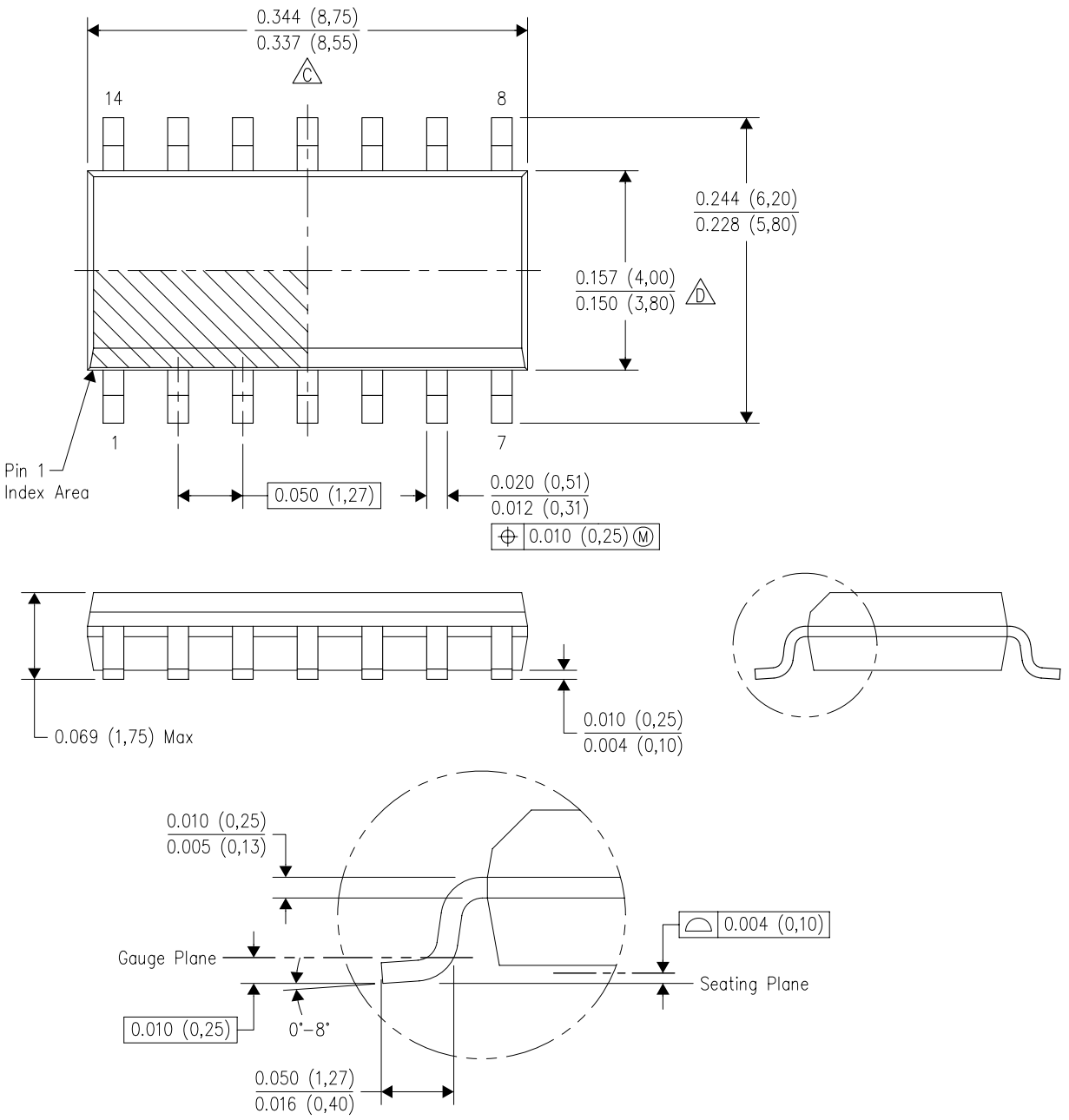
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

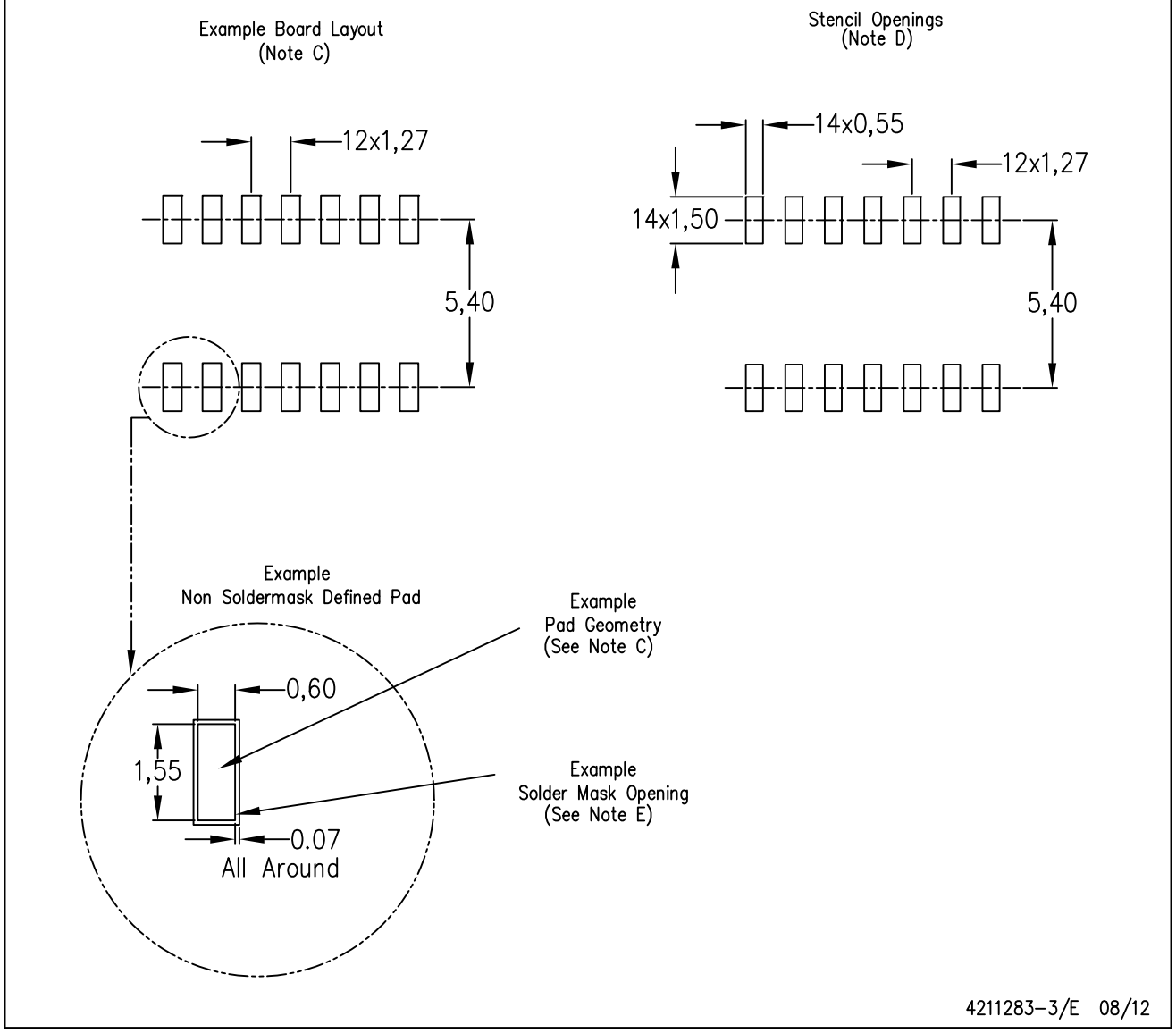
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HCU04M96 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| CD74HCU04PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



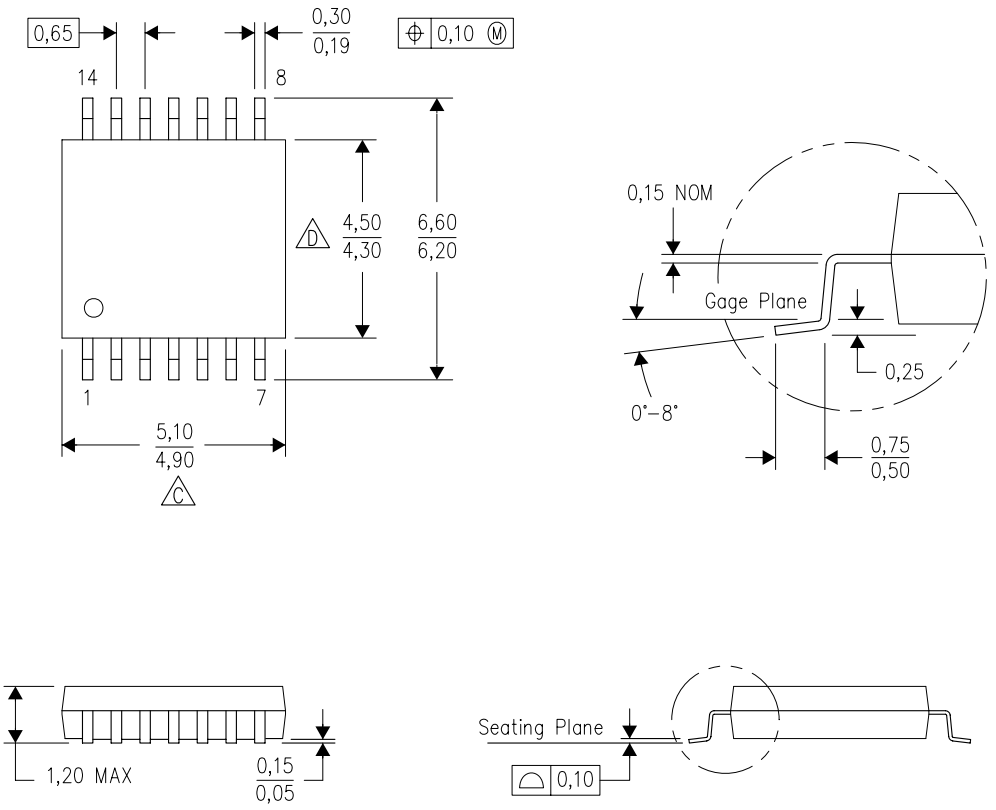

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

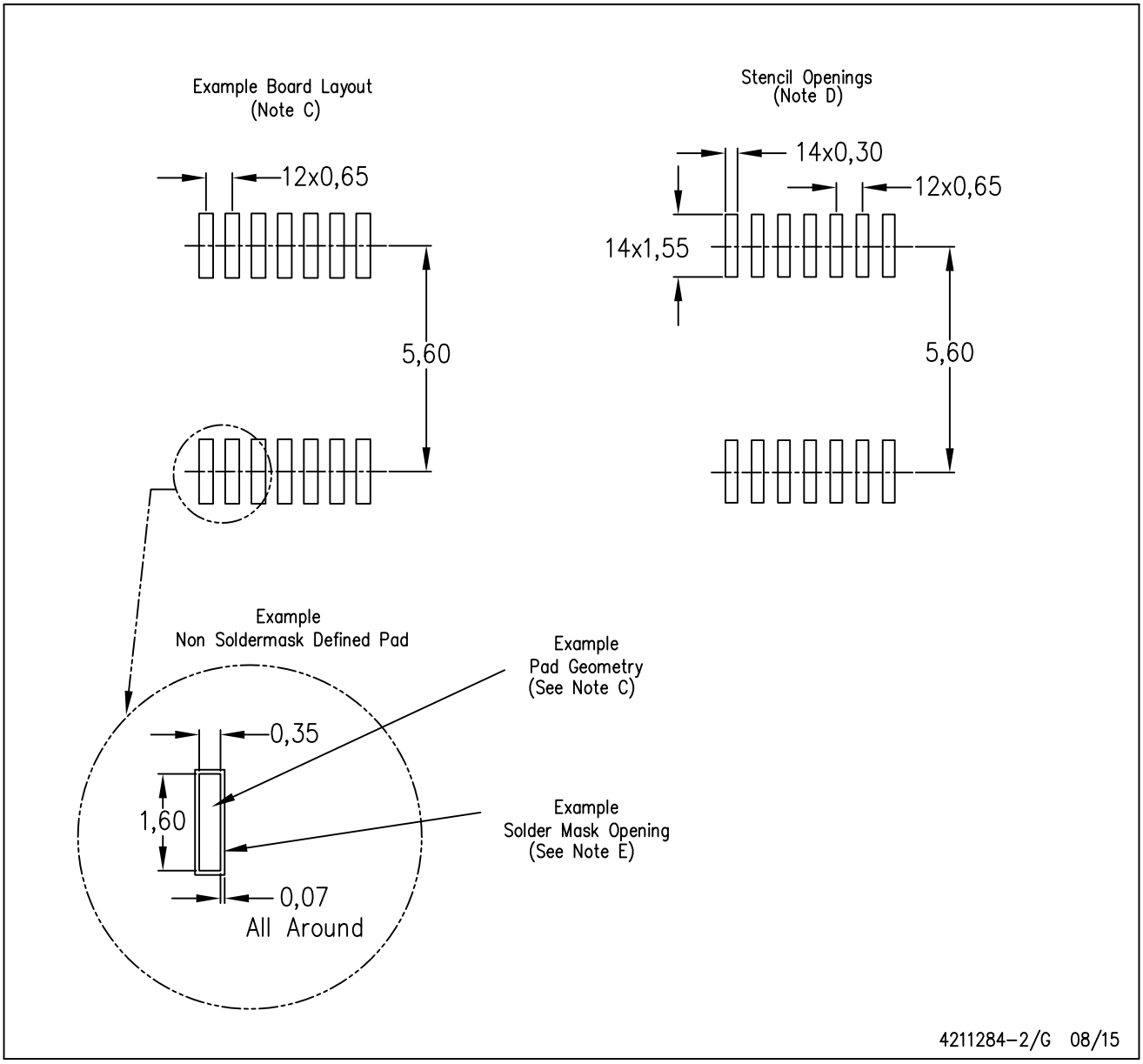
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

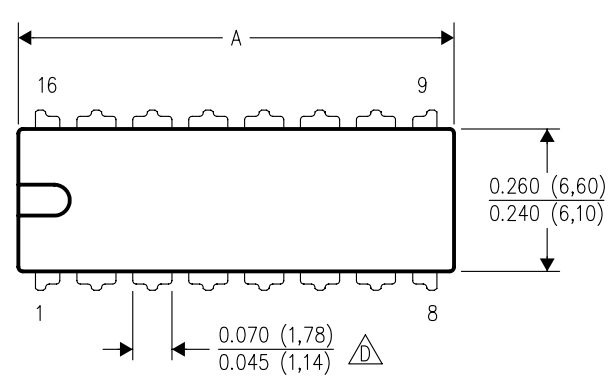



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

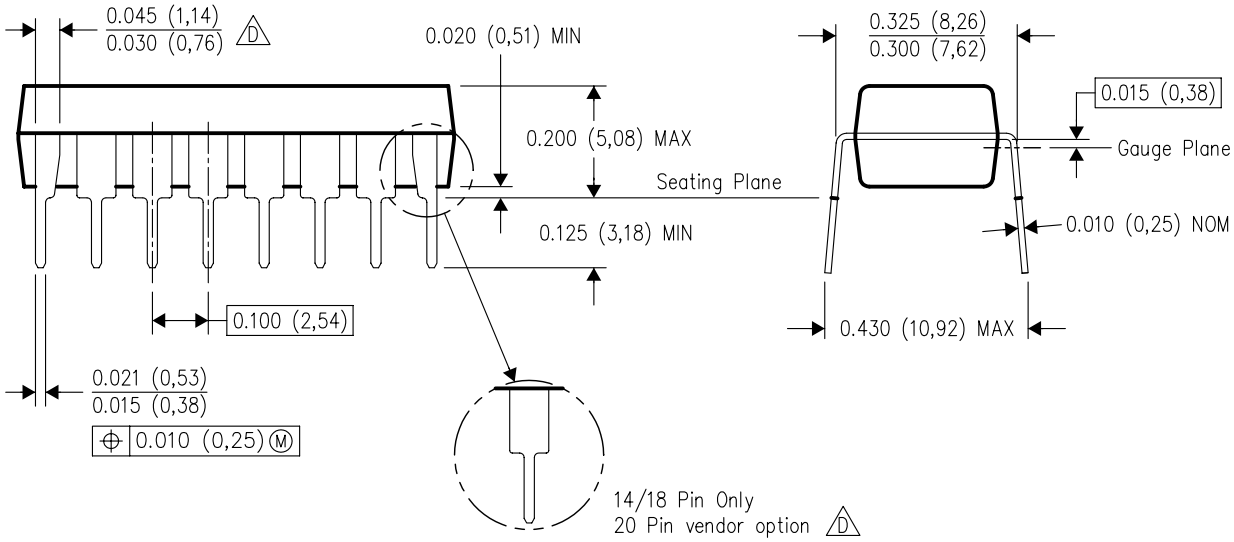
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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