THE DATASHEET OF

LTC1649IS#PBF

3.3V Input High Power Step-Down Switching Regulator Controller

FEATURES

- **High Power 3.3V to 1.xV-2.xV Switching Regulator Controller: Up to 20A Output**
- **All N-Channel External MOSFETs**
- **Provides 5V MOSFET Gate Drive with 3.3V Input**
- **Excellent Output Regulation: ±1% Over Line, Load and Temperature Variations**
- Constant Frequency Operation Minimizes Inductor Size
- High Efficiency: Over 90% Possible
- No Low-Value Sense Resistor Needed
- Available in 16-Lead SO Package

APPLICATIONS

- 3.3V Input Power Supply for Low Voltage Microprocessors and Logic
- Low Input Voltage Power Supplies
- High Power, Low Voltage Regulators
- Local Regulation for Multiple Voltage Distributed Power Systems

DESCRIPTION

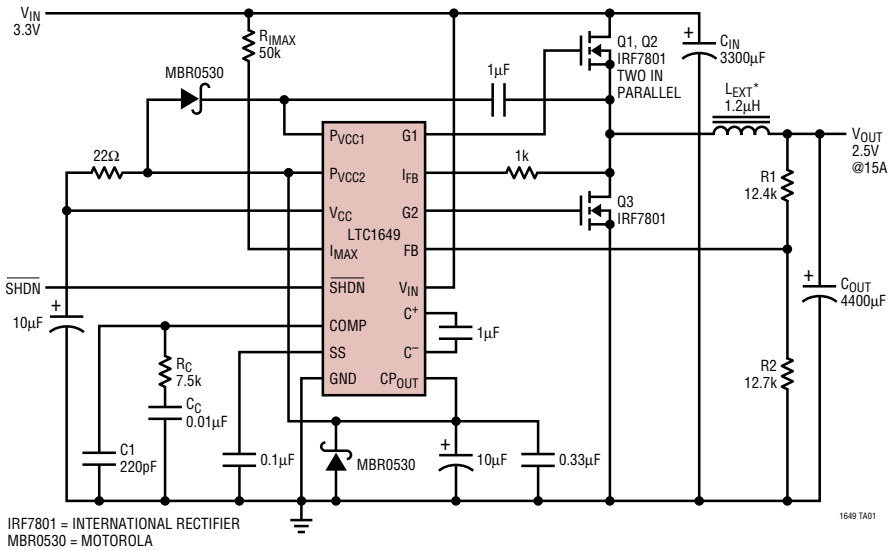
The LTC®1649 is a high power, high efficiency switching regulator controller optimized for use with very low supply voltages. It operates from 2.7V to 5V input, and provides a regulated output voltage from 1.26V to 2.5V at up to 20A load current. A typical 3.3V to 2.5V application features efficiency above 90% from 1A to 10A load. The LTC1649 uses a pair of standard 5V logic-level N-channel external MOSFETs, eliminating the need for expensive P-channel or super-low-threshold devices.

The LTC1649 shares its internal switching architecture with the LTC1430, and features the same ±1% line, load and temperature regulation characteristics. Current limit is user-adjustable without requiring an external low-value sense resistor. The LTC1649 uses a 200kHz switching frequency and voltage mode control, minimizing external component count and size. Shutdown mode drops the quiescent current to below 10µA.

The LTC1649 is available in the 16-pin narrow SO package.

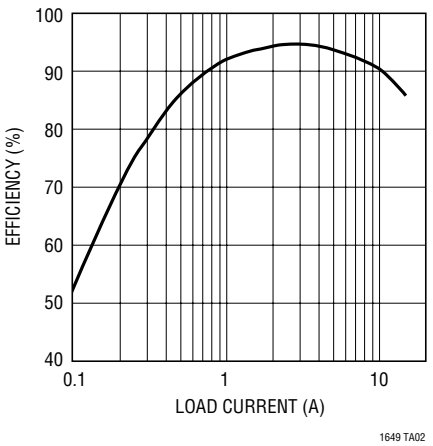
TYPICAL APPLICATION

3.3V to 2.5V, 15A Converter



IRF7801 = INTERNATIONAL RECTIFIER
MBR0530 = MOTOROLA
*12TS-1R2HL = PANASONIC

LTC1649 Efficiency



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

V_{IN} 6V

V_{CC} 9V

$P_{VCC1, 2}$ 13V

Input Voltage

I_{FB} ..... –0.3V to 18V

C^+, C^- ..... –0.3V to (V_{IN} + 0.3V)

All Other Inputs ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range

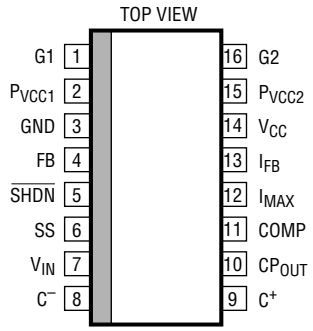
LTC1649C ..... 0°C to 70°C

LTC1649I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1649CS
LTC1649IS

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V (Note 2)

SYMBOL	PARAMETER	CONDITIONS		LTC1649CS MIN	LTC1649CS TYP	LTC1649CS MAX	LTC1649IS MIN	LTC1649IS TYP	LTC1649IS MAX	UNITS
V_{IN}	Minimum Supply Voltage	Figure 1 (Note 3)	●	2.7			2.7			V
V_{FB}	Feedback Voltage	Figure 1	●	1.25	1.265	1.28	1.23	1.265	1.29	V
V_{CPOUT}	Charge Pump Output Voltage	Figure 1	●	4.8	5	5.2	4.75	5	5.25	V
I_{IN}	Supply Current (V_{IN})	$V_{\overline{SHDN}}$ = V_{CC}, I_{LOAD} = 0 $V_{\overline{SHDN}}$ = 0V	●		3 10	5 25		3 10	5 25	mA µA
$I_{PVCC1, 2}$	Supply Current ($P_{VCC1, 2}$)	P_{VCC} = 5V, $V_{\overline{SHDN}}$ = V_{CC} (Note 4) $V_{\overline{SHDN}}$ = 0V			1.5 0.1			1.5 0.1		mA µA
f_{CP}	Internal Charge Pump Frequency	I_{CPOUT} = 20mA (Note 5)			700			700		kHz
f_{OSC}	Internal PWM Oscillator Frequency		●	140	200	260	130	200	325	kHz
V_{IH}	$\overline{SHDN}$ Input High Voltage		●	2.4			2.4			V
V_{IL}	$\overline{SHDN}$ Input Low Voltage		●			0.8			0.8	V
I_{IN}	$\overline{SHDN}$ Input Current		●		±0.01	±1		±0.01	±1	µA
gm_V	Error Amplifier Transconductance				650			650		µMho
gm_I	I_{LIM} Amplifier Transconductance	(Note 6)			1300			1300		µMho
I_{IMAX}	I_{MAX} Sink Current	V_{IMAX} = V_{CC}	●	8	12	16	8	12	17	µA
I_{SS}	Soft Start Source Current	V_{SS} = 0V	●	–8	–12	–16	–8	–12	–17	µA
t_r, t_f	Driver Rise/Fall Time	P_{VCC1} = P_{VCC2} = 5V (Note 7)			80	250		80	250	ns
t_{NOV}	Driver Non-Overlap Time	P_{VCC1} = P_{VCC2} = 5V		25	130	250	25	130	250	ns
DC_{MAX}	Maximum Duty Cycle	V_{COMP} = V_{CC}		90.5	93		90.5	93		%

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a part may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: Maximum Duty Cycle limitations will limit the output voltage obtainable at very low supply voltages.

Note 4: Supply current at P_{VCC1} and P_{VCC2} is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with the operating voltage and the external MOSFETs used.

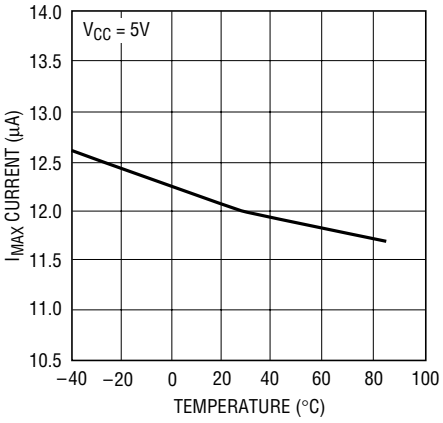
Note 5: Under normal operating conditions, the charge pump will skip cycles to maintain regulation and the apparent frequency will be lower than 700kHz.

Note 6: The I_{LIM} amplifier can sink but not source current. Under normal (not current limited) operation, the I_{LIM} output current will be zero.

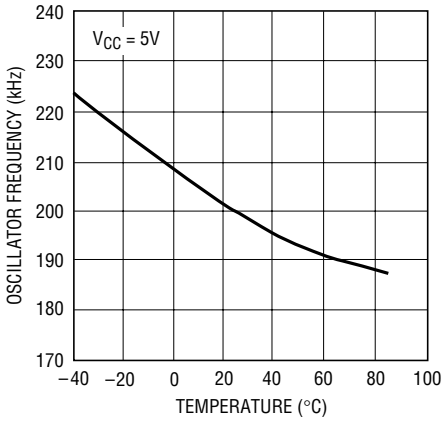
Note 7: Driver rise and fall times are measured from 10% to 90%.

TYPICAL PERFORMANCE CHARACTERISTICS

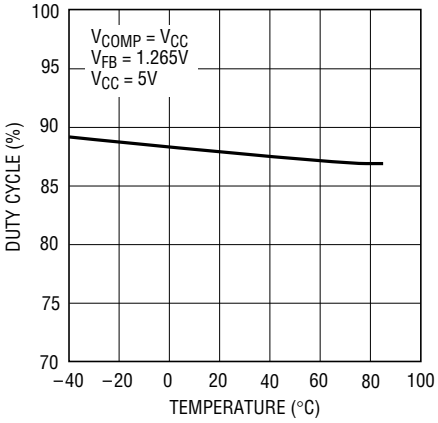
I_{MAX} Pin Current vs Temperature



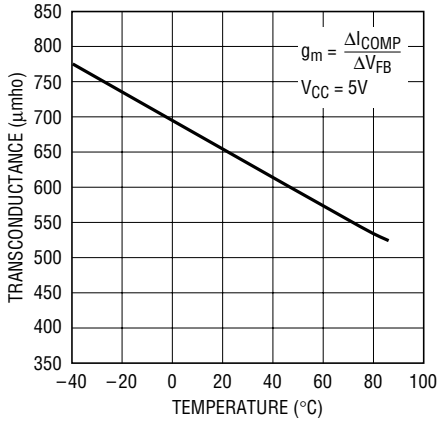
Oscillator Frequency vs Temperature



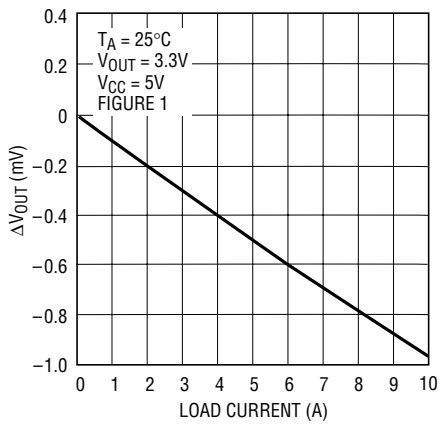
Maximum Duty Cycle vs Temperature



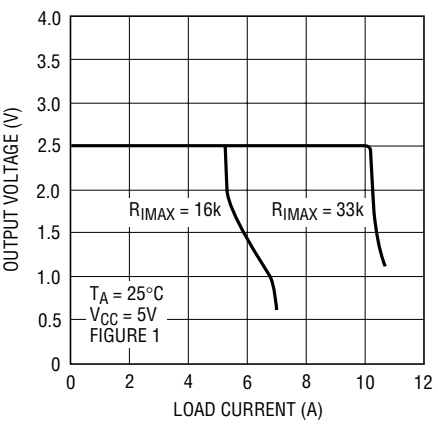
Error Amplifier Transconductance vs Temperature



Load Regulation



Output Voltage vs Load Current with Current Limit



PIN FUNCTIONS

G1 (Pin 1): Driver Output 1. Connect this pin to the gate of the upper N-channel MOSFET, Q1. This output will swing from P_{VCC1} to GND. G1 will always be low when G2 is high. In shutdown, G1 and G2 go low.

P_{VCC1} (Pin 2): Power V_{CC} for Driver 1. This is the power supply input for G1. G1 will swing from P_{VCC1} to GND. P_{VCC1} must be connected to a potential of at least V_{IN} + $V_{GS(ON)}$(Q1). This potential can be generated using a simple charge pump connected to the switching node between the two external MOSFETs as shown in Figure 1.

GND (Pin 3): System Ground. Connect to a low impedance ground in close proximity to the source of Q2. The system signal and power grounds should meet at only one point, at the GND pin of the LTC1649.

FB (Pin 4): Feedback. The FB pin is connected to the output through a resistor divider to set the output voltage. $V_{OUT} = V_{REF}$ [1 + (R1/R2)].

$\overline{SHDN}$ (Pin 5): Shutdown, Active Low. A TTL compatible LOW level at $\overline{SHDN}$ for more than 50µs puts the LTC1649 into shutdown mode. In shutdown, G1, G2, COMP and SS go low, and the quiescent current drops to 25µA max. CP_{OUT} remains at 5V in shutdown mode. A TTL compatible HIGH level at $\overline{SHDN}$ allows the LTC1649 to operate normally.

SS (Pin 6): Soft Start. An external capacitor from SS to GND controls the startup time and also compensates the current limit loop, allowing the LTC1649 to enter and exit current limit cleanly.

V_{IN} (Pin 7): Charge Pump Input. This is the main low voltage power supply input. V_{IN} requires an input voltage between 3V and 5V. Bypass V_{IN} to ground with a 1µF ceramic capacitor located close to the LTC1649.

C^- (Pin 8): Flying Capacitor, Negative Terminal. Connect a 1µF ceramic capacitor from C^- to C^+.

C^+ (Pin 9): Flying Capacitor, Positive Terminal.

CP_{OUT} (Pin 10): Charge Pump Output. CP_{OUT} provides a regulated 5V output to provide power for the internal switching circuitry and gate drive for the external MOSFETs. CP_{OUT} should be connected directly to P_{VCC2} in most applications. At least 10µF of reservoir capacitance to ground is required at CP_{OUT}. This requirement can usually be met by the bypass capacitor at P_{VCC2}.

COMP (Pin 11): External Compensation. The COMP pin is connected directly to the output of the internal error amplifier and the input of the PWM generator. An RC network is used at this node to compensate the feedback loop to provide optimum transient response.

I_{MAX} (Pin 12): Current Limit Set. I_{MAX} sets the threshold for the internal current limit comparator. If I_{FB} drops below I_{MAX} with G1 on, the LTC1649 will go into current limit. I_{MAX} has an internal 12µA pull-down to GND. The voltage at I_{MAX} can be set with an external resistor to the drain of Q1 or with an external voltage source.

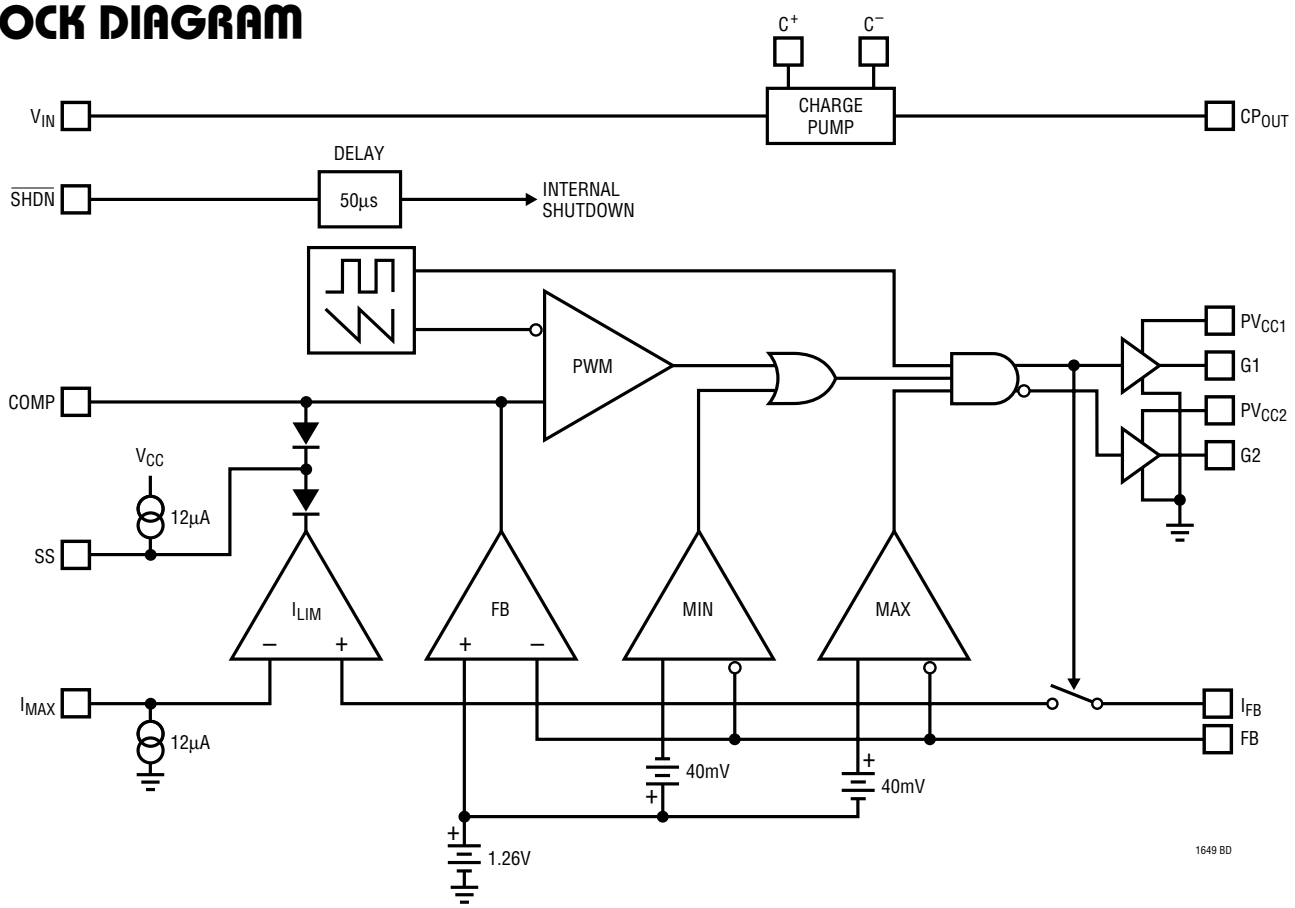
I_{FB} (Pin 13): Current Limit Sense. Connect to the switched node at the source of Q1 and the drain of Q2 through a 1kΩ resistor. The resistor is required to prevent voltage transients at the switched node from damaging the I_{FB} pin. I_{FB} can be taken up to 18V above GND without damage.

V_{CC} (Pin 14): Internal Power Supply. V_{CC} provides power to the feedback amplifier and switching control circuits. V_{CC} is designed to run from the 5V supply provided by CP_{OUT}. V_{CC} requires a 10µF bypass capacitor to GND.

P_{VCC2} (Pin 15): Power V_{CC} for Driver 2. This is the power supply input for G2. G2 will swing from P_{VCC2} to GND. P_{VCC2} must be connected to a potential of at least $V_{GS(ON)}$(Q2). This voltage is usually supplied by the CP_{OUT} pin. P_{VCC2} requires a bypass capacitor to GND; this capacitor also provides the reservoir capacitance required by the CP_{OUT} pin.

G2 (Pin 16): Driver Output 2. Connect this pin to the gate of the lower N-channel MOSFET, Q2. This output will swing from P_{VCC2} to GND. G2 will always be low when G1 is high. In shutdown, G1 and G2 go low.

BLOCK DIAGRAM



TEST CIRCUIT

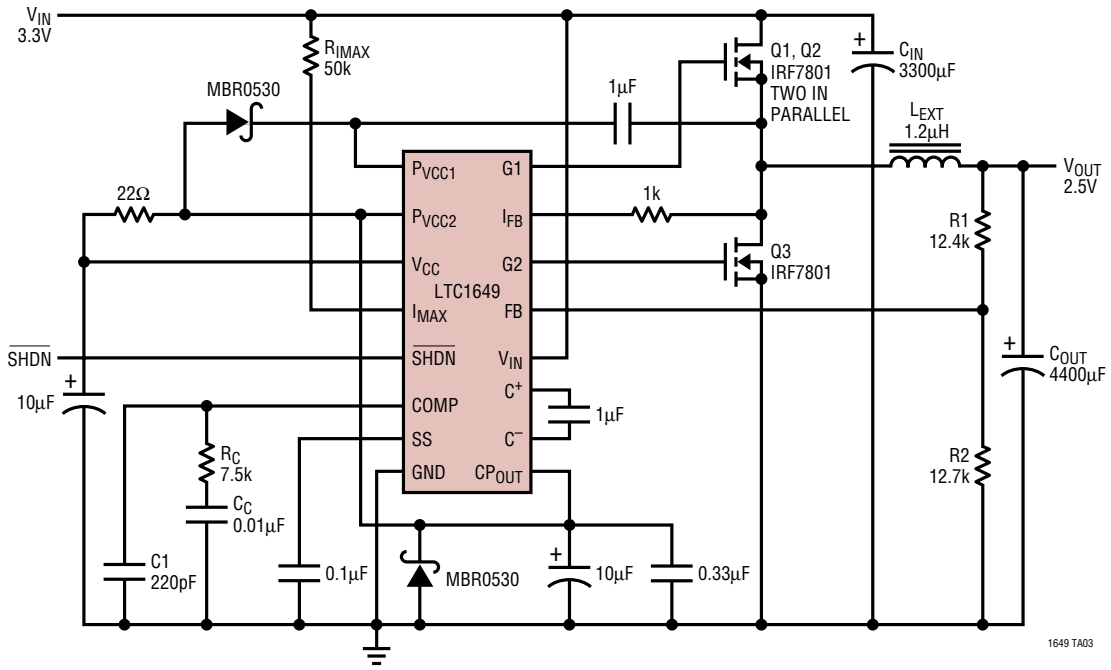


Figure 1

APPLICATIONS INFORMATION

OVERVIEW

The LTC1649 is a voltage feedback PWM switching regulator controller (see Block Diagram) designed for use in high power, low input voltage step-down (buck) converters. It includes an onboard PWM generator, a precision reference trimmed to ±0.5%, two high power MOSFET gate drivers and all necessary feedback and control circuitry to form a complete switching regulator circuit. Also included is an internal charge pump which provides 5V gate drive to the external MOSFETs with input supply voltage as low as 2.7V. The LTC1649 runs at an internally fixed 200kHz clock frequency and requires an external resistor divider to set the output voltage.

The LTC1649 includes a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor. Also included is an internal soft start feature that requires only a single external capacitor to operate.

THEORY OF OPERATION

Primary Feedback Loop

The LTC1649 senses the output voltage of the circuit at the output capacitor through a resistor divider connected to the FB pin and feeds this voltage back to the internal transconductance amplifier FB. FB compares the resistor-divided output voltage to the internal 1.26V reference and outputs an error signal to the PWM comparator. This is then compared to a fixed frequency sawtooth waveform generated by the internal oscillator to generate a pulse width modulated signal. This PWM signal is fed back to the external MOSFETs through G1 and G2, closing the loop. Loop compensation is achieved with an external compensation network at COMP, the output node of the FB transconductance amplifier.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the FB amplifier may not respond quickly enough. MIN compares the feedback signal to a voltage 40mV (3%) below the internal reference. At this point, the MIN comparator overrides the FB amplifier and forces the loop to full duty cycle, set by the internal oscillator at about 93%. Similarly, the MAX comparator monitors the output voltage at 3% above the internal reference and forces the output to 0% duty cycle when tripped. These two comparators prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

Current Limit Loop

The LTC1649 includes yet another feedback loop to control operation in current limit. The I_{LIM} amplifier monitors the voltage drop across external MOSFET Q1 with the I_{FB} pin during the portion of the cycle when G1 is high. It compares this voltage to the voltage at the I_{MAX} pin. As the peak current rises, the drop across Q1 due to its $R_{DS(ON)}$ increases. When I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, I_{LIM} starts to pull current out of the external soft start capacitor, cutting the duty cycle and controlling the output current level. At the same time, the I_{LIM} comparator generates a signal to disable the MIN comparator to prevent it from conflicting with the current limit circuit. If the internal feedback node drops below about 0.8V, indicating a severe output overload, the circuitry will force the internal oscillator to slow down by a factor of as much as 100. If desired, the turn on time of the current limit loop can be controlled by adjusting the size of the soft start capacitor, allowing the LTC1649 to withstand brief overcurrent conditions without limiting.

By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limit circuit eliminates the sense resistor that would otherwise be required and minimizes the number of components in the external high current path. Because power MOSFET $R_{DS(ON)}$ is not tightly controlled and varies with temperature, the LTC1649 current limit is not designed to be accurate; it is meant to prevent damage to the power supply circuitry during fault conditions. The actual current level where the limiting circuit begins to take effect may vary from unit to unit, depending on the power MOSFETs used. See Soft Start and Current Limit for more details on current limit operation.

APPLICATIONS INFORMATION

MOSFET Gate Drive

The LTC1649 is designed to operate from supplies as low as 2.7V while using standard 5V logic-level N-channel external MOSFETs. This poses somewhat of a challenge—from as little as 2.7V, the LTC1649 must provide a 0V to 5V signal to the lower MOSFET, Q2, while the upper MOSFET, Q1, requires a gate drive signal that swings from 0V to (V_{IN} + 5V). The LTC1649 addresses this situation with two specialized circuits. An onboard charge pump boosts the input voltage at V_{IN} to a regulated 5V at CP_{OUT}. This 5V supply is used to power the PV_{CC2} pin, which in turn supplies 5V gate drive to Q2. This 5V supply is also used to power the V_{CC} pin, which allows the internal drive circuitry to interface to the boosted driver supplies.

Gate drive for the top N-channel MOSFET, Q1, is supplied by PV_{CC1}. This supply must reach V_{IN} + 5V while Q1 is on. Conveniently, the switching node at the source of Q1 rises to V_{IN} whenever Q1 is on. The LTC1649 uses this fact to generate the required voltage at PV_{CC1} with a simple external charge pump as shown in Figure 2. This circuit charges the flying capacitor C2 to the 5V level at CP_{OUT} when the switching node is low. As the top MOSFET turns on, the switching node begins to rise to V_{IN}, and the PV_{CC1} is pulled up to V_{IN} + 5V by C2. The 93% maximum duty cycle (typical) means the switching node at the source of Q1 will return to ground during at least 7% of each cycle, ensuring that the charge pump will always provide adequate gate drive to Q1.

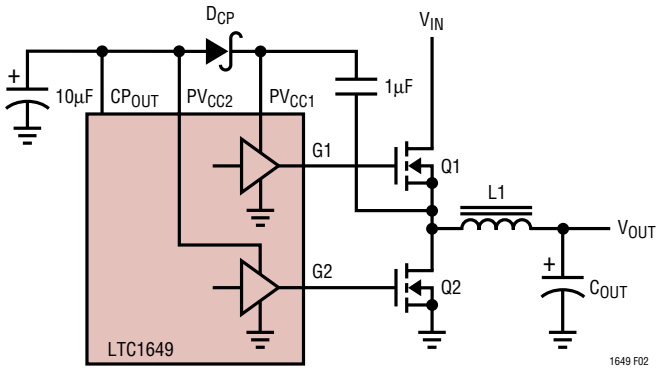


Figure 2. PV_{CC1} Charge Pump

Synchronous Operation

The LTC1649 uses a synchronous switching architecture, with MOSFET Q2 taking the place of the diode in a classic buck circuit (Figure 3). This improves efficiency by reducing the voltage drop and the resultant power dissipation across Q2 to $V_{ON} = (I)(R_{DS(ON)(Q2)})$, usually much lower than V_F of the diode in the classical circuit. This more than offsets the additional gate drive required by the second MOSFET, allowing the LTC1649 to achieve efficiencies in the mid-90% range for a wide range of load currents.

Another feature of the synchronous architecture is that unlike a diode, Q2 can conduct current in either direction. This allows the output of a typical LTC1649 circuit to sink current as well as sourcing it while remaining in regulation. The ability to sink current at the output allows the LTC1649 to be used with reactive or other nonconventional loads that may supply current to the regulator as well as drawing current from it.

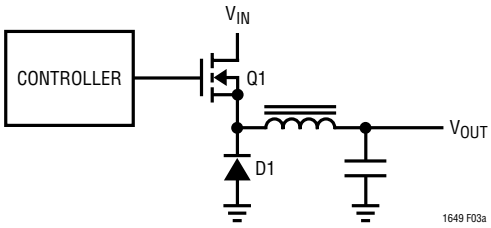


Figure 3a. Classical Buck Architecture

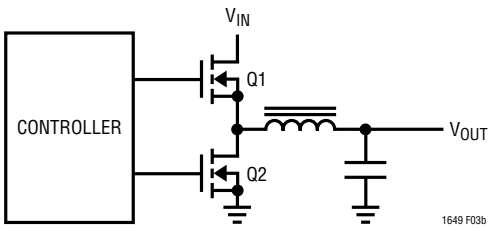


Figure 3b. Synchronous Buck Architecture

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION

Power MOSFETs

Two N-channel power MOSFETs are required for most LTC1649 circuits. These should be selected primarily by on-resistance considerations; thermal dissipation is often a secondary concern in high efficiency designs. The LTC1649 is designed to be used with 5V logic-level MOSFETs; "standard" threshold MOSFETs with $R_{DS(ON)}$ specified at 10V only will not provide satisfactory performance.

MOSFET $R_{DS(ON)}$ should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. In a typical LTC1649 buck converter circuit operating in continuous mode, the average inductor current is equal to the output load current. This current is always flowing through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC\ (Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC\ (Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The R_{ON} required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$:

$$R_{DS(ON)}\ (Q1) = \frac{P_{MAX}(Q1)}{DC(Q1)(I_{MAX}^2)} = \frac{V_{IN}(P_{MAX})(Q1)}{V_{OUT}(I_{MAX}^2)}$$

$$R_{DS(ON)}\ (Q2) = \frac{P_{MAX}(Q2)}{DC(Q2)(I_{MAX}^2)} = \frac{V_{IN}(P_{MAX})(Q2)}{(V_{IN} - V_{OUT})(I_{MAX}^2)}$$

P_{MAX} should be calculated based primarily on required efficiency. A typical high efficiency circuit designed for 3.3V in, 2.5V at 10A out might require no more than 3% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of (2.5V)(10A/0.9)(0.03) = 833mW per FET and a required R_{DSON} of:

$$R_{DS(ON)}\ (Q1) = \frac{(3.3V)(833mW)}{(2.5V)(10A^2)} = 0.011\Omega$$

$$R_{DS(ON)}\ (Q2) = \frac{(3.3V)(833mW)}{(3.3V - 2.5V)(10A^2)} = 0.034\Omega$$

Note that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the dissipation numbers are less than a watt per device— large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY and International Rectifier IRF7801 are two small, surface mount devices with R_{ON} values of 0.03Ω or below with 5V of gate drive; both work well in LTC1649 circuits. A higher P_{MAX} value will generally decrease MOSFET cost and circuit efficiency and increase MOSFET heat sink requirements.

Inductor

The inductor is often the largest component in an LTC1649 design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of the current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the LTC1649. In a typical 3.3V to 2.5V application, the maximum rise time will be:

$$93\%\ \frac{(V_{IN} - V_{OUT})}{L}\ \frac{AMPS}{SECOND} = \frac{0.744A}{\mu s}\ \frac{I}{L}$$

where L is the inductor value in µH. A 2µH inductor would have a 0.37A/µs rise time in this application, resulting in a 14µs delay in responding to a 5A load current step. During this 14µs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most typical 3.3V to 2.xV LTC1649 circuits. Different combinations of input and output volt-

APPLICATIONS INFORMATION

ages and expected loads may require different values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current added to half the peak-to- peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. If the efficiency is high and can be considered approximately equal to 1, the ripple current is approximately equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT})}{(f_{OSC})(L)} DC$$

$$DC = \frac{V_{OUT}}{V_{IN}}$$

f_{OSC} = LTC1649 oscillator frequency = 200kHz
L = inductor value

Solving this equation with our typical 3.3V to 2.5V application, we get:

$$\frac{(0.8)(0.76)}{(200kHz)(2\mu H)} = 1.5A_{P-P}$$

Peak inductor current at 10A load:

$$10A + \frac{1.5A}{2} = 10.8A$$

The inductor core must be adequate to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that the current may rise above this maximum level in circuits under current limit or under fault conditions in unlimited circuits; the inductor should be sized to withstand this additional current.

Input and Output Capacitors

A typical LTC1649 design puts significant demands on both the input and output capacitors. Under normal steady load operation, a buck converter like the LTC1649 draws square waves of current from the input supply at the switching frequency, with the peak value equal to the output current and the minimum value near zero. Most of this current must come from the input bypass capacitor, since few raw supplies can provide the current slew rate to feed such a load directly. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (3 months) lifetime; further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit.

The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually a fraction of the total load current. Output capacitor duty places a premium not on power dissipation but on low ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC1649 can adjust the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. A 5A load step with a 0.05Ω ESR output capacitor will result in a 250mV output voltage shift; this is a 10% output voltage shift for a 2.5V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC1649 applications. OS-CON electrolytic capacitors from Sanyo give excellent performance and have a very high performance/size ratio for an electrolytic capacitor. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies; low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular tantalum capaci-

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tors that work well in LTC1649 applications. A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC1649 application might require an input capacitor with a 5A ripple current capacity and 2% output shift with a 10A output load step, which requires a 0.005Ω output capacitor ESR. Sanyo OS-CON part number 10SA220M (220µF/10V) capacitors feature 2.3A allowable ripple current at 85°C and 0.035Ω ESR; three in parallel at the input and seven at the output will meet the above requirements.

Input Supply Considerations/Charge Pump

The LTC1649 requires four supply voltages to operate: V_{IN}, V_{CC}, PV_{CC1} and PV_{CC2}. V_{IN} is the primary high power input, supplying current to the drain of Q1 and the input to the internal charge pump at the V_{IN} pin. This supply must be between 2.7V and 6V for the LTC1649 to operate properly. An internal charge pump uses the voltage at V_{IN} to generate a regulated 5V output at CP_{OUT}. This charge pump requires an external 1µF capacitor connected between the C^+ and C^- pins, and an external 10µF reservoir capacitor connected from CP_{OUT} to ground. The voltage at CP_{OUT} must always be greater than or equal to V_{IN}. If V_{IN} is expected to rise above 5V, an additional Schottky diode (D5) should be added from V_{IN} to CP_{OUT}.

CP_{OUT} is typically connected to PV_{CC2} directly, providing the 5V supply that the G2 driver output uses to drive Q2. PV_{CC2} requires a 10µF bypass to ground; this capacitor can double as the CP_{OUT} reservoir capacitor, allowing a typical application with CP_{OUT} and PV_{CC2} connected together to get away with only a single 10µF capacitor at this node, located close to the PV_{CC2} pin. V_{CC} can also be powered from CP_{OUT}, but is somewhat sensitive to noise. PV_{CC2} happens to be a significant noisemaker, so most applications require an RC filter from CP_{OUT}/PV_{CC2} to V_{CC}. 22Ω and 10µF are typical filter values that work well in most applications.

PV_{CC1} needs to be boosted to a level higher than CP_{OUT} to provide gate drive to Q1. The LTC1649 initially used a charge pump from V_{IN} to create CP_{OUT}; the typical application uses a second charge pump to generate the PV_{CC1} supply. This second charge pump consists of a Schottky diode (D_{CP}) from CP_{OUT} to PV_{CC1}, and a 1µF capacitor from PV_{CC1} to the source of Q1. While Q2 is on, the diode charges the capacitor to CP_{OUT}. When Q1 comes on, its source rises to V_{IN}, and the cap hauls PV_{CC1} up to (CP_{OUT} + V_{IN}), adequate to fully turn on Q1. When Q1 turns back off, PV_{CC1} drops back down to CP_{OUT}; fortunately, we're not interested in turning Q1 on at this point, so the lower voltage doesn't cause problems. The next time Q1 comes on, PV_{CC1} bounces back up to (CP_{OUT} + V_{IN}), keeping Q1 happy. Figure 4 shows a complete power supply circuit for the LTC1649.

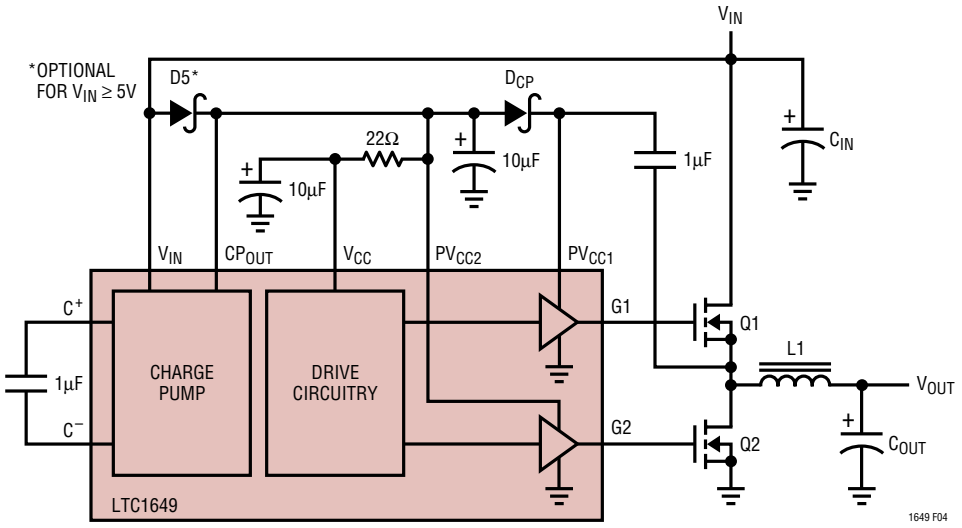

Figure 4. LTC1649 Power Supplies

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The CP_{OUT} pin can typically supply 50mA at 5V, adequate to power the V_{CC} and PV_{CC} pins. This supply can also be used to power external circuitry, but any additional current drawn from CP_{OUT} subtracts from the current available to drive the external MOSFETs. Circuits with small external MOSFETs can draw as much as 20mA or 30mA from CP_{OUT} without hindering performance. High output current circuits with large or multiple external MOSFETs may need every milliamp they can get from CP_{OUT}, and external loads should be minimized. The charge pump at PV_{CC1} is more limited in its abilities, and should not be connected to anything except PV_{CC1}. In particular, do not connect a bypass capacitor from PV_{CC1} to ground—it will steal charge from the charge pump and actually degrade performance.

Compensation and Transient Response

The LTC1649 voltage feedback loop is compensated at the COMP pin; this is the output node of the internal g_m error amplifier. The loop can generally be compensated properly with an RC network from COMP to GND and an additional small C from COMP to GND (Figure 5). Loop stability is affected by inductor and output capacitor values and by other factors. Optimum loop response can be obtained by using a network analyzer to find the loop poles and zeros; nearly as effective and a lot easier is to empirically tweak the R_C values until the transient recovery looks right with an output load step.

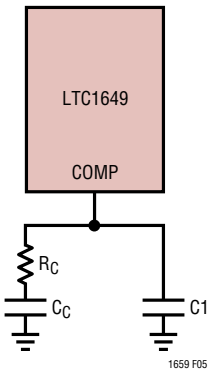

Figure 5. Compensation Pin Hook-Up

Output transient response is set by three major factors: the time constant of the inductor and the output capacitor, the ESR of the output capacitor, and the loop compensation components. The first two factors usually have much more impact on overall transient recovery time than the third; unless the loop compensation is way off, more improvement can be had by optimizing the inductor and the output capacitor than by fiddling with the loop compensation components. In general, a smaller value inductor will improve transient response at the expense of ripple and inductor core saturation rating. Minimizing output capacitor ESR will also help optimize output transient response. See Input and Output Capacitors for more information.

Soft Start and Current Limit

The LTC1649 includes a soft start circuit at the SS pin; this circuit is used both for initial start-up and during current limit operation. SS requires an external capacitor to GND with the value determined by the required soft start time. An internal 12μA current source is included to charge the external capacitor. Soft start functions by clamping the maximum voltage that the COMP pin can swing to, thereby controlling the duty cycle (Figure 6). The LTC1649 will begin to operate at low duty cycle as the SS pin rises to about 2V below the V_{CC} pin. As SS continues to rise, the duty cycle will increase until the error amplifier takes over and begins to regulate the output. When SS reaches 1V below V_{CC} the LTC1649 will be in full operation. An internal switch shorts the SS pin to GND during shutdown.

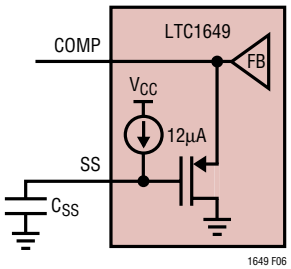

Figure 6. Soft Start Clamps COMP Pin

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The LTC1649 detects the output current by watching the voltage at I_{FB} while Q1 is ON. The I_{LIM} amplifier compares this voltage to the voltage at I_{MAX} (Figure 7). In the ON state, Q1 has a known resistance; by calculating backwards, the voltage generated at I_{FB} by the maximum output current in Q1 can be determined. As I_{FB} falls below I_{MAX}, I_{LIM} will begin to sink current from the soft start pin, causing the voltage at SS to fall. As SS falls, it will limit the output duty cycle, limiting the current at the output. Eventually the system will reach equilibrium, where the pull-up current at the SS pin matches the pull-down current in the I_{LIM} amplifier; the LTC1649 will stay in this state until the overcurrent condition disappears. At this time I_{FB} will rise, I_{LIM} will stop sinking current and the internal pull-up will recharge the soft start capacitor, restoring normal operation. Note that the I_{FB} pin requires an external 1k series resistor to prevent voltage transients at the drain of Q2 from damaging internal structures.

The I_{LIM} amplifier pulls current out of SS in proportion to the difference between I_{FB} and I_{MAX}. Under mild overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not trip the current limit circuit at all. Longer overload conditions will allow the SS pin to reach a steady level, and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a larger overdrive at I_{LIM}, allowing it to pull SS down more quickly and preventing damage to the output components.

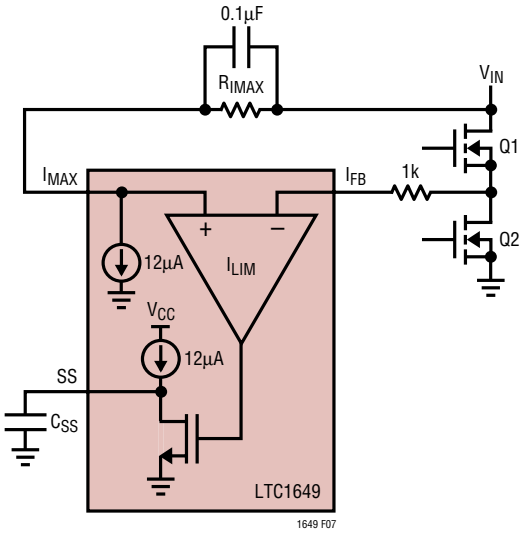

Figure 7. Current Limit Operation

The I_{LIM} amplifier output is disabled when Q1 is OFF to prevent the low I_{FB} voltage in this condition from activating the current limit. It is re-enabled a fixed 170ns after Q1 turns on; this allows for the I_{FB} node to slew back high and the I_{LIM} amplifier to settle to the correct value. As the LTC1649 goes deeper into current limit, it will reach a point where the Q1 on-time needs to be cut to below 170ns to control the output current. This conflicts with the minimum settling time needed for proper operation of the I_{LIM} amplifier. At this point, a secondary current limit circuit begins to reduce the internal oscillator frequency, lengthening the off-time of Q1 while the on-time remains constant at 170ns. This further reduces the duty cycle, allowing the LTC1649 to maintain control over the output current.

Under extreme output overloads or short circuits, the I_{LIM} amplifier will pull the SS pin more than 2V below V_{CC} in a single switching cycle, cutting the duty cycle to zero. At this point all switching stops, the output current decays through Q2 and the LTC1649 runs a partial soft start cycle and restarts. If the short is still present the cycle will repeat. Peak currents can be quite high in this condition, but the average current is controlled and a properly designed circuit can withstand short circuits indefinitely with only moderate heat rise in the output FETs. In addition, the soft start cycle repeat frequency can drop into the low kHz range, causing vibrations in the inductor which provide an audible alarm that something is wrong.

Shutdown

The LTC1649 includes a low power shutdown mode, controlled by the logic at the SHDN pin. A high at $\overline{SHDN}$ allows the part to operate normally. A low level at $\overline{SHDN}$ stops all internal switching, pulls COMP and SS to ground internally and turns Q1 and Q2 off. In shutdown, the LTC1649 itself will drop below 25µA quiescent current typically, although off-state leakage in the external MOSFETs may cause the total V_{IN} current to be somewhat higher, especially at elevated temperatures. When $\overline{SHDN}$ rises again, the LTC1649 will rerun a soft start cycle and

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resume normal operation. The CP_{OUT} pin remains regulated at 5V in shutdown, and can be used as a keep-alive supply for external circuitry if desired. Note that any current drawn from the CP_{OUT} pin adds to the quiescent current in shutdown, and subtracts from the current available to drive the external MOSFETs if the load remains connected while the LTC1649 is active.

External Clock Synchronization

The LTC1649 $\overline{SHDN}$ pin can double as an external clock input for applications that require a synchronized clock or a faster switching speed. The $\overline{SHDN}$ pin terminates the internal sawtooth wave and resets the oscillator immediately when it goes low, but waits 50µs before shutting down the rest of the internal circuitry. A clock signal applied directly to the $\overline{SHDN}$ pin will force the LTC1649 internal oscillator to lock to its frequency as long as the external clock runs faster than the internal oscillator frequency. The LTC1649 can be synchronized to frequencies between 250kHz and about 350kHz.

Frequencies above 350kHz can cause erratic current limit operation and are not recommended.

Setting the Output Voltage

The LTC1649 feedback loop senses the output voltage at the FB pin. The loop regulates FB to 1.265V; to set the output voltage, FB should be connected to the output node through a resistor divider, set up so the voltage at FB is 1.265V when the output is at the desired voltage (see Figure 8). The upper end of R1 should be connected to the output voltage as close to the load as possible, to minimize errors caused by resistance in the output leads. The bottom of R2 should be connected to the high power ground node, at the GND pin of the LTC1649.

R1 and R2 should be chosen so that:

$$V_{OUT} = \frac{R_1 + R_2}{R2} V_{REF} = \frac{R_1 + R_2}{R2} (1.265V)$$

An easy way to simplify the math is to choose R2 = 12.65kΩ. This simplifies the equation to:

$$V_{OUT} = \frac{R_1}{10k\Omega} + 1.265V$$

A typical 2.5V output application might use R1 = 12.35kΩ, R2 = 12.65kΩ. The nearest standard 1% values are R1 = 12.4kΩ, R2 = 12.7kΩ, which gives an output voltage of 2.5001V—pretty close to 2.5V.

Note that using 1% resistors can cause as much as 1% error in the output voltage in a typical LTC1649 application—a significant fraction of the total output error. 0.1% or 0.25% feedback resistors are recommended for applications which require the output voltage to be controlled to better than 3%.

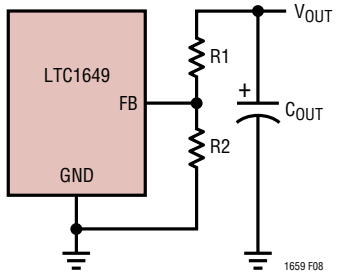


Figure 8. Resistor Divider at FB Pin

LAYOUT CONSIDERATIONS

Grounding

Proper grounding is critical for the LTC1649 to obtain specified output regulation. Extremely high peak currents (as high as several amps) can flow between the bypass capacitors and the PV_{CC1}, PV_{CC2} and GND pins. These currents can generate significant voltage differences between two points that are nominally both "ground." As a general rule, power and signal grounds should be totally separated on the layout, and should be brought together at only one point, right at the LTC1649 GND pin. This helps minimize internal ground disturbances in the LTC1649, while preventing excessive current flow from disrupting the operation of the circuits connected to GND. The high power GND node should be as compact and low impedance as possible, with the negative terminals of the input

APPLICATIONS INFORMATION

and output capacitors, the source of Q2, the LTC1649 GND pin, the output return and the input supply return all clustered at one point. Figure 9 is a modified schematic showing the common connections in a proper layout. Note that at 10A current levels or above, current density in the PC board itself can become a concern; traces carrying high currents should be as wide as possible.

Power Component Hook-Up/Heat Sinking

As current levels rise much above 1A, the power components supporting the LTC1649 start to become physically large (relative to the LTC1649, at least) and can require special mounting considerations. Input and output capacitors need to carry high peak currents and must have low ESR; this mandates that the leads be clipped as short as possible and PC traces be kept wide and short. The power inductor will generally be the most massive single component on the board; it can require a mechanical hold-down in addition to the solder on its leads, especially if it is a surface mount type.

The power MOSFETs used require some care to ensure proper operation and reliability. Depending on the current levels and required efficiency, the MOSFETs chosen may be as large as TO-220s or as small as SO-8s. High efficiency circuits may be able to avoid heat sinking the power devices, especially with TO-220 type MOSFETs. As an example, a 90% efficient converter working at a steady 2.5V/10A output will dissipate only (25W/90%)10% = 2.8W. The power MOSFETs generally account for the majority of the power lost in the converter; even assuming that they consume 100% of the power used by the converter, that's only 2.8W spread over two or three devices. A typical SO-8 MOSFET with a R_{ON} suitable to provide 90% efficiency in this design can commonly dissipate 2W when soldered to an appropriately sized piece of copper trace on a PC board. Slightly less efficient or higher output current designs can often get by with standing a TO-220 MOSFET straight up in an area with some airflow; such an arrangement can dissipate as much as 3W without a heat sink. Designs which must work in high ambient temperatures or which will be routinely overloaded will generally fare best with a heat sink.

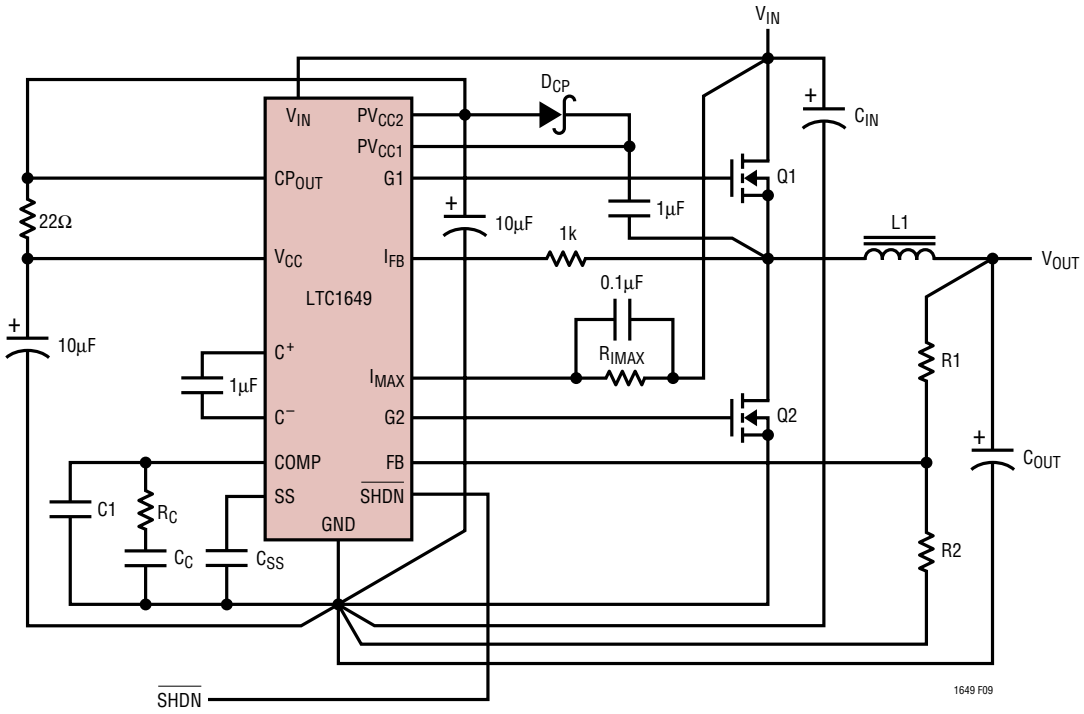
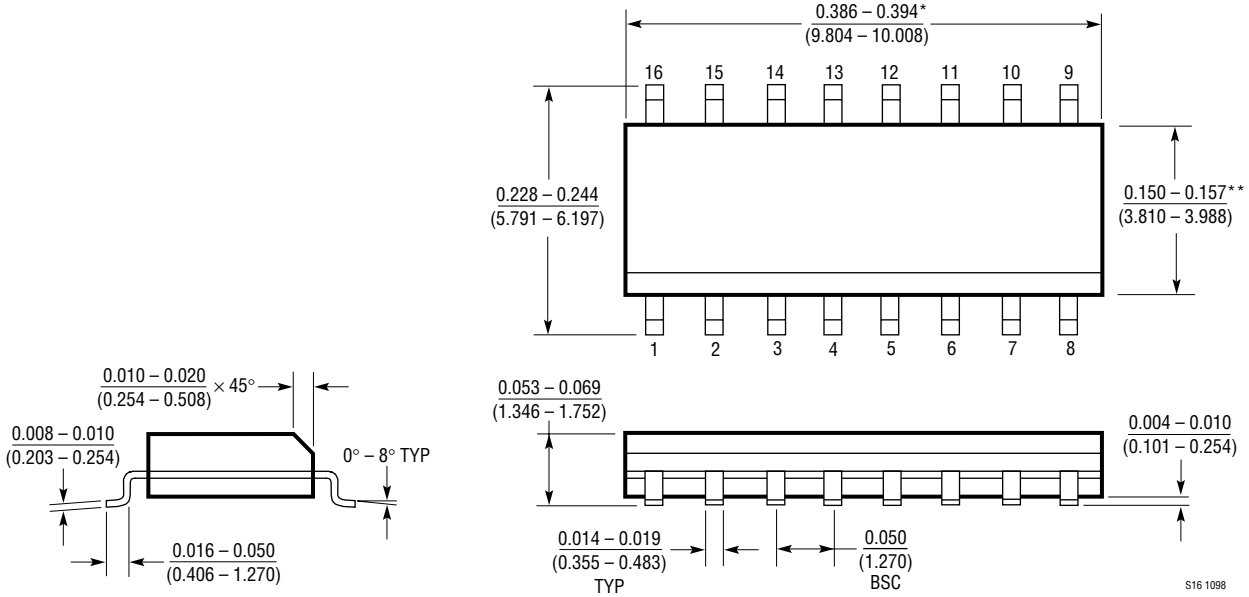


Figure 9. Typical Schematic Showing Layout Considerations

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

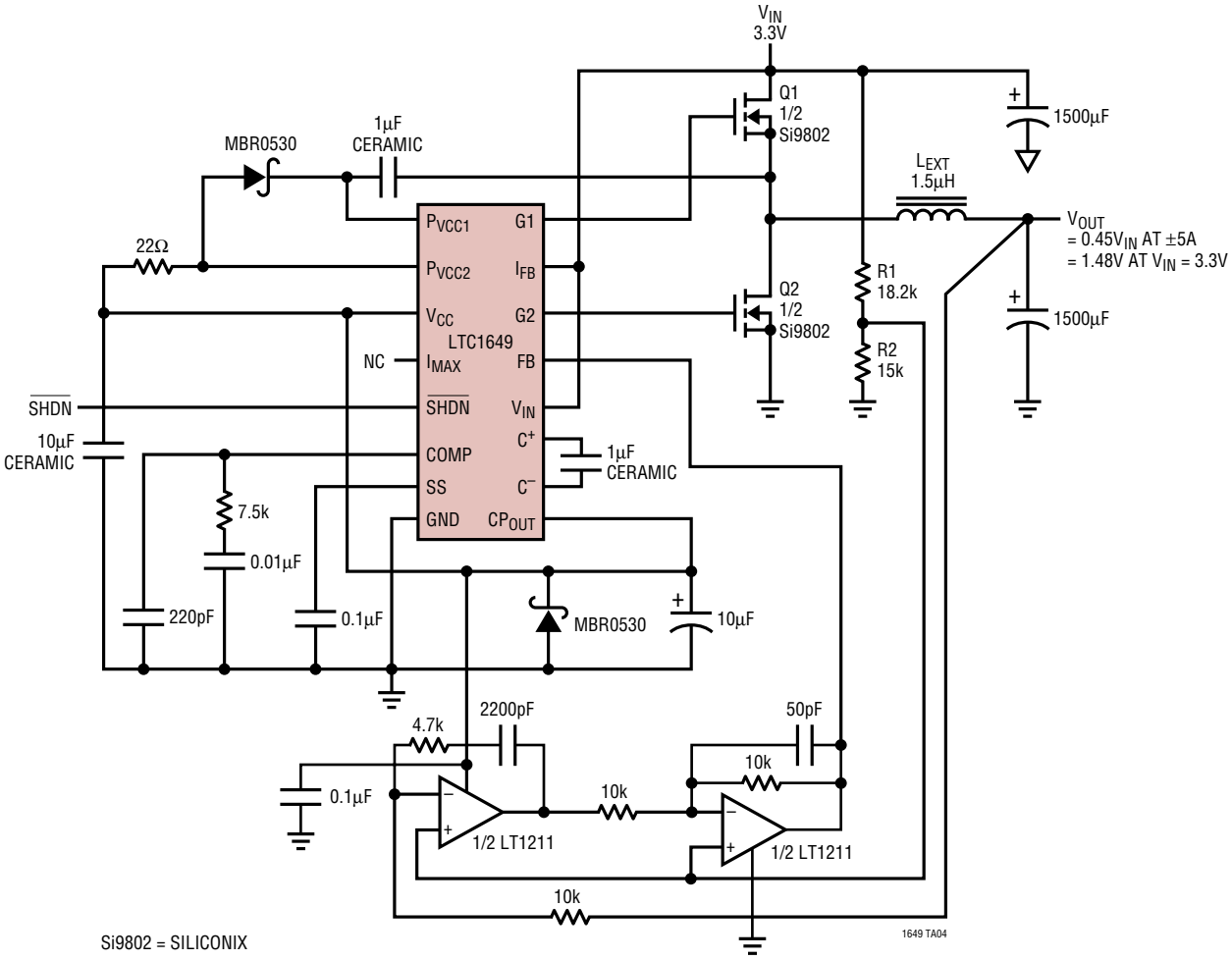


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

SSTL Logic Termination Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1430A	High Power Step-Down Switching Regulator Controller	5V to 1.xV @10A, Maximum Duty cycle > 90% Permits 3.3V to 2.xV Conversion
LTC1517-5	Micropower, Regulated 5V Charge Pump in a 5-Pin SOT-23 Package	Low Power 3.3V to 5V Step-Up Converter
LTC1702	2-Phase, Dual Output DC/DC Step-Down Controller	3.3V Input to As Low As 0.8V Conversion, Minimum C_{IN} and C_{OUT}
LTC1772	SOT-23 Step-Down DC/DC Controller	550kHz Operation for Small Circuit
LTC1773	3.3V Input DC/DC Synchronous Step-Down Controller	550kHz Operation, Up to 6A Output, 10-Lead MSOP
LTC1874	Dual Output DC/DC Step-Down Controller	550kHz Operation, Up to 4A Output, 16-Lead SSOP
LTC1876	Triple Ouput 2-Phase DC/DC Controller	Converts 3.3V_{IN} to Two Output Voltages Using 5V Logic N-Channel MOSFETS, Eliminates Need for Auxiliary 5V Supply, >90% Efficiency

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