



# THE DATASHEET OF LNBH26LPQR



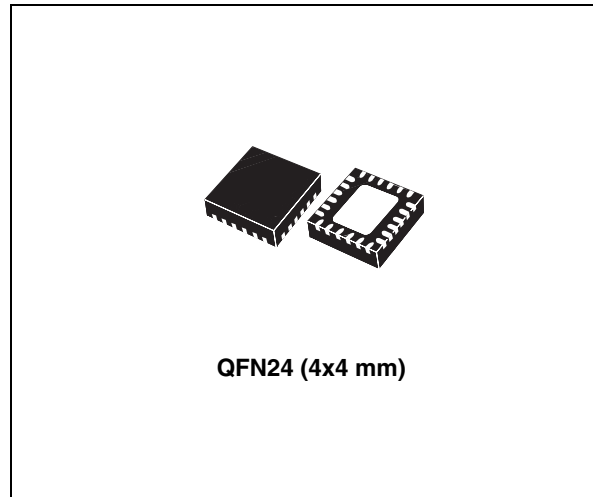
## Dual LNBS supply and control IC with step-up and I<sup>2</sup>C interface

### Features

- Complete interface between LNB and I<sup>2</sup>C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specification (8 programmable levels)
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- 22 kHz tone waveform integrity guaranteed also at no load condition
- Low-drop post regulator and high efficiency step-up PWM with integrated power N-MOS allowing low power losses
- Overload and overtemperature internal protection with I<sup>2</sup>C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

### Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers



### Description

Intended for analog and digital DUAL satellite receivers/Sat-TV, Sat-PC cards, the LNBH26L is a monolithic voltage regulator and interface IC, assembled in QFN24 (4x4) specifically designed to provide the 13 / 18 V power supply and the 22 kHz tone signalling to the LNB down-converter in the antenna dishes or to the multi-switch box. In this application field, it offers a complete solution for dual tuner satellite receivers with an extremely low component count and low power dissipation together with simple design and I<sup>2</sup>C standard interfacing.

**Table 1. Device summary**

Order code	Package	Packaging
LNBH26LPQR	QFN24 (4x4)	Tape and reel

# Contents

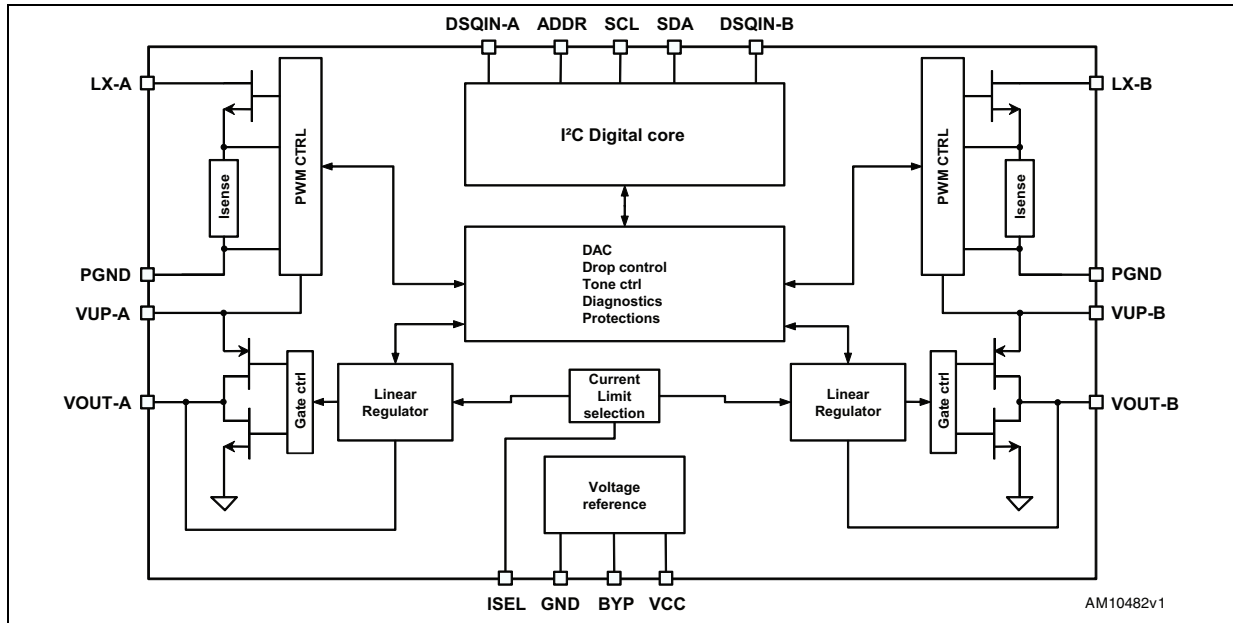
<b>1</b>	<b>Block diagram</b> .....	<b>3</b>
<b>2</b>	<b>Application information (valid for each section A/B)</b> .....	<b>4</b>
2.1	DiSEQC data encoding (DSQIN pin) .....	4
2.2	Data encoding by external 22 kHz tone TTL signal .....	4
2.3	Data encoding by external DiSEQC envelope control through the DSQIN pin .....	5
2.4	Output current limit selection .....	5
2.5	Output voltage selection .....	6
2.6	Diagnostic and protection functions .....	6
2.7	Surge protection and TVS diodes .....	6
2.8	Power-on I <sup>2</sup> C interface reset and undervoltage lockout .....	7
2.9	PNG: input voltage minimum detection .....	7
2.10	OLF: overcurrent and short-circuit protection and diagnostic .....	7
2.11	OTF: thermal protection and diagnostic .....	7
<b>3</b>	<b>Pin configuration</b> .....	<b>9</b>
<b>4</b>	<b>Maximum ratings</b> .....	<b>11</b>
<b>5</b>	<b>Typical application circuits</b> .....	<b>12</b>
<b>6</b>	<b>I<sup>2</sup>C bus interface</b> .....	<b>13</b>
6.1	Data validity .....	13
6.2	START and STOP condition .....	13
6.3	Byte format .....	13
6.4	Acknowledge .....	13
6.5	Transmission without acknowledge .....	13
<b>7</b>	<b>I<sup>2</sup>C interface protocol</b> .....	<b>15</b>
7.1	Write mode transmission .....	15
7.2	Read mode transmission .....	16
7.3	Data registers .....	17

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7.4	Status registers .....	19
<b>8</b>	<b>Electrical characteristics .....</b>	<b>20</b>
8.1	Output voltage selection .....	21
<b>9</b>	<b>Package mechanical data .....</b>	<b>23</b>
<b>10</b>	<b>Revision history .....</b>	<b>27</b>

# 1 Block diagram

Figure 1. Block diagram



## 2 Application information (valid for each section A/B)

This IC has a built-in DC-DC step-up converter that, from a single source (8 V to 16 V), generates the voltages ( $V_{UP}$ ) that let the integrated LDO post-regulator (generating the 13 V / 18 V LNB output voltages plus the 22 kHz DiSEqC tone) to work with a minimum dissipated power of 0.5 W typ. @ 500 mA load (the LDO drop voltage is internally kept at  $V_{UP} - V_{OUT} = 1$  V typ.). The IC is also provided with an undervoltage lockout circuit that disables the whole circuit when the supplied  $V_{CC}$  drops below a fixed threshold (4.7 V typically). The step-up converter soft-start function reduces the inrush current during startup. The SS time is internally fixed at 4 ms typ. to switch from 0 to 13 V and 6 ms typ. to switch from 0 to 18 V.

### 2.1 DiSEqC data encoding (DSQIN pin)

The internal 22 kHz tone generator is factory trimmed in accordance with the DiSEqC standards, and can be activated in 3 different ways:

- 1) by an external 22 kHz source DiSEqC data connected to the DSQIN logic pin (TTL compatible). In this case the I<sup>2</sup>C tone control bits must be set: EXTM=TEN=1.
- 2) by an external DiSEqC data envelope source connected to the DSQIN logic pin. In this case the I<sup>2</sup>C tone control bits must be set: EXTM=0 and TEN=1.
- 3) through the TEN I<sup>2</sup>C bit if the 22 kHz presence is requested in continuous mode. In this case the DSQIN TTL pin must be pulled high and the EXTM bit set to "0".

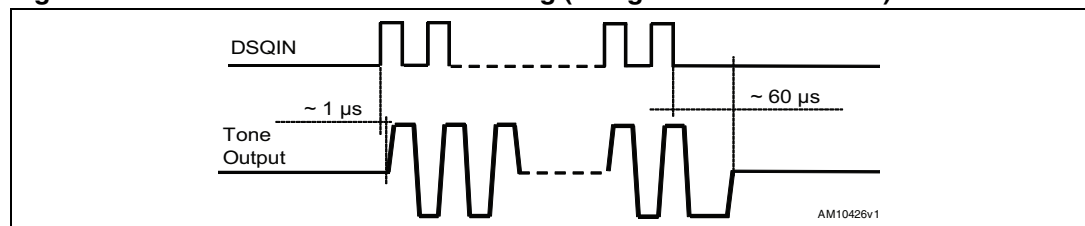
### 2.2 Data encoding by external 22 kHz tone TTL signal

In order to improve design flexibility, an external tone signal can be input to the DSQIN pin by setting the EXTM bit to "1".

The DSQIN is a logic input pin which activates the 22 kHz tone to the  $V_{OUT}$  pin, by using the LNBH26L integrated tone generator.

The output tone waveforms are internally controlled by the LNBH26L tone generator in terms of rise/fall time and tone amplitude, while, the external 22 kHz signal on the DSQIN pin is used to define the frequency and the duty cycle of the output tone. A TTL compatible 22 kHz signal is required for the proper control of the DSQIN pin function. Before sending the TTL signal on the DSQIN pin, the EXTM and TEN bits must be previously set to "1". As soon as the DSQIN internal circuit detects the 22 kHz TTL external signal code, the LNBH26L activates the 22 kHz tone on the  $V_{OUT}$  output with about 1  $\mu$ s delay from TTL signal activation, and it stops with about 60  $\mu$ s delay after the 22 kHz TTL signal on DSQIN has expired. Refer to [Figure 2](#).

**Figure 2. Tone enable and disable timing (using external waveform)**

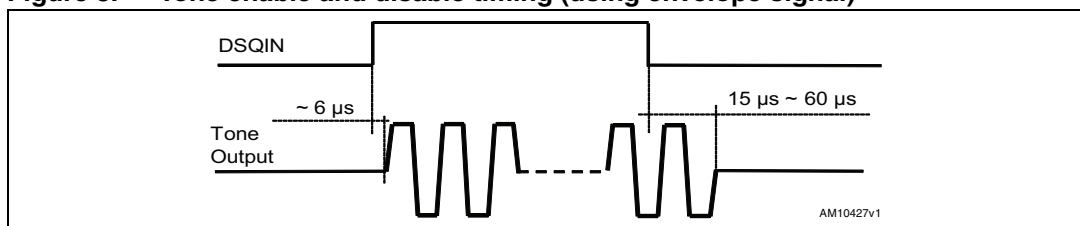


## 2.3 Data encoding by external DiSEqC envelope control through the DSQIN pin

If an external DiSEqC envelope source is available, it is possible to use the internal 22 kHz generator activated during the tone transmission by connecting the DiSEqC envelope source to the DSQIN pin. In this case the I<sup>2</sup>C tone control bits must be set: EXT<sub>M</sub>=0 and TEN=1. In this way, the internal 22 kHz signal is superimposed to the V<sub>OUT</sub> DC voltage to generate the LNB output 22 kHz tone. During the period in which the DSQIN is kept high the internal control circuit activates the 22 kHz tone output.

The 22 kHz tone on the V<sub>OUT</sub> pin is activated with about 6 μs delay from the DSQIN TTL signal rising edge, and it stops with a delay time in the range from 15 μs to 60 μs after the 22 kHz TTL signal on DSQIN has expired (refer to [Figure 3](#)).

**Figure 3. Tone enable and disable timing (using envelope signal)**



## 2.4 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit by the equation:

**Equation 1**

$$I_{\text{MAX}}(\text{typ.}) = \frac{16578}{\text{RSEL}^{1.206}}$$

with ISET=0,

where RSEL is the resistor connected between ISEL and GND expressed in kΩ and I<sub>MAX</sub>(typ.) is the typical current limit threshold expressed in mA. I<sub>MAX</sub> can be set up to 750 mA for each channel. However, it is recommended to not exceed for a long period a total amount of current of 1 A from both sections (I<sub>OUT\_A</sub> + I<sub>OUT\_B</sub> < 1 A) in order to avoid the overtemperature protection from triggering and to thoroughly validate the PCB layout thermal management in real application environment conditions.

## 2.5 Output voltage selection

Each linear regulator channel output voltage level can be easily programmed in order to accomplish application specific requirements, using 4 + 4 bits of an internal DATA1 register (see [Section 7.3: Data registers](#) and [Table 13: Output voltage selection table \(Data1 register, write mode\)](#) for exact programmable values). Register writing is accessible via the I<sup>2</sup>C bus.

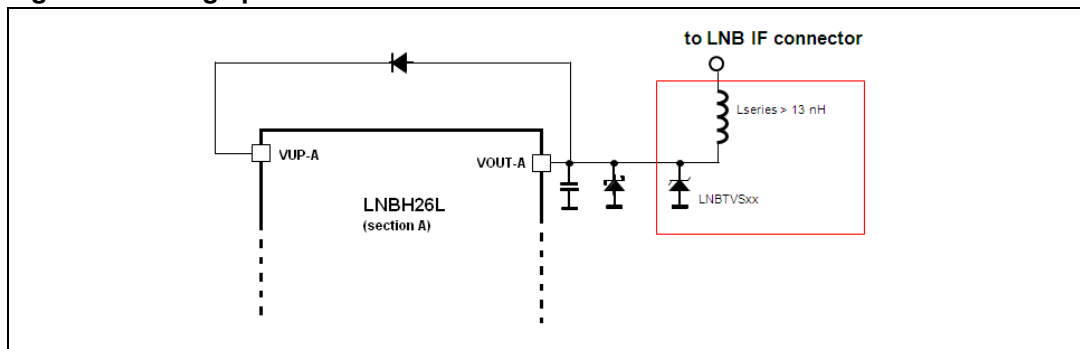
## 2.6 Diagnostic and protection functions

The LNBH26L has 4 diagnostic internal functions provided via the I<sup>2</sup>C bus, by reading 4 bits on the STATUS1 register (in read mode). All the diagnostic bits are, in normal operation (that is, no failure detected), set to LOW. One diagnostic bit is dedicated to the overtemperature (OTF), and two bits (one per section) are dedicated to overcurrent (OLF-A, OLF-B). One bit is dedicated to the input voltage power not good function (PNG). Once the OTF bit (or OLF-A, OLF-B or PNG) has been activated (set to “1”), it is latched to “1” until the relevant cause is removed and a new register reading operation is done.

## 2.7 Surge protection and TVS diodes

Each LNBH26L device section is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. Transient voltage suppressor (TVS) devices are usually placed, as shown in the following schematic, to protect each section of STB output circuits where the LNBH26L and other devices are electrically connected to the antenna cable.

**Figure 4. Surge protection circuit**



For this purpose the use of LNBTVSxx surge protection diodes specifically designed by ST is recommended. The selection of the LNBTVS diode should be made based on the maximum peak power dissipation that the diode is capable of supporting (see the LNBTVS datasheet for further details).

## 2.8 Power-on I<sup>2</sup>C interface reset and undervoltage lockout

The I<sup>2</sup>C interface built into the LNBH26L is automatically reset at power-on. As long as the V<sub>CC</sub> stays below the undervoltage lockout (UVLO) threshold (4.7 V typ.), the interface does not respond to any I<sup>2</sup>C command and all DATA register bits are initialized to zeroes, therefore keeping the power blocks disabled. Once the V<sub>CC</sub> rises above 4.8 V typ., the I<sup>2</sup>C interface becomes operative and the DATA registers can be configured by the main microprocessor.

## 2.9 PNG: input voltage minimum detection

When input voltage (VCC pin) is lower than LPD (low power diagnostic) minimum thresholds, the PNG I<sup>2</sup>C bit is set to “1”. Refer to the electrical characteristics table for threshold details.

## 2.10 OLF: overcurrent and short-circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short-circuit condition, each section of the device is provided with a dynamic short-circuit protection. It is possible to set the short-circuit current protection either statically (simple current clamp) or dynamically through the corresponding PCL bit of the I<sup>2</sup>C DATA3 register. When the PCL (pulsed current limiting) bit is set to LOW, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for T<sub>ON</sub> time 90 ms and after that, the output is set in shutdown for a T<sub>OFF</sub> time of typically 900 ms. Simultaneously, the corresponding diagnostic OLF I<sup>2</sup>C bit of the STATUS1 register is set to “1”. After this time has elapsed, the involved output is resumed for a time T<sub>ON</sub>. At the end of T<sub>ON</sub>, if the overload is still detected, the protection circuit cycles again through T<sub>OFF</sub> and T<sub>ON</sub>. At the end of a full T<sub>ON</sub> in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to low after register reading is done. Typical T<sub>ON</sub> + T<sub>OFF</sub> time is 990 ms and is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short-circuit condition, while still ensuring excellent power-on startup in most conditions. However, there may be some cases in which a highly capacitive load on the output can cause a difficult startup when the dynamic protection is chosen. This can be solved by initiating any power startup in static mode (PCL=1) and, then, switching to the dynamic mode (PCL=0) after a chosen amount of time depending on the output capacitance. Also in static mode, the diagnostic OLF bit goes to “1” (and the FLT pin is set to low) when the current clamp limit is reached and returns low when the overload condition is cleared and register reading is done.

After the overload condition is removed, normal operation can be resumed in two ways, according to the OLR I<sup>2</sup>C bit on the DATA4 register.

If OLR=1, all VSEL bits corresponding to the involved section are reset to “0” and the LNB section output (V<sub>OUT</sub> pin) is disabled. To re-enable the output stage, the VSEL bits must be set again by the microprocessor and the OLF bit is reset to “0” after a register reading operation.

If OLR=0, the involved output is automatically re-enabled as soon as the overload condition is removed, and OLF bit is reset to “0” after a register reading operation.

## 2.11 OTF: thermal protection and diagnostic

The LNBH26L is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and both linear regulators are shut off, the diagnostic OTF bit in the STATUS1 register is set to “1”. After the overtemperature condition is removed, normal operation can be resumed in two ways, according to the THERM I<sup>2</sup>C bit on the DATA4 register.

If THERM=1, all VSEL bits are reset to “0” and both LNB outputs (V<sub>OUT</sub> pins) are disabled. To re-enable the output stages, the VSEL bits must be set again by the microprocessor, while the OTF bit is reset to “0” after a register reading operation.

If THERM=0, outputs are automatically re-enabled as soon as the overtemperature condition is removed, while the OTF bit is reset to “0” after a register reading operation.

### 3 Pin configuration

Figure 5. Pin connections (top view)

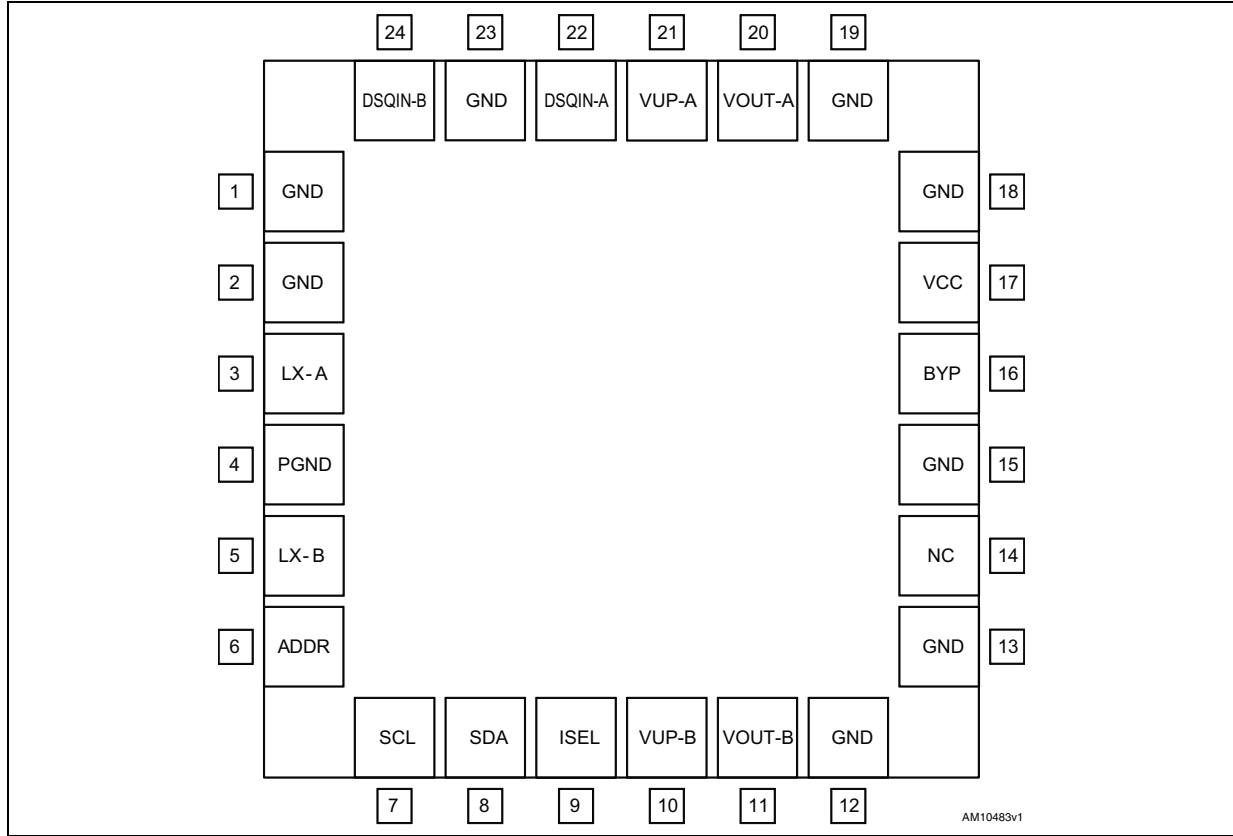


Table 2. Pin description

Pin n°	Symbol	Name	Pin function
3	LX-A	N-Mos drain	Channel A, integrated N-channel Power MOSFET drain.
4	P-GND	Power ground	DC-DC converter power ground. To be connected directly to the Epad.
5	LX-B	N-Mos drain	Channel B, integrated N-channel Power MOSFET drain.
6	ADDR	Address setting	Two I <sup>2</sup> C bus addresses available by setting the Address pin level voltage. See the Address pin characteristics table.
7	SCL	Serial clock	Clock from I <sup>2</sup> C bus.
8	SDA	Serial data	Bi-directional data from/to I <sup>2</sup> C bus.
9	ISEL	Current selection for both channel A and B	The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold. Refer to “output current limit selection” <a href="#">Section 2</a> . The RSEL resistor defines the same current limit both for channels A and B.
1, 2, 12, 13, 15, 18, 19, 23	GND	Analog ground	Analog circuits ground. To be connected directly to the Epad.

Table 2. Pin description (continued)

Pin n°	Symbol	Name	Pin function
10	V <sub>UP-B</sub>	Channel B step-up voltage	Input of channel B linear post-regulator. The voltage on this pin is monitored by the internal channel B step-up controller to keep a minimum dropout across the linear pass transistor.
11	V <sub>OUT-B</sub>	Channel B, LNB output port	Output of channel B integrated very low-drop linear regulator. Refer to <a href="#">Table 13</a> for voltage selection and description.
14	N.C.	Not internally connected	Not internally connected pin. Set floating if not used.
16	BYP	Bypass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to an external current or voltage sources may cause permanent damage to the device.
17	V <sub>CC</sub>	Supply input	8 to 16 V IC DC-DC power supply.
20	V <sub>OUT-A</sub>	Channel A, LNB output port	Output of channel A integrated very low-drop linear regulator. Refer to <a href="#">Table 13</a> for voltage selection and description.
21	V <sub>UP-A</sub>	Channel A step-up voltage	Input of channel A linear post-regulator. The voltage on this pin is monitored by the internal channel A step-up controller to keep a minimum dropout across the linear pass transistor.
22	DSQIN-A	DSQIN for DiSEqC envelope input or external 22 KHz TTL input	It is intended for channel A 22 kHz tone control. It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on the EXTM-A I <sup>2</sup> C bit setting as follows: If EXTM-A=0, TEN-A=1: it accepts the DiSEqC envelope code from the main microcontroller. The LNBH26L uses this code to modulate the internally generated 22 kHz carrier. If EXTM-A=TEN-A=1: it accepts external 22 kHz logic signals which activate the 22 kHz tone output (refer to <a href="#">Section 2.2</a> ). Pull up high if the tone output is activated only by the TEN-A I <sup>2</sup> C bit.
24	DSQIN-B	DSQIN for DiSEqC envelope Input or external 22 KHz TTL input	It is intended for channel B 22 kHz tone control. It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on the EXTM-B I <sup>2</sup> C bit setting as follows: If EXTM-B=0, TEN-B=1: it accepts the DiSEqC envelope code from the main microcontroller. The LNBH26L uses this code to modulate the internally generated 22 kHz carrier. If EXTM-A=TEN-A=1: it accepts external 22 kHz logic signals which activate the 22 kHz tone output (refer to <a href="#">Section 2.2</a> ). Pull up high if the tone output is activated only by TEN-B I <sup>2</sup> C bit.
Epad	Epad	Exposed pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat.

## 4 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC power supply input voltage pins	-0.3 to 20	V
$V_{UP}$	DC input voltage	-0.3 to 40	V
$I_{OUT}$	Output current	Internally limited	mA
$V_{OUT}$	DC output pin voltage	-0.3 to 40	V
$V_I$	Logic input pin voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
LX	LX input voltage	-0.3 to 30	V
$V_{BYP}$	Internal reference pin voltage	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 3.5	V
$T_{STG}$	Storage temperature range	-50 to 150	°C
$T_J$	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with human body model (HBM) all pins, unless power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case	2	°C/W
$R_{thJA}$	Thermal resistance junction-ambient with device soldered on 2s2p 4-layer PCB provided with thermal vias below the exposed pad.	40	°C/W

*Note:* Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal.

## 5 Typical application circuits

Figure 6. DiSEqC 1.x application circuit

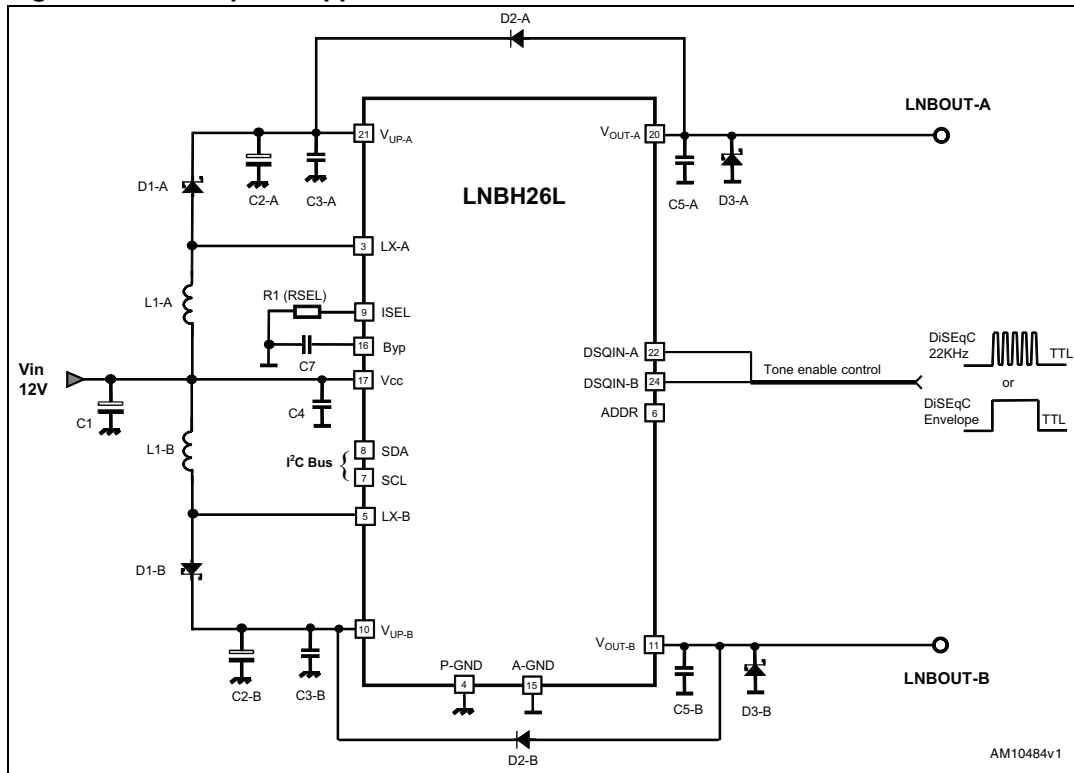


Table 5. DiSEqC 1.x bill of material (valid for A and B channels except for C1, C4, C7 and R1)

Component	Notes
R1 (RSEL)	SMD resistor. Refer to <a href="#">Table 12</a> and the ISEL pin description in <a href="#">Table 2</a> .
C1, C2	> 25 V electrolytic capacitor, 100 $\mu$ F is suitable.
C3	From 470 nF to 2.2 $\mu$ F ceramic capacitor. Higher values allow lower DC-DC noise.
C5	From 100 nF to 220 nF ceramic capacitor. Higher values allow lower DC-DC noise.
C4, C7	220 nF ceramic capacitors.
D1	STPS130A or similar Schottky diode.
D3	BAT54, BAT43, 1N5818, or any low power schottky diode with $I_F(AV) > 0.2$ A, $V_{RRM} > 25$ V, $V_F < 0.5$ V. To be placed as close as possible to the $V_{OUT}$ pin.
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier.
L1	10 $\mu$ H inductor with $I_{sat} > I_{peak}$ where $I_{peak}$ is the boost converter peak current.

## 6 I<sup>2</sup>C bus interface

Data transmission from the main microprocessor to the LNBH26L, and vice versa, takes place through the 2-wire I<sup>2</sup>C bus interface, consisting of the 2-line SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

### 6.1 Data validity

As shown in [Figure 7](#), the data on the SDA line must be stable during the high semi-period of the clock. The high and low state of the data line can only change when the clock signal on the SCL line is LOW.

### 6.2 START and STOP condition

As shown in [Figure 8](#), a START condition is a high to low transition of the SDA line while SCL is HIGH. The STOP condition is a low to high transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

### 6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSb is transferred first.

### 6.4 Acknowledge

The master (microprocessor) puts a resistive high level on the SDA line during the acknowledge clock pulse (see [Figure 9](#)). The peripheral (LNBH26L) which acknowledges must pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during this clock pulse. The peripheral which has been addressed must generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the high level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH26L won't generate acknowledge if the  $V_{CC}$  supply is below the undervoltage lockout threshold (4.7 V typ.).

### 6.5 Transmission without acknowledge

If the detection of LNBH26L acknowledge is not necessary, the microprocessor can use a simpler transmission; it simply waits one clock without checking the slave acknowledging, and sends the new data. This approach is of course less protected from misworking and decreases noise immunity.

Figure 7. Data validity on the I<sup>2</sup>C bus

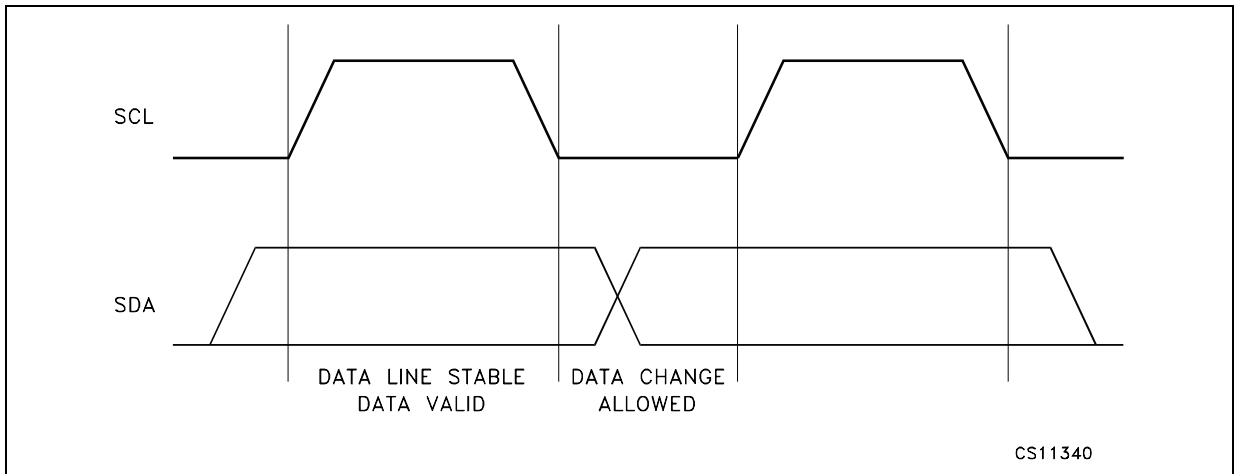


Figure 8. Timing diagram of I<sup>2</sup>C bus

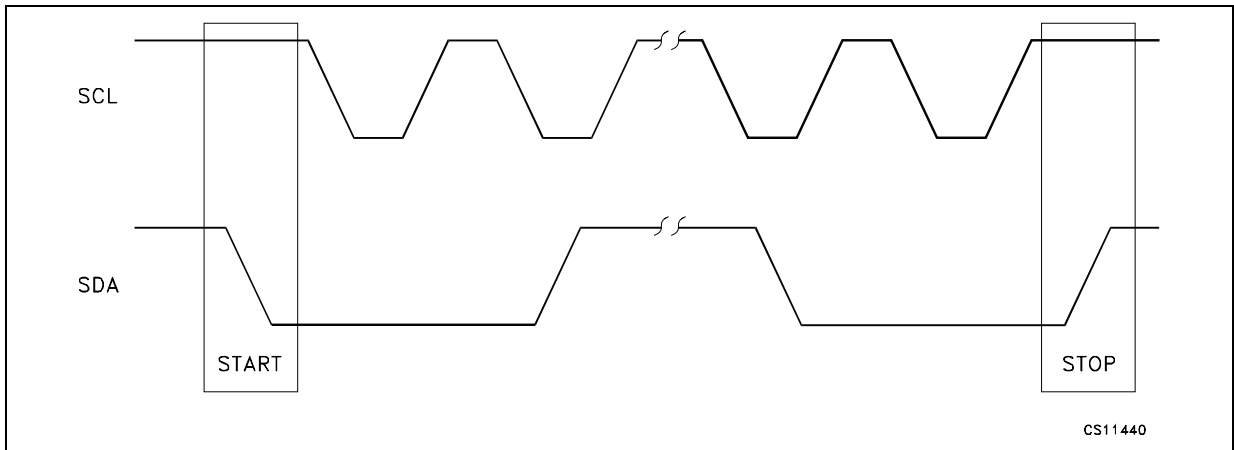
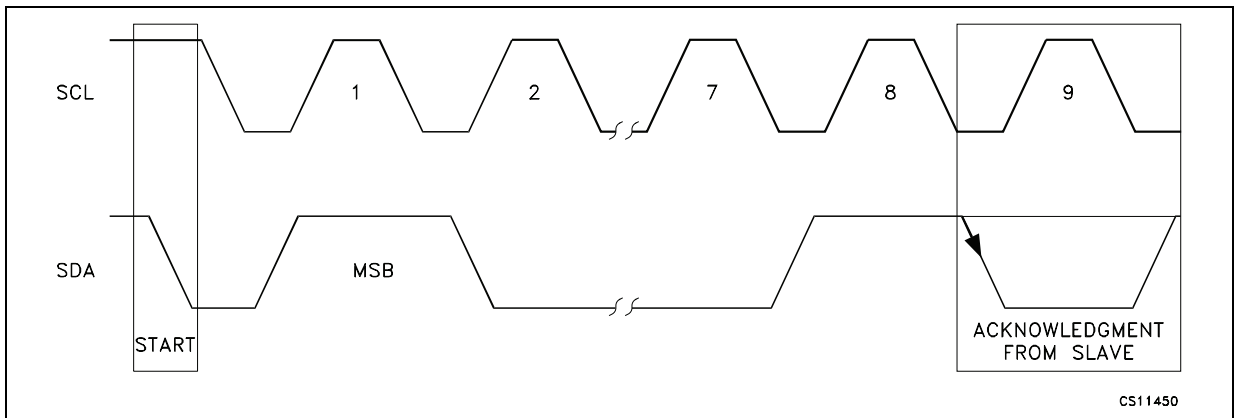


Figure 9. Acknowledge on the I<sup>2</sup>C bus







### 7.3 Data registers

The DATA 1..4 registers can be addressed both in write and read mode. In read mode they return the last writing byte status received in the previous write transmission.

The following tables provide the register address values of Data 1..4 and a function description of each bit.

**Table 6. DATA 1 (read/write register. Register address = 0X2)**

Bit	Name	CH	Value	Description
Bit 0 (LSb)	VSEL1-A	A	0/1	Channel A output voltage selection bits. (Refer to <a href="#">Table 13</a> )
Bit 1	VSEL2-A		0/1	
Bit 2	VSEL3-A		0/1	
Bit 3	VSEL4-A		0/1	
Bit 4	VSEL1-B	B	0/1	Channel B output voltage selection bits. (Refer to <a href="#">Table 13</a> )
Bit 5	VSEL2-B		0/1	
Bit 6	VSEL3-B		0/1	
Bit 7 (MSb)	VSEL4-B		0/1	

N/A = Reserved bit.

All bits reset to "0" at power-on.

**Table 7. DATA 2 (read/write register. Register address = 0X3)**

Bit	Name	CH	Value	Description	
Bit 0 (LSb)	TEN-A	A	1	22 kHz tone enabled. Tone output controlled by the DSQIN pin	
			0	22 kHz tone output disabled	
Bit 1	N/A		0	Reserved. Keep to "0".	
Bit 2	EXTM-A		1	DSQIN input pin is set to receive external 22 kHz TTL signal source	
			0	DSQIN input pin is set to receive external DiSEqC envelope TTL signal	
Bit 3	N/A		0	Reserved. Keep to "0".	
Bit 4	TEN-B		B	1	22 kHz tone enabled. Tone output controlled by the DSQIN pin
				0	22 kHz tone output disabled
Bit 5	N/A	0		Reserved. Keep to "0".	
Bit 6	EXTM-B	1		DSQIN input pin is set to receive external 22 kHz TTL signal source	
		0		DSQIN input pin is set to receive external DiSEqC envelope TTL signal	
Bit 7 (MSb)	N/A	0		Reserved. Keep to "0".	

N/A = Reserved bit.

All bits reset to "0" at power-on.

**Table 8. DATA 3 (read/write register. Register address = 0X4)**

Bit	Name	CH	Value	Description
Bit 0 (LSb)	N/A	A	0	Reserved. Keep to "0"
Bit 1	N/A		0	Reserved. Keep to "0"
Bit 2	PCL-A		1	Pulsed (Dynamic) LNB output current limiting is deactivated
			0	Pulsed (Dynamic) LNB output current limiting is activated
Bit 3	N/A		0	Reserved. Keep to "0"
Bit 4	N/A	B	0	Reserved. Keep to "0"
Bit 5	N/A		0	Reserved. Keep to "0"
Bit 6	PCL-B		1	Pulsed (Dynamic) LNB output current limiting is deactivated
			0	Pulsed (Dynamic) LNB output current limiting is activated
Bit 7 (MSb)	N/A		0	Reserved. Keep to "0"

N/A = Reserved bit.

All bits reset to "0" at power-on.

**Table 9. DATA 4 (read/write register. Register address = 0X5)**

Bit	Name	CH	Value	Description
Bit 0 (LSb)	N/A	-	0	Reserved. Keep to "0".
Bit 1	N/A	-	0	Reserved. Keep to "0".
Bit 2	N/A	-	0	Reserved. Keep to "0".
Bit 3	OLR	A/B	1	In the case of overload protection activation (OLF=1), all VSEL 1..4 bits are reset to "0" and LNB output (V <sub>OUT</sub> pin) is disabled. The VSEL bits must be set again by the master after the overcurrent condition is removed (OLF=0).
			0	In the case of overload protection activation (OLF=1) the LNB output (V <sub>OUT</sub> pin) is automatically enabled as soon as the overload condition is removed (OLF=0) with the previous VSEL bits setting.
Bit 4	N/A	-	0	Reserved. Keep to "0".
Bit 5	N/A	-	0	Reserved. Keep to "0".
Bit 6	THERM	A/B	1	If thermal protection is activated (OTF=1), all VSEL 1..4 bits are reset to "0" and LNB output (V <sub>OUT</sub> pin) is disabled. The VSEL bits must be set again by the master after the overtemperature condition is removed (OTF=0).
			0	In the case of thermal protection activation (OTF=1) the LNB output (V <sub>OUT</sub> pin) is automatically enabled as soon as the overtemperature condition is removed (OTF=0) with the previous VSEL bits setting.
Bit 7 (MSb)	COMP	-	0	Reserved. Keep to "0"

## 7.4 Status registers

The STATUS 1, 2 registers can be addressed only in read mode and provide the diagnostic functions described in the following tables.

**Table 10. STATUS 1 (read register. Register address = 0X0)**

Bit	Name	CH	Value	Description
Bit 0 (LSb)	OLF-A	A	1	V <sub>OUT</sub> pin overload protection has been triggered (I <sub>OUT</sub> > I <sub>MAX</sub> ). Refer to <a href="#">Table 8</a> for the overload operation and PCL settings.
			0	No overload protection has been triggered to the V <sub>OUT</sub> pin (I <sub>OUT</sub> < I <sub>MAX</sub> ).
Bit 1	OLF-B	B	1	V <sub>OUT</sub> pin overload protection has been triggered (I <sub>OUT</sub> > I <sub>MAX</sub> ). Refer to <a href="#">Table 8</a> for the overload operation and PCL settings.
			0	No overload protection has been triggered to V <sub>OUT</sub> pin (I <sub>OUT</sub> < I <sub>MAX</sub> ).
Bit 2	N/A	-	-	Reserved
Bit 3	N/A	-	-	Reserved
Bit 4	N/A	-	-	Reserved
Bit 5	N/A	-	-	Reserved
Bit 6	OTF	A/B	1	Junction overtemperature is detected, T <sub>J</sub> > 150 °C (typ.). See also THERM bit setting in <a href="#">Table 9</a> .
			0	Junction overtemperature not detected, T <sub>J</sub> < 135 °C (typ.). T <sub>J</sub> is below thermal protection threshold.
Bit 7 (MSb)	PNG	A/B	1	Input voltage (V <sub>CC</sub> pin) lower than LPD minimum thresholds. Refer to <a href="#">Table 12</a> .
			0	Input voltage (V <sub>CC</sub> pin) higher than LPD thresholds. Refer to <a href="#">Table 12</a> .

N/A = Reserved bit.

All bits reset to “0” at power-on.

**Table 11. STATUS 2 (read register. Register address = 0X1)**

Bit	Name	CH	Value	Description
Bit 0 (LSb)	N/A	-	-	Reserved
Bit 1	N/A	-	-	Reserved
Bit 2	N/A	-	-	Reserved
Bit 3	N/A	-	-	Reserved
Bit 4	N/A	-	-	Reserved
Bit 5	N/A	-	-	Reserved
Bit 6	N/A	-	-	Reserved
Bit 7 (MSb)	N/A	-	-	Reserved

N/A = Reserved bit.

All bits reset to “0” at power-on.

## 8 Electrical characteristics

Refer to [Section 5](#),  $T_J$  from 0 to 85 °C, all DATA 1..4 register bits set to 0 unless VSEL1 = 1, RSEL = 11 k $\Omega$ , DSQIN = LOW,  $V_{IN}$  = 12 V,  $I_{OUT}$  = 50 mA, unless otherwise stated. Typical values are referred to  $T_J$  = 25 °C.  $V_{OUT}$  =  $V_{OUT}$  pin voltage. See software description section for I<sup>2</sup>C access to the system register ([Section 6](#) and [Section 7](#)).

**Table 12. Electrical characteristics of section A/B**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Supply voltage <sup>(1)</sup>		8	12	16	V
$I_{IN}$	Supply current	Both sections A and B enabled, $I_{OUT}$ = 0 mA		12		mA
		22 kHz tone enabled (TEN-A/B = 1, DSQIN-A/B = High), $I_{OUT}$ = 0 mA		19		
		Both sections A and B set in standby: VSEL1=VSEL2=VSEL3=VSEL4=0		2		
$V_{OUT}$	Output voltage total accuracy	Valid at any $V_{OUT}$ selected level	-3.5		+3.5	%
$V_{OUT}$	Line regulation	$V_{IN}$ = 8 to 16 V			40	mV
$V_{OUT}$	Load regulation	$I_{OUT}$ from 50 to 500 mA		75	100	
$I_{MAX}$	Output current limiting thresholds	RSEL = 15 k $\Omega$	500		750	mA
		RSEL = 20 k $\Omega$	350		550	
$I_{SC}$	Output short-circuit current	RSEL = 15 k $\Omega$		350		mA
SS	Soft-start time	$V_{OUT}$ from 0 to 13 V		4		ms
SS	Soft-start time	$V_{OUT}$ from 0 to 18 V		6		ms
T13-18	Soft transition rise time	$V_{OUT}$ from 13 to 18 V		1.5		ms
T18-13	Soft transition fall time	$V_{OUT}$ from 18 to 13 V		1.5		ms
$T_{OFF}$	Dynamic overload protection OFF time	PCL = 0, output shorted		900		ms
$T_{ON}$	Dynamic overload protection ON time	PCL = 0, output shorted		$T_{OFF}/10$		
$A_{TONE}$	Tone amplitude	DSQIN=High, EXTM=0, TEN=1 $I_{OUT}$ from 0 to 500 mA $C_{BUS}$ from 0 to 750 nF	0.55	0.675	0.8	$V_{PP}$
$F_{TONE}$	Tone frequency	DSQIN=High, EXTM=0, TEN=1	20	22	24	kHz
$D_{TONE}$	Tone duty cycle		43	50	57	%
tr, tf	Tone rise or fall time <sup>(2)</sup>		5	8	15	$\mu$ s
Eff <sub>DC/DC</sub>	DC-DC converter efficiency	$I_{OUT}$ = 500 mA		93		%
$F_{SW}$	DC-DC converter switching frequency			440		kHz
UVLO	Undervoltage lockout thresholds	UVLO threshold rising		4.8		V
		UVLO threshold falling		4.7		

Table 12. Electrical characteristics of section A/B (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LP}$	Low power diagnostic (LPD) thresholds	$V_{LP}$ threshold rising		7.2		V
		$V_{LP}$ threshold falling		6.7		
$V_{IL}$	DSQIN, pin logic low				0.8	V
$V_{IH}$	DSQIN, pin logic high		2			V
$I_{IH}$	DSQIN, pin input current	$V_{IH} = 5\text{ V}$		15		$\mu\text{A}$
$I_{OBK}$	Output backward current	All VSELx = 0, $V_{OBK} = 30\text{ V}$		-3	-6	mA
$I_{SINK}$	Output low-side sink current	$V_{OUT}$ forced at $V_{OUT\_nom} + 0.1\text{ V}$		70		mA
$I_{SINK\_TIME-OUT}$	Low-side sink current time-out	$V_{OUT}$ forced at $V_{OUT\_nom} + 0.1\text{ V}$		10		ms
$I_{REV}$	Max. reverse current	$V_{OUT}$ forced at $V_{OUT\_nom} + 0.1\text{ V}$ , after $I_{SINK\_TIME-OUT}$ is elapsed.		2		mA
$T_{SHDN}$	Thermal shutdown threshold			150		$^{\circ}\text{C}$
$\Delta T_{SHDN}$	Thermal shutdown hysteresis			15		$^{\circ}\text{C}$

1. In applications where  $(V_{CC} - V_{OUT}) > 1.3\text{ V}$ , the increased power dissipation inside the integrated LDO must be taken into account in the application thermal management design.
2. Guaranteed by design.

## 8.1 Output voltage selection

Each LNBH26L channel is provided with 8 output voltage levels (4 levels for 13 V range when VSEL4-A/B=0 and 4 levels for 18 V range when VSEL4-A/B=1) which can be selected through the register Data1. The following table shows the output voltage values corresponding to VSELx bit combinations both for channel A and B. If all VSELx are at "0" the device is set in standby mode and the  $V_{OUT-A/B}$  are disabled.

**Table 13. Output voltage selection table (Data1 register, write mode) <sup>(1)</sup>**

VSEL4-A/B	VSEL3-A/B	VSEL2-A/B	VSEL1-A/B	V <sub>OUT</sub> min.	V <sub>OUT</sub> -A/B pin voltage	V <sub>OUT</sub> max.	Function
0	0	0	0		0		V <sub>OUT</sub> -A/B disabled. LNBH26L set in standby mode
0	0	0	1	12.545	13.000	13.455	
0	0	1	0	12.867	13.333	13.800	
0	0	1	1	13.188	13.667	14.145	
0	1	0	0	13.51	14.000	14.490	
1	0	0	0	17.515	18.150	18.785	
1	0	0	1	17.836	18.483	19.130	
1	0	1	0	18.158	18.817	19.475	
1	0	1	1	18.48	19.150	19.820	

1. T<sub>J</sub> from 0 to 85 °C, V<sub>I</sub> = 12 V.

T<sub>J</sub> from 0 to 85 °C, V<sub>I</sub> = 12 V.

**Table 14. I<sup>2</sup>C electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Low level input voltage	SDA, SCL			0.8	V
V <sub>IH</sub>	High level input voltage	SDA, SCL	2			V
I <sub>IN</sub>	Input current	SDA, SCL, V <sub>IN</sub> = 0.4 to 4.5 V	-10		10	µA
V <sub>OL</sub>	Low level output voltage <sup>(1)</sup>	SDA (open drain), I <sub>OL</sub> = 6 mA			0.6	V
F <sub>MAX</sub>	Maximum clock frequency	SCL	400			kHz

1. Guaranteed by design.

T<sub>J</sub> from 0 to 85 °C, V<sub>I</sub> = 12 V.

**Table 15. Address pin characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>ADDR-1</sub>	“0001000(R/W)” Address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
V <sub>ADDR-2</sub>	“0001001(R/W)” Address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

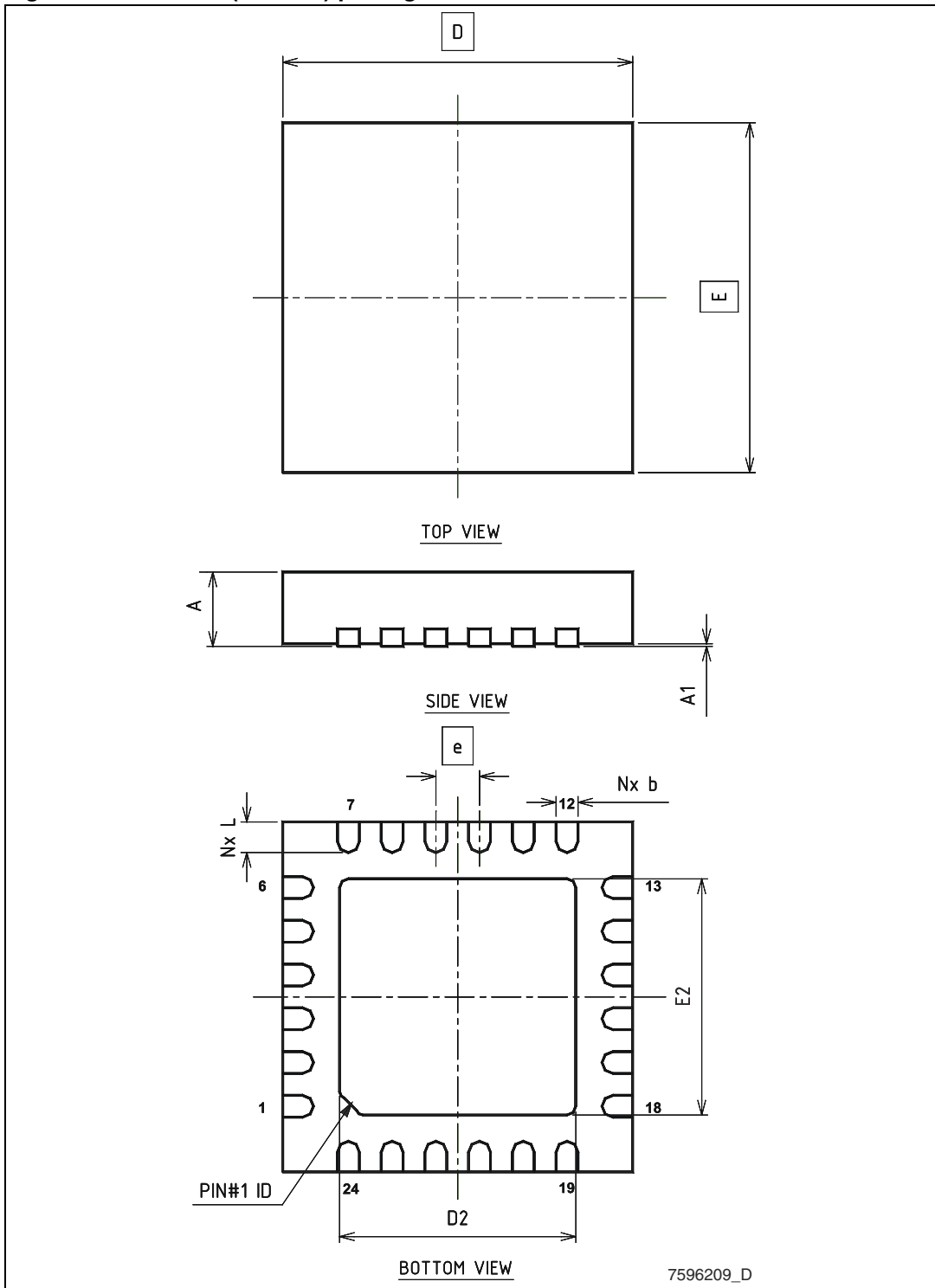
## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 16. QFN24L (4x4 mm) mechanical data**

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
e	0.45	0.50	0.55
L	0.25	0.35	0.45

Figure 12. QFN24L (4x4 mm) package dimensions



**Tape & reel QFNxx/DFNxx (4x4) mechanical data**

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

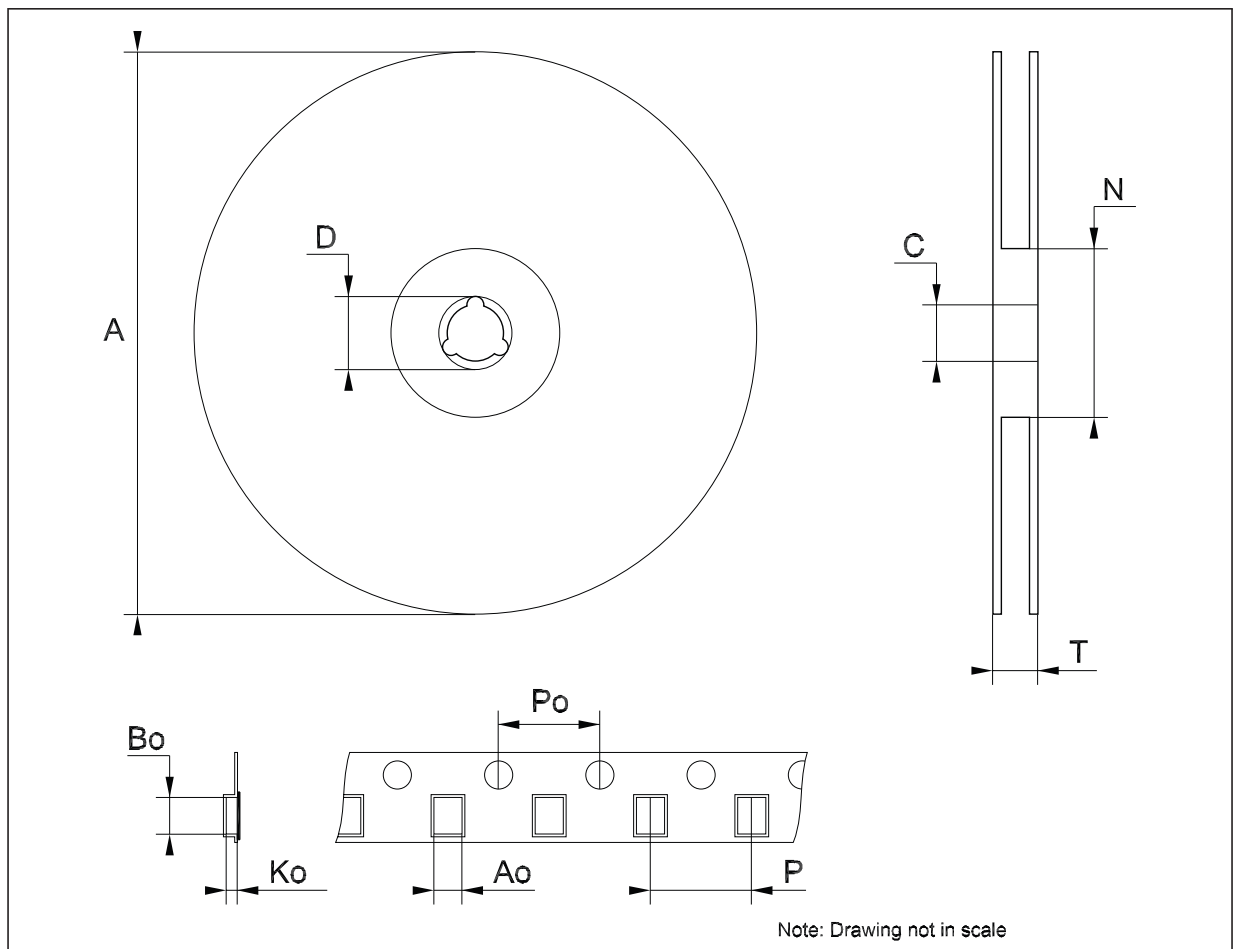
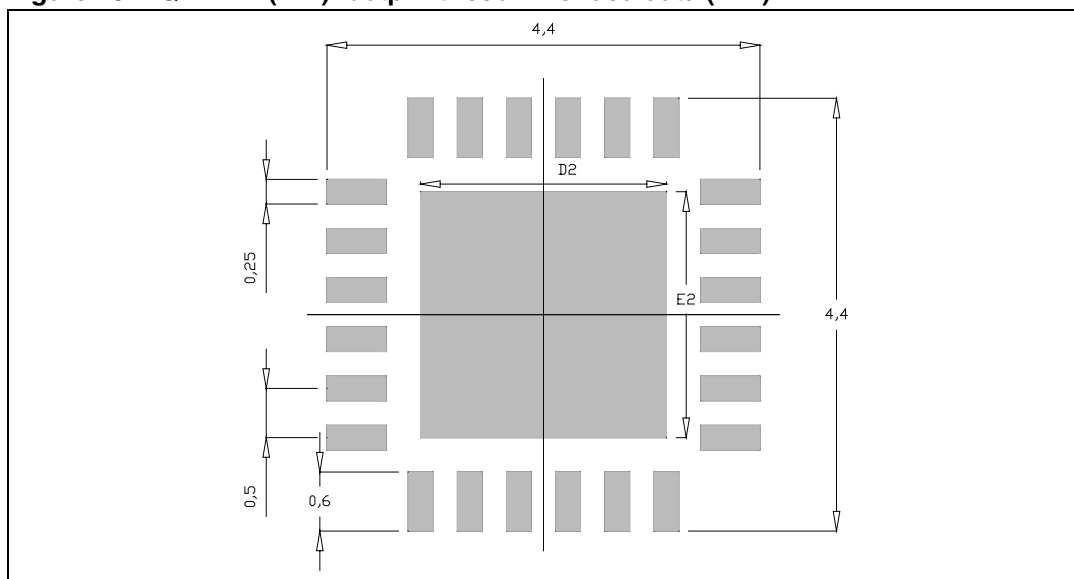


Figure 13. QFN24L (4x4) footprint recommended data (mm)



## 10 Revision history

Table 17. Document revision history

Date	Revision	Changes
01-Mar-2012	1	Initial release.

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