THE DATASHEET OF

SN75LBC182DRG4

SNx5LBC182 Differential Bus Transceiver

1 Features

- One-fourth unit load allows up to 128 devices on a bus
- Meets or exceeds the requirements of ANSI standard TIA/EIA-485-A and ISO 8482: 1987(E)
- Controlled driver output-voltage slew rates allow longer cable stub lengths
- Designed for signaling rates.
  - The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second) up to 250 kbps
- Low disabled supply current: 250-µA maximum
- Thermal shutdown protection
- Open-circuit fail-safe receiver design
- Receiver input hysteresis: 70-mV typical
- Glitch-free power-up and power-down protection

2 Applications

- Utility meters
- Industrial process control
- Building automation

3 Description

The SN65LBC182 and SN75LBC182 are differential data line transceivers with a high level of ESD protection in the trade-standard footprint of the SN75176. They are designed for balanced transmission lines and meet ANSI standard TIA/EIA-485-A and ISO 8482. The SN65LBC182 and SN75LBC182 combine a 3-state, differential line driver and differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control.

The driver outputs and the receiver inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus. This port operates over a wide range of common-mode voltage, making the device suitable for party-line applications. The device also includes additional features for party-line data buses in electrically noisy environment applications such as industrial process control or power inverters.

The SN75LBC182 and SN65LBC182 bus pins also exhibit a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus. The high ESD tolerance protects the device for cabled connections. (For an even higher level of protection, see the SN65/75LBC184, literature number SLLS236.)

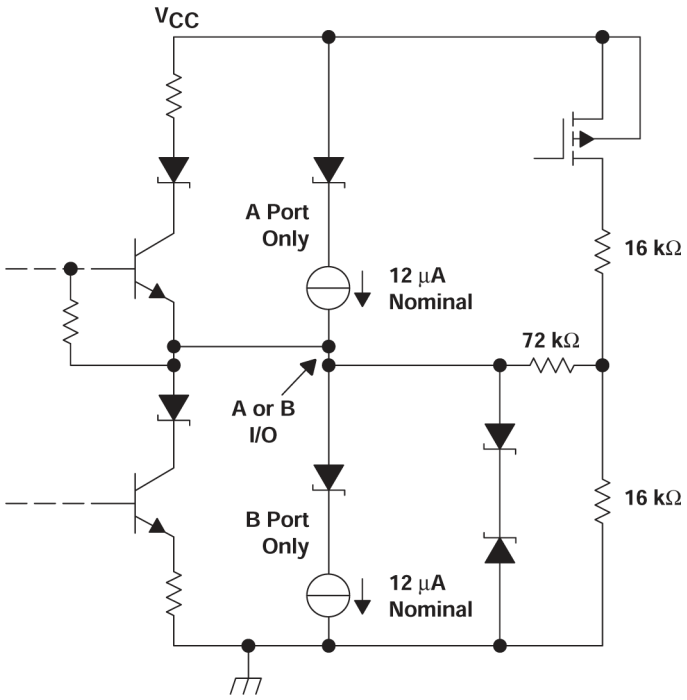
The differential driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled voltage transitions. The receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). Very low device supply current can be achieved by disabling the driver and the receiver.

The SN65LBC182 is characterized for operation from −40°C to 85°C, and the SN75LBC182 is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN65LBC182, SN75LBC182	P (PDIP, 8)	9.81 mm × 9.43 mm
	D (SOIC, 8)	4.9 mm × 6 mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Schematic of Inputs and Outputs

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4 Pin Configuration and Functions

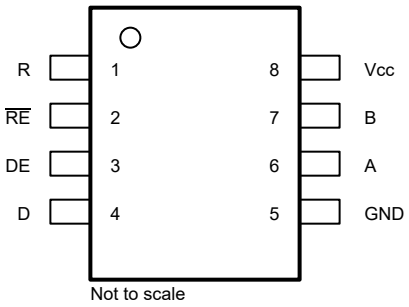


Figure 4-1. P (PDIP) or D (SOIC) Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Receiver Output
$\overline{RE}$	2	I	Active Low Receiver Enable Input
DE	3	I	Active High Driver Enable Input
D	4	I	Driver Input
GND	5	GND	Device GND
A	6	I/O	Non-Inverting Differential Bus I/O
B	7	I/O	Inverting Differential Bus I/O
V_{CC}	8	PWR	Device VCC (4.75V to 5.25V)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free−air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range, (see (2))	−0.5	7	V
(A or B)	Voltage range at any bus terminal	−15	15	V
V_I (D, DE, R or $\overline{RE}$)	Input voltage	−0.3	7	V
I_O	Receiver output current		±20	mA
	Continuous total power dissipation		See *Dissipation Rating* table	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, GND	±15	kV
		All pins	±3	
	IEC 61000-4-2 contact discharge	A, B, GND	±8	kV
	IEC 61000-4-2 Air-gap discharge	A, B, GND	±15	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Dissipation Rating

PACKAGE(2)	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal (separately or common mode) V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}				0.8	
Differential input voltage, V_{ID} (see (1))		−12		12	V
Output current, I_O	Driver	−60		60	mA
	Receiver	−8		4	
Operating free-air temperature, T_A	SN65LBC182	−40		85	°C
	SN75LBC182	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.5 Thermal Information

THERMAL METRIC[1]		D (SOIC)	P (PDIP)	UNIT
		8-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.6 Driver Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA		−1.5			V
V_O	Output voltage		I_O = 0		0		V_{CC}	V
$\lvert V_{OD}\rvert$	Differential output voltage		R_L = 54 Ω,	See Figure 6-1	1.5	2.2	V_{CC}	V
			V_{test} = −7 V to 12 V,	See Figure 6-2	1.5	2.2	V_{CC}	V
ΔV_{OD}	Change in magnitude of differential output voltage		See Figure 6-1		−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1		3	
ΔVOC(SS)	Change in steady-state common-mode output voltage		See Figure 6-1 and Figure 6-4		−0.2		0.2	
VOC(PP)	Peak-to-peak change in common-mode output voltage during state transitions					0.8		V
I_{OZ}	High-impedance output current		See receiver input currents					
I_{IH}	High-level input current (D, DE)		V_I = 2.4 V				50	µA
I_{IL}	Low-level input current (D, DE)		V_I = 0.4 V		−50			µA
I_{OS}	Short-circuit output current		V_O = −7 V to 12 V		−250		250	mA
I_{CC}	Supply current	SN75LBC182	No load, DE at V_{CC},	$\overline{RE}$ at V CC		12	25	mA
		SN65LBC182				12	30	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					0.2	V
V_{IT-}	Negative-going input threshold voltage			−0.2			
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})				70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA		−1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_O = −8 mA,	See Figure 6-7	2.8			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, I_O = 4 mA,	See Figure 6-7			0.4	V

5.7 Receiver Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
I_{OZ}	High-impedance-state output current	V_O = 0.4 to 2.4 V				±1	µA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V	Other input at 0 V			250	µA
		V_{IH} = 12 V, V_{CC} = 0 V				250	
		V_{IH} = −7 V, V_{CC} = 5 V		−200			
		V_{IH} = −7 V, V_{CC} = 0 V		−200			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V				50	µA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V		−50			µA
I_{CC}	Supply current	No load	DE at 0 V, $\overline{RE}$ at 0 V			3.5	mA
			DE at 0 V, $\overline{RE}$ at V_{CC}		175	250	µA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	R_L = 54 Ω, See Figure 6-3	C_L = 50 pF,	0.25	0.72	1.2	µs
t_f	Differential output signal fall time			0.25	0.73	1.2	
t_{PLH}	Propagation delay time, low-to-high-level output					1.3	
t_{PHL}	Propagation delay time, high-to-low-level output					1.3	
$t_{sk(p)}$	Pulse skew (t_{PHL} − t_{PLH})				0.075	0.15	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 6-5			3.5	µs
t_{PHZ}	Output disable time from high level					3.5	
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 6-6			3.5	µs
t_{PLZ}	Output disable time from low level					3.5	

5.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	C_L = 50 pF,	See Figure 6-7		20		ns
t_f	Differential output signal fall time				20		
t_{PLH}	Propagation delay time, low-to-high-level output					150	
t_{PHL}	Propagation delay time, high-to-low-level output					150	
t_{PZH}	Output enable time to high level	See Figure 6-8				100	ns
t_{PZL}	Output enable time to low level					100	
t_{PHZ}	Output disable time from high level					100	ns
t_{PLZ}	Output disable time from low level					100	
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$					50	ns

5.10 Typical Characteristics

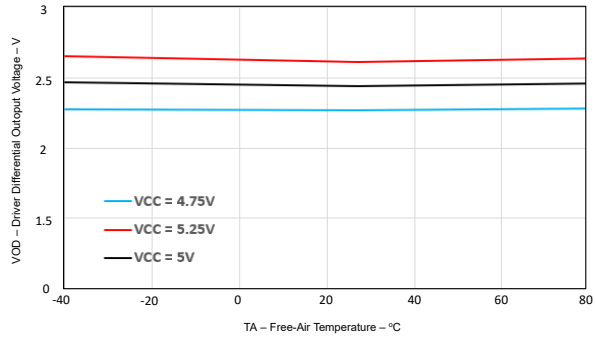


Figure 5-1. Driver Differential Output Voltage vs Temperature

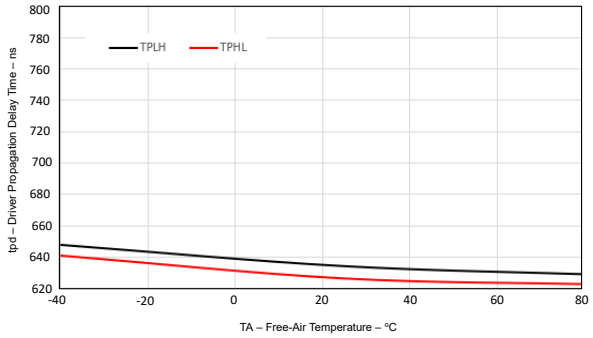


Figure 5-2. Driver Propagation Delay Time vs Temperature

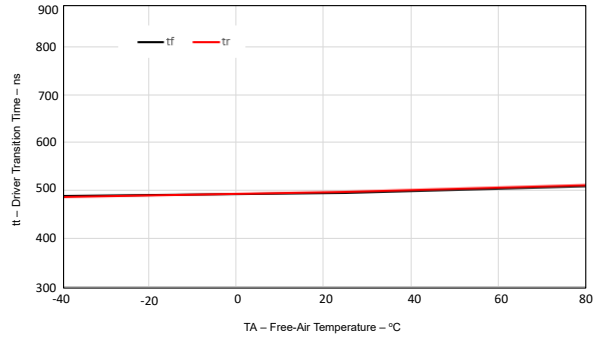


Figure 5-3. Driver Transition Time vs Temperature

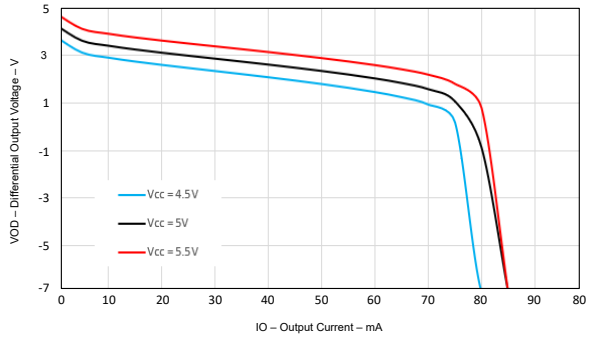


Figure 5-4. Differential Output Voltage vs Output Current

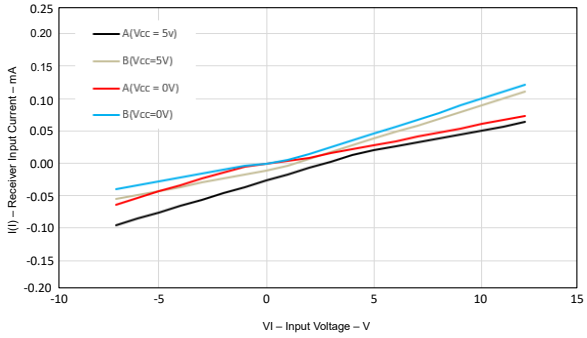
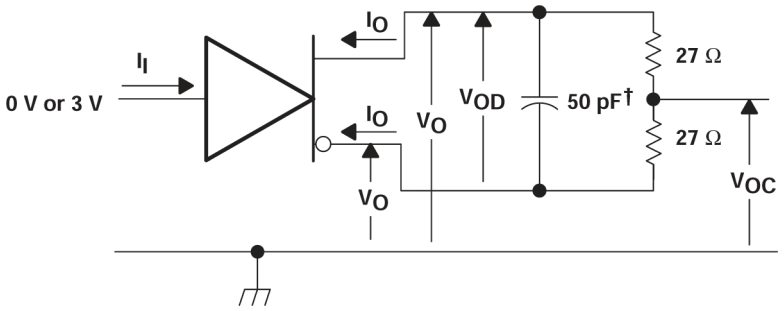


Figure 5-5. Receiver Input Current vs Input Voltage

6 Parameter Measurement Information



A. Includes probe and jig capacitance

Figure 6-1. Driver Test Circuit, v_{OD} And v_{OC} Without Common-Mode Loading

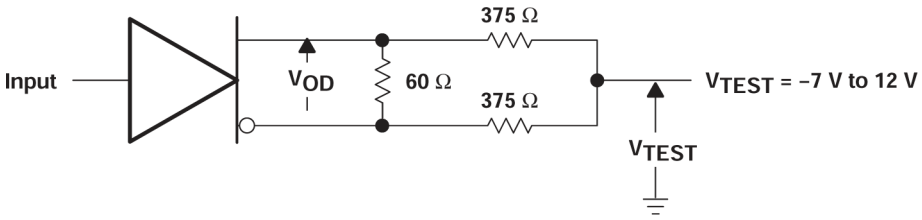
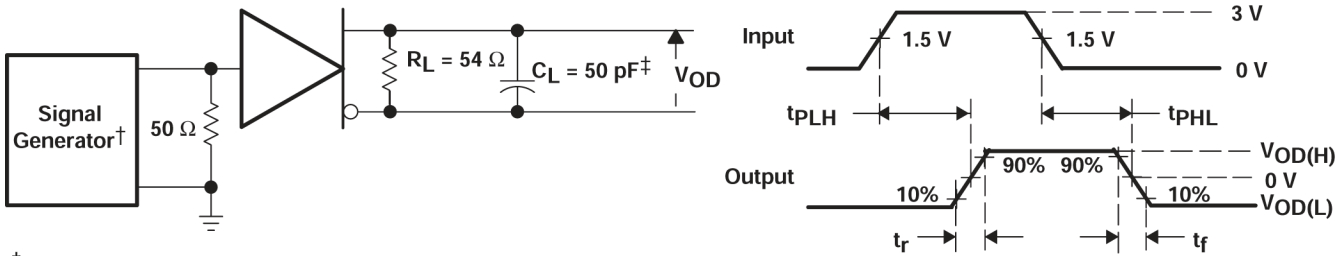


Figure 6-2. Driver Test Circuit, v_{OD} With Common-Mode Loading



A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω
B. Includes probe and jig capacitance

Figure 6-3. Driver Switching Test Circuit and Waveforms

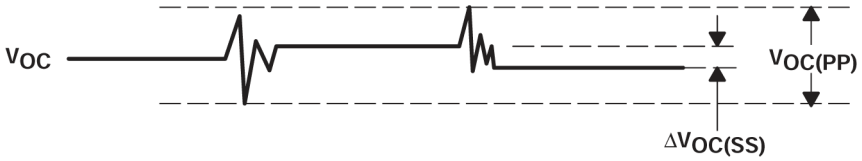
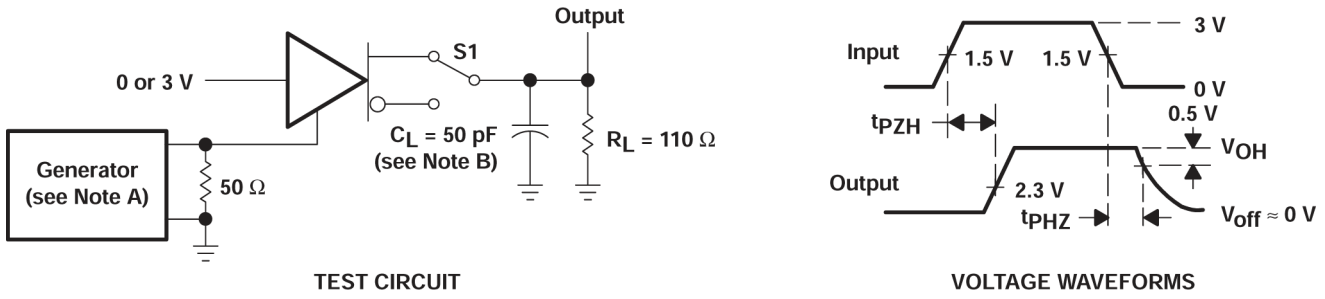


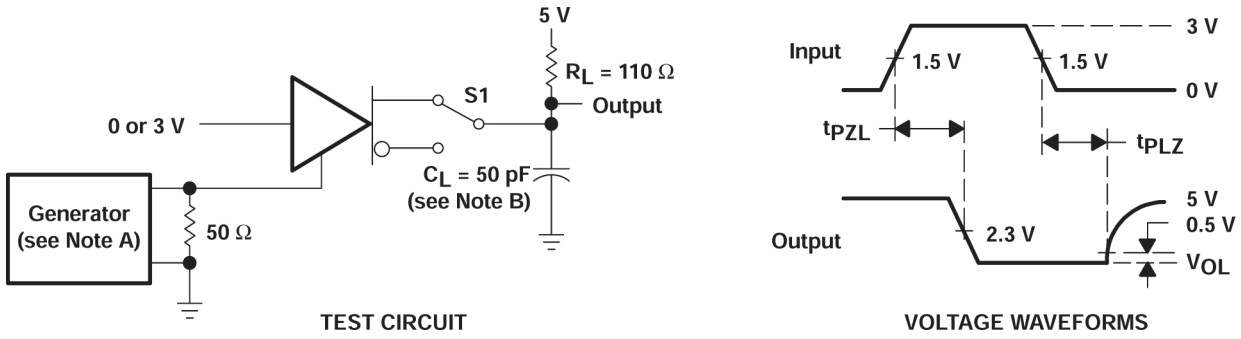
Figure 6-4. V_{OC} Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

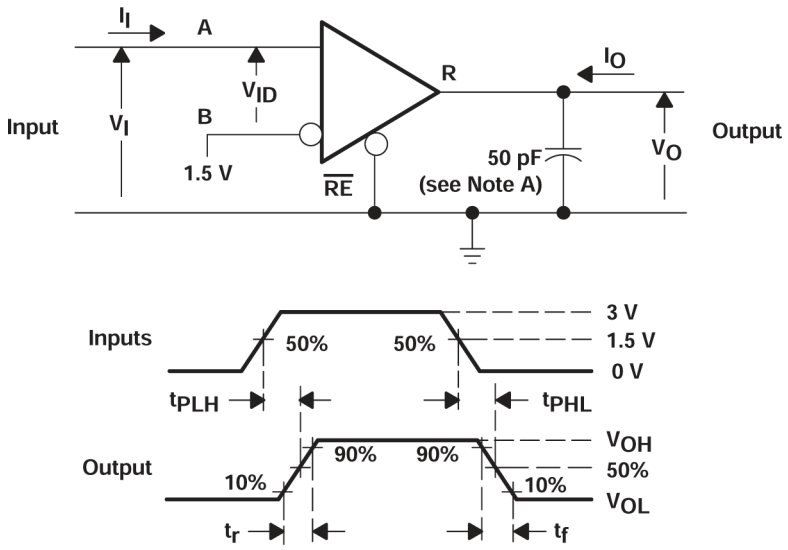
Figure 6-5. Driver T_{PZH} And T_{PHZ} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.

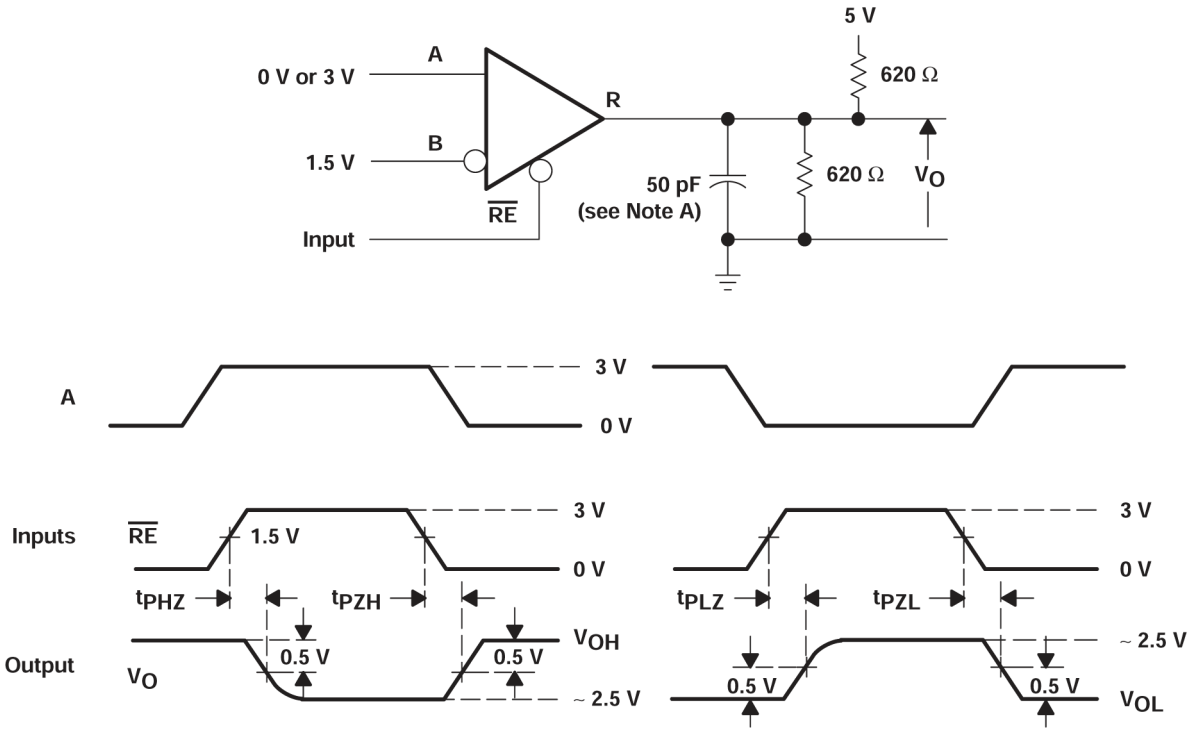
B. C_L includes probe and jig capacitance.

Figure 6-6. Driver T_{PZL} And T_{PLZ} Test Circuit and Voltage Waveforms



A. This value includes probe and jig capacitance (± 10%).

Figure 6-7. Receiver T_{PLH} And T_{PHL} Test Circuit and Voltage Waveforms

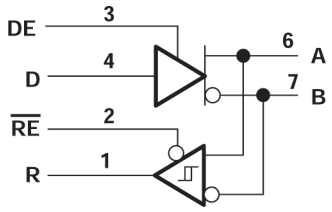


A. This value includes probe and jig capacitance (± 10%).

Figure 6-8. Receiver T_{PZL}, T_{PLZ}, T_{PZH}, And T_{PHZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

Table 7-1. Function Tables Driver

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

Table 7-2. Function Tables Receiver

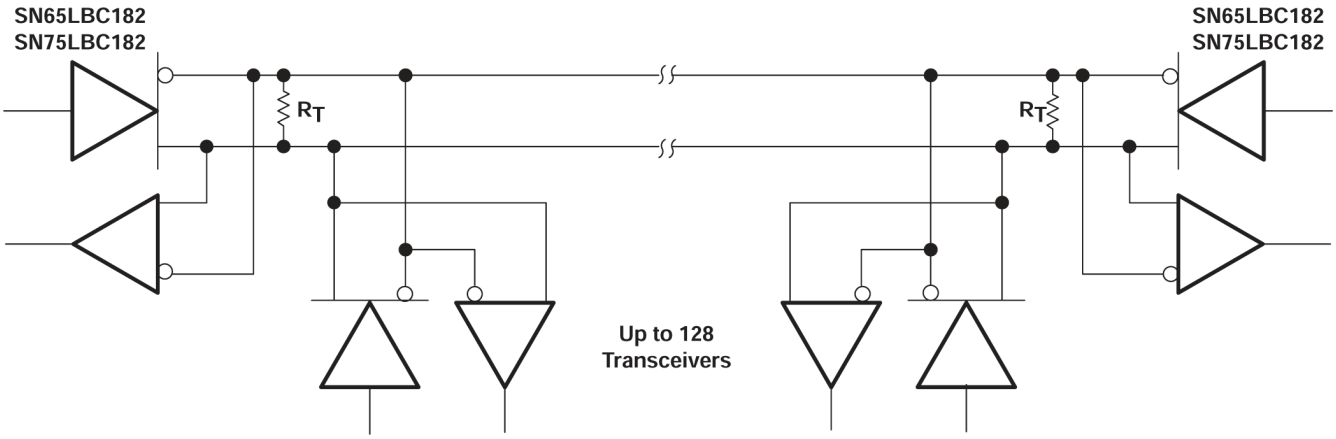
DIFFERENTIAL INPUTS	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information



A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2005) to Revision B (October 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC182D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	
SN65LBC182DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC182	Samples
SN75LBC182D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	
SN75LBC182DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	
SN75LBC182DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182P	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC182	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

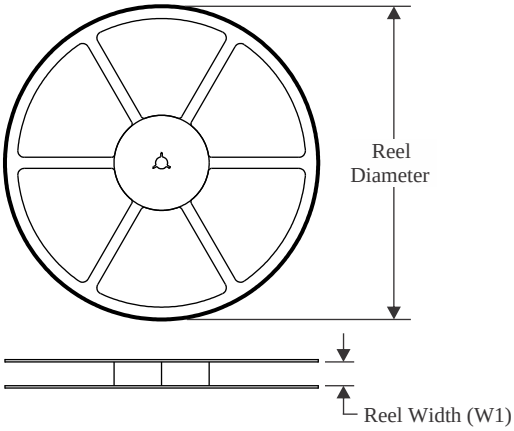
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

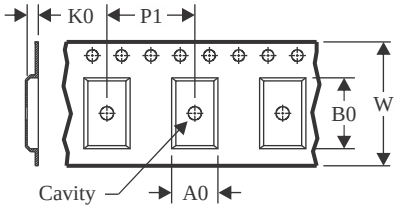
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

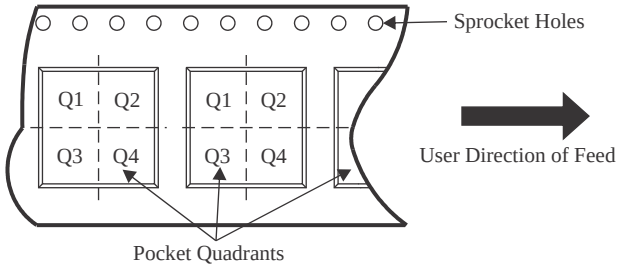


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

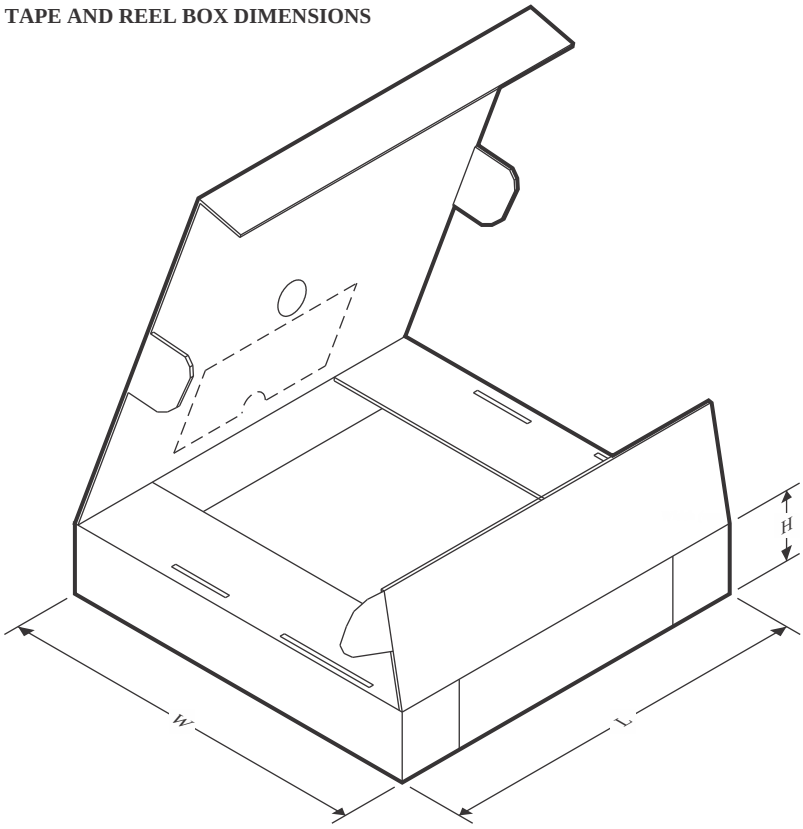
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

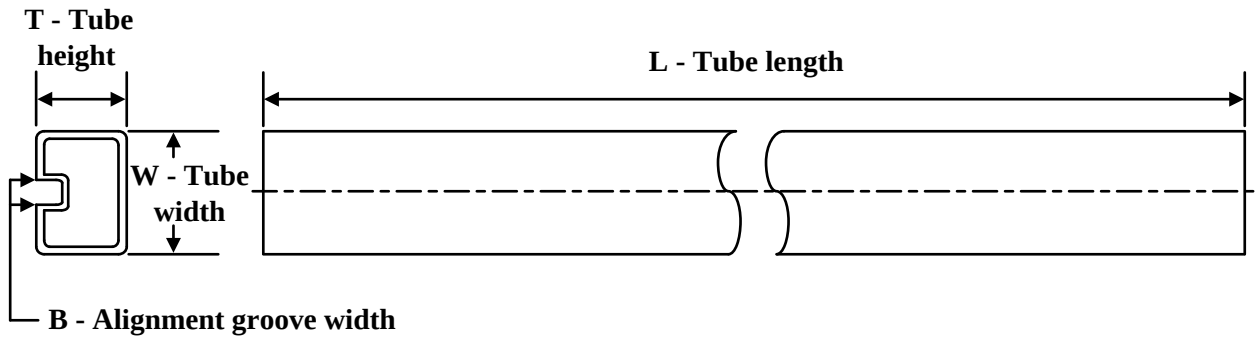
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

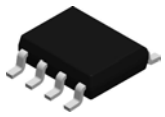
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC182DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC182DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC182D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LBC182D	D	SOIC	8	75	507	8	3940	4.32
SN65LBC182P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC182D	D	SOIC	8	75	507	8	3940	4.32
SN75LBC182DG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC182P	P	PDIP	8	50	506	13.97	11230	4.32

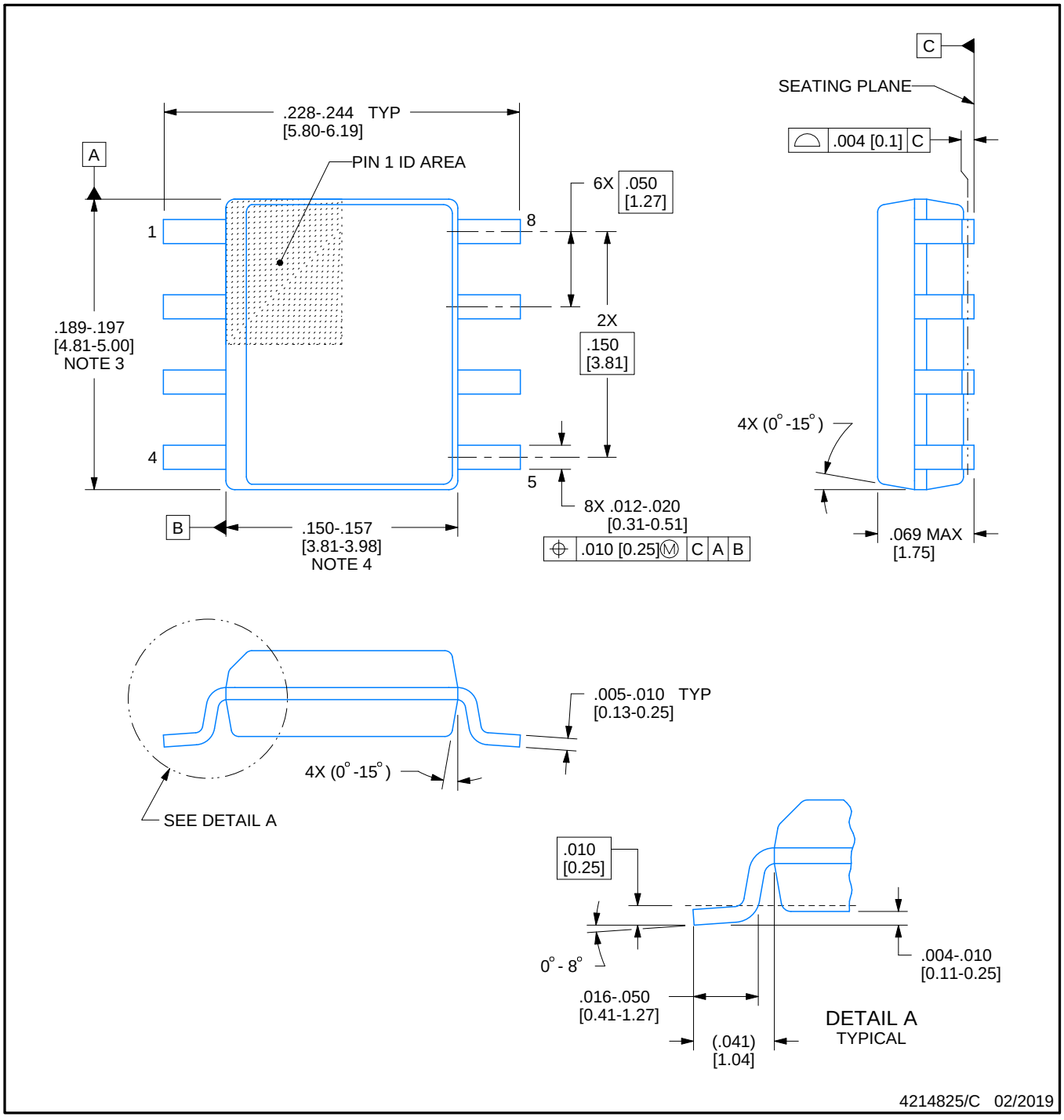


PACKAGE OUTLINE

D0008A

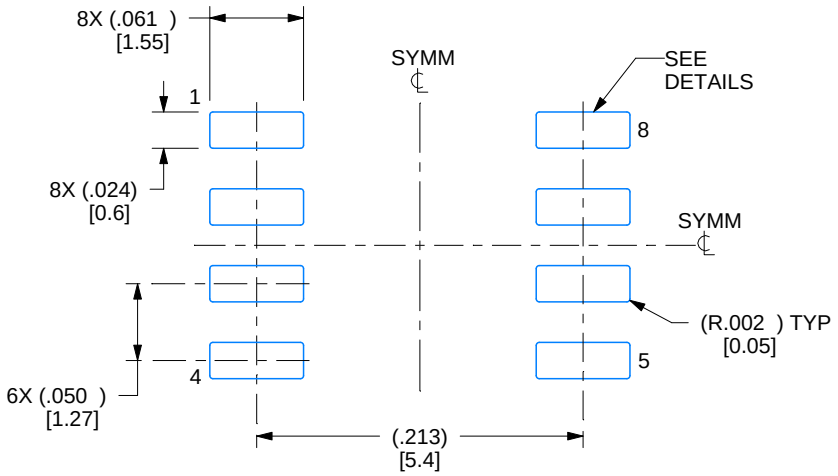
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

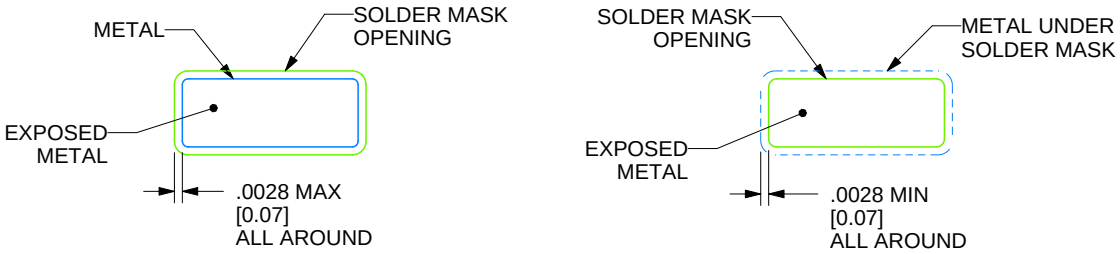


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

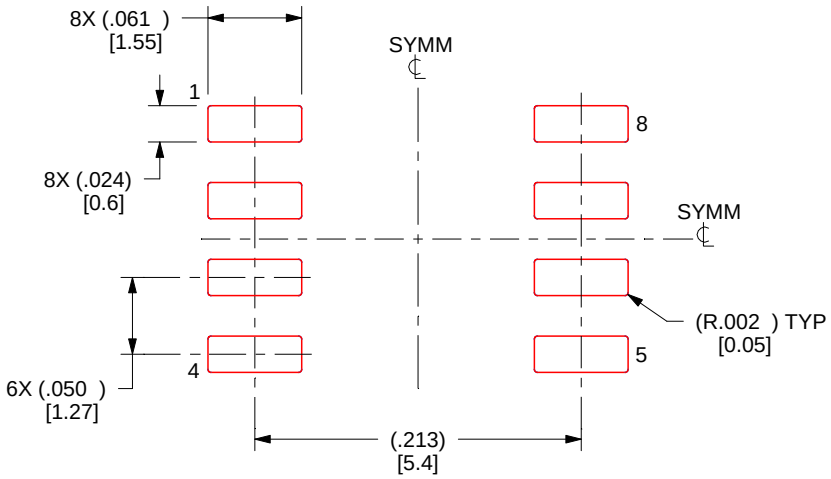
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



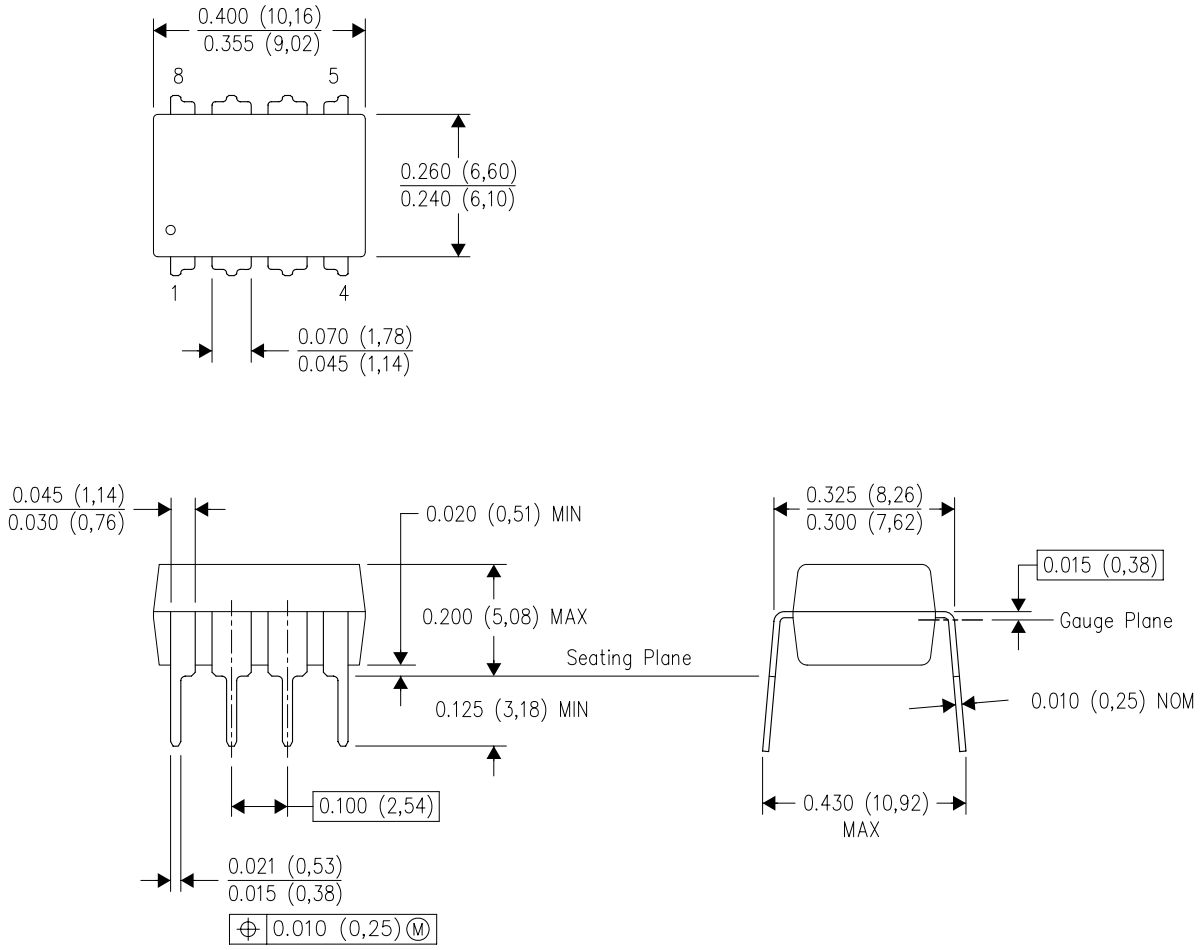
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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