



THE DATASHEET OF UC2524DWTR

ADVANCED REGULATING PULSE WIDTH MODULATORS

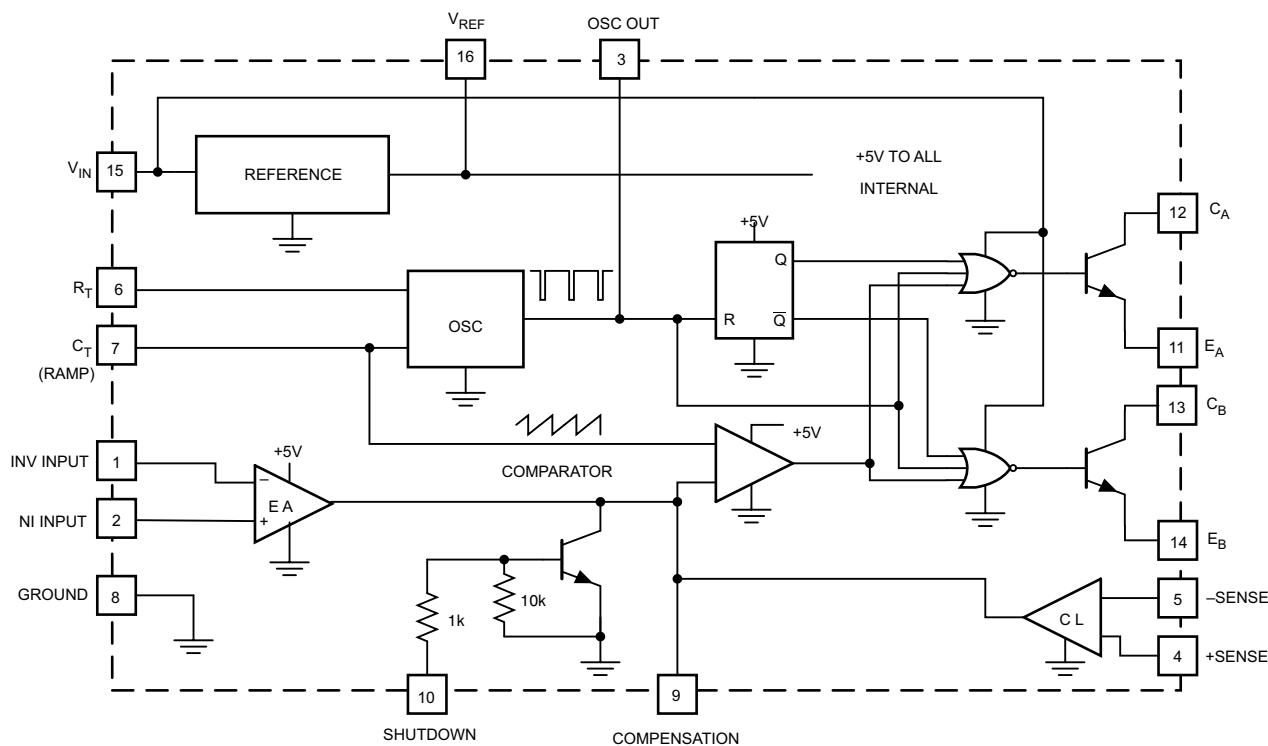
FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Applications
- Low Standby Current . . . 8 mA Typical
- Interchangeable With SG1524, SG2524 and SG3524, Respectively

DESCRIPTION

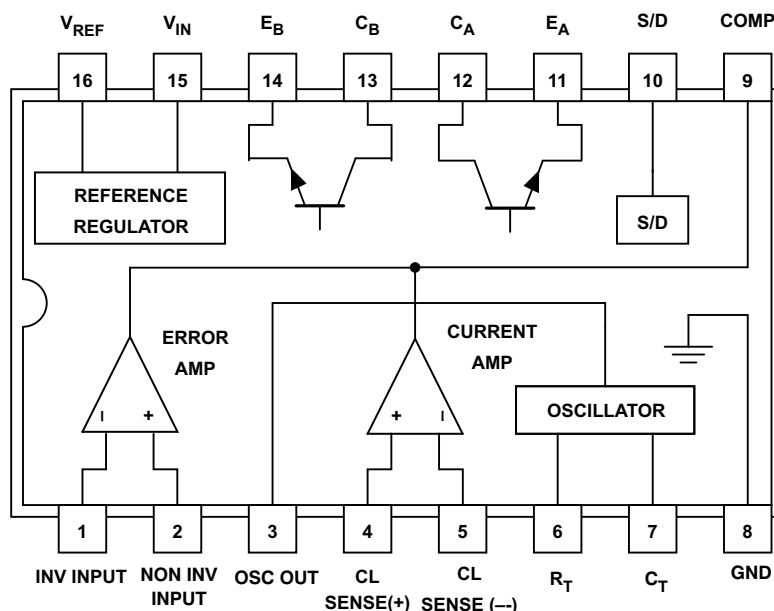
The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to 125°C . The UC2524 and UC3524 are designed for operation from -25°C to 85°C and 0°C to 70°C , respectively.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage ⁽¹⁾⁽²⁾	40 V
	Collector output current	100 mA
	Reference output current	50 mA
	Current through C_T terminal	–50 mA
Power dissipation	$T_A = 25^\circ\text{C}^{(3)}$	1000 mW
	$T_C = 25^\circ\text{C}^{(3)}$	2000 mW
Operating junction temperature range		–55°C to 150°C
Storage temperature range		–65°C to +150°C

(1) All voltage values are with respect to the ground terminal, pin 8.

(2) The reference regulator may be bypassed for operation from a fixed 5 V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6 V.

(3) Consult packaging section of data book for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	8		40	V
	Reference output current	0		20	mA
	Current through C_T terminal	–0.03		–2	mA
R_T	Timing resistor	1.8		100	k Ω
C_T	Timing capacitor	0.001		0.1	μF
Operating ambient temperature range	UC1524	–55		125	°C
	UC2524	–25		85	
	UC3524	0		70	

ELECTRICAL CHARACTERISTICS

these specifications apply for $T_A = -55^\circ\text{C}$ to 125°C for the UC1524, -25°C to 85°C for the UC2524, and 0°C to 70°C for the UC3524, $V_{IN} = 20\text{ V}$, and $f = 20\text{ kHz}$, $T_A = T_J$, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	V _{IN} = 8 V to 40 V		10	20		10	30	mV
Load regulation	I _L = 0 mA to 20 mA		20	50		20	50	mV
Ripple rejection	f = 120 Hz, T _J = 25°C		66			66		dB
Short circuit current limit	V _{REF} = 0, T _J = 25°C		100			100		mA
Temperature stability	Over operating temperature range		0.3%	1%		0.3%	1%	
Long term stability	T _J = 125°C, t = 1000 Hrs		20			20		mV
OSCILLATOR SECTION								
Maximum frequency	C _T = 1 nF, R _T = 2 kΩ		300			300		kHz
Initial accuracy	R _T and C _T constant		5%			5%		
Voltage stability	V _{IN} = 8 V to 40 V, T _J = 25°C			1%			1%	
Temperature stability	Over operating temperature range			5%			5%	
Output amplitude	Pin 3, T _J = 25°C		3.5			3.5		V
Output pulse width	C _T = 0.01 mfd, T _J = 25°C		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	V _{CM} = 2.5 V		0.5	5		2	10	mV
Input bias current	V _{CM} = 2.5 V		2	10		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	T _J = 25°C	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	T _J = 25°C		70			70		dB
Small signal bandwidth	A _V = 0 dB, T _J = 25°C		3			3		MHz
Output voltage	T _J = 25°C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty-cycle	% Each output on	0%		45%	0%		45%	
Input threshold	Zero duty-cycle		1			1		V
	Maximum duty-cycle		3.5			3.5		
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2 V with error amplifier set for maximum out, T _J = 25°C	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV/°C
Common mode voltage	T _J = −55°C to 85°C for the −1 V to 1 V limit	−1		1	−1		1	V
	T _J = 25°C	−0.3		1				
OUTPUT SECTION (EACH OUTPUT)								
Collector-emitter voltage		40			40			V
Collector leakage current	V _{CE} = 40 V		0.1	50		0.1	50	μ A
Saturation voltage	I _C = 50 mA		1	2		1	2	V
Emitter output voltage	V _{IN} = 20 V	17	18		17	18		V
Rise Time	R _C = 2 kΩ, T _J = 25°C		0.2			0.2		μs
Fall Time	R _C = 2 kΩ, T _J = 25°C		0.1			0.1		μs
Total standby current (Note)	V _{IN} = 40 V		8	10		8	10	mA

PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T), and one timing capacitor (C_T). R_T establishes a constant charging current for C_T . This results in a linear voltage ramp at C_T , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5 V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T . The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering

flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator. Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION
OF ERROR AMPLIFIER
VS
FREQUENCY

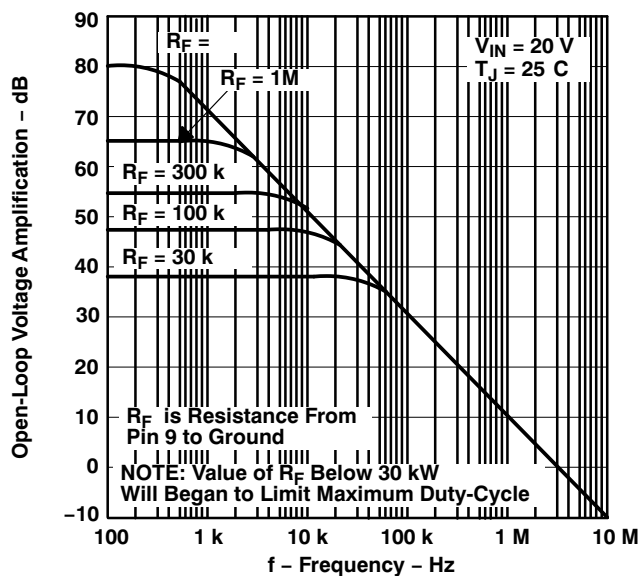


Figure 1.

OSCILLATOR FREQUENCY
VS
TIMING COMPONENTS

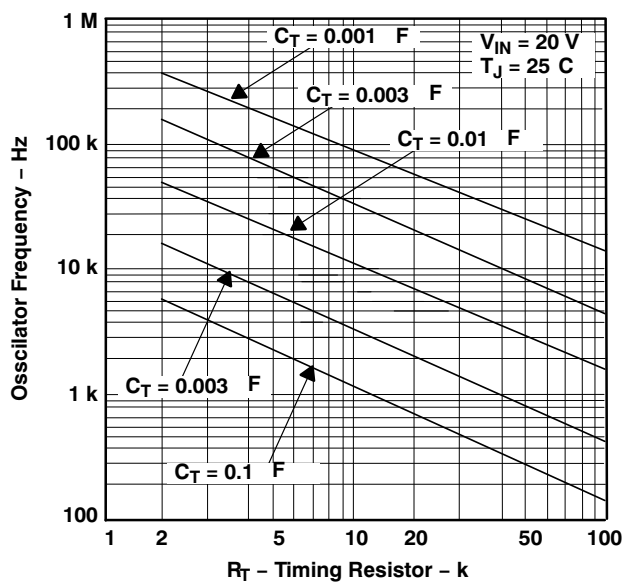


Figure 2.

OUTPUT DEAD TIME
VS
TIMING CAPACITANCE VALUE

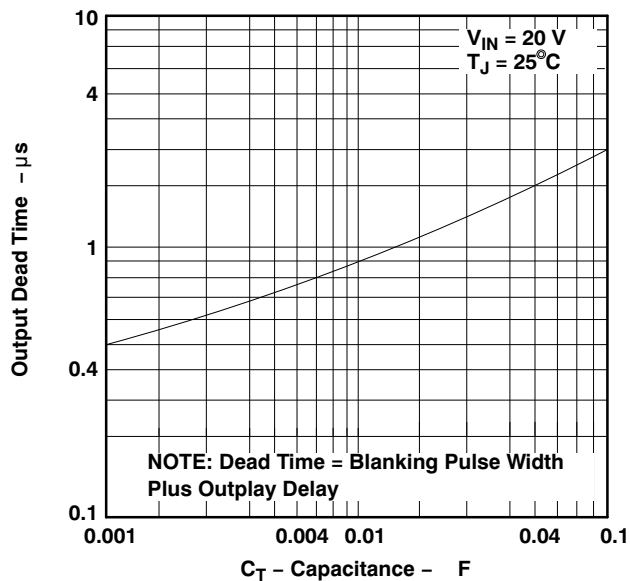


Figure 3.

OUTPUT SATURATION VOLTAGE
VS
LOAD CURRENT

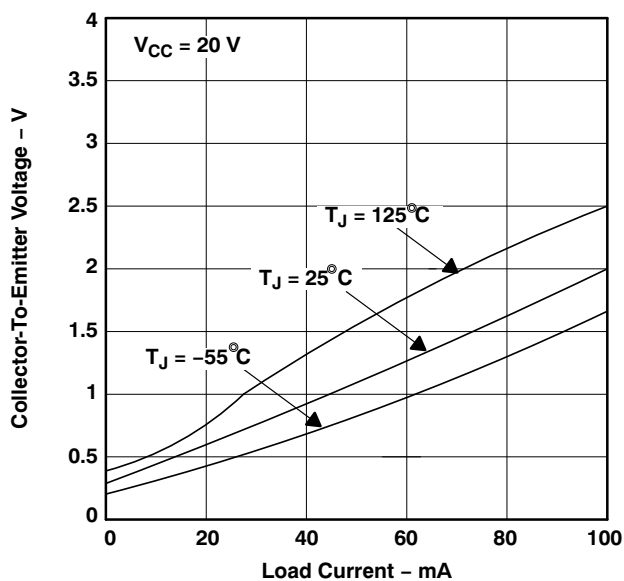


Figure 4.

APPLICATION INFORMATION

OSCILLATOR

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

$$f = \frac{1.18}{R_T C_T} \quad (1)$$

where

R_T is in $k\Omega$

C_T is in μF

f is in kHz

Practical values of C_T fall between 1 nF and 100 nF. Practical values of R_T fall between 1.8 $k\Omega$ and 100 $k\Omega$. This results in a frequency range typically from 120 Hz to 500 kHz.

BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T . If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in Figure 5.

SYNCHRONOUS OPERATIONS

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 $k\Omega$. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operate synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to single timing capacitor, and the timing resistor connected to a single R_T terminal.

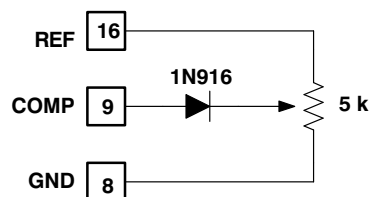


Figure 5. Error Amplifier Clamp

The other R_T terminals can be left open or shorted to V_{REF} . Minimum lead lengths should be used between the C_T terminals.

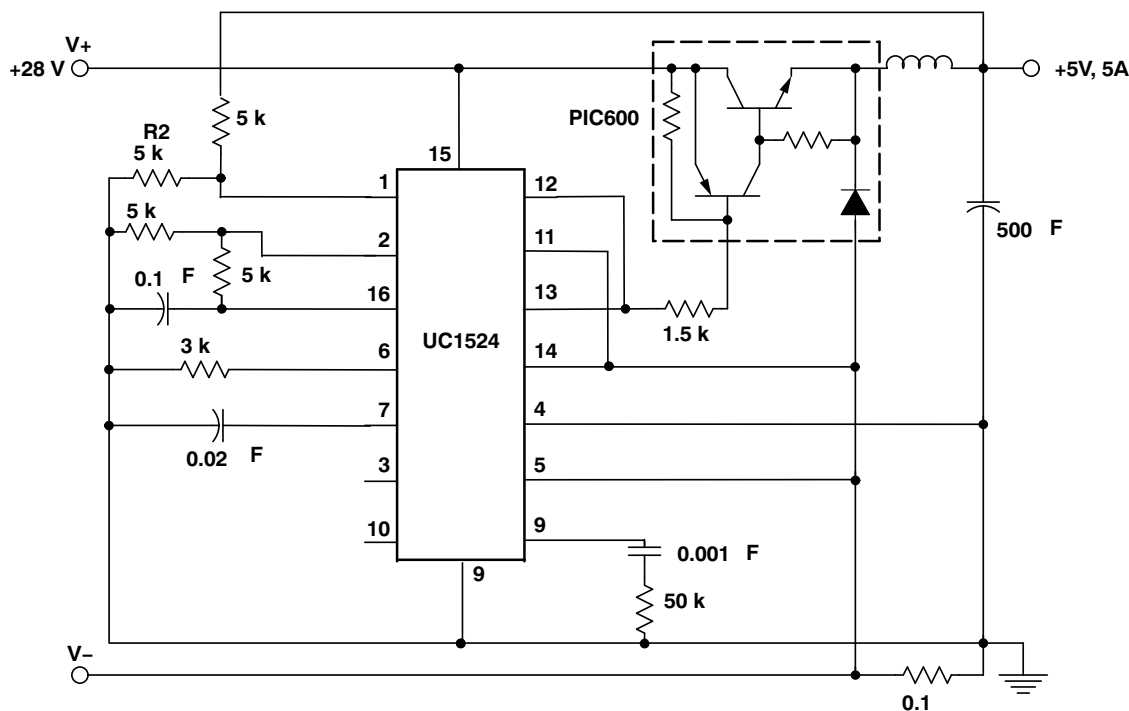


Figure 6. Single-Ended LC Switching Regulator Circuit

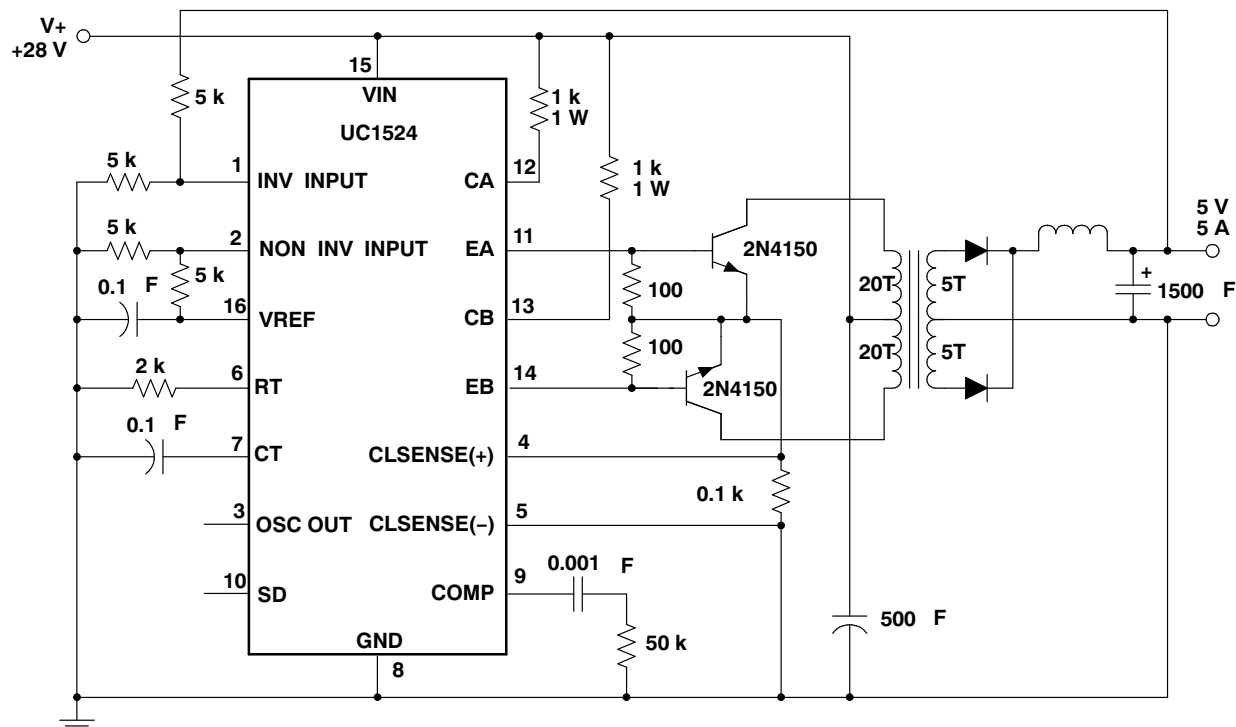


Figure 7. Push-Pull Transformer Coupled Circuit

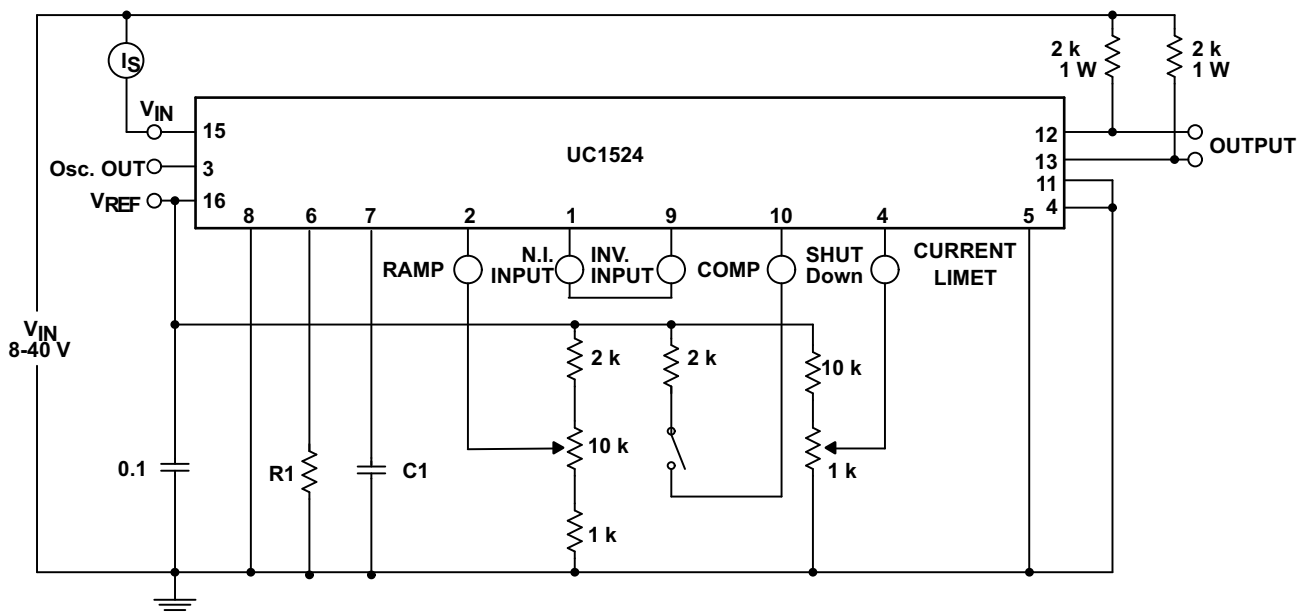


Figure 8. Open Loop Test Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1524J/80937	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1524J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC2524DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2524DW	Samples
UC2524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-25 to 85		
UC3524-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
UC3524D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524D	Samples
UC3524DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524D	Samples
UC3524DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW	Samples
UC3524DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW	Samples
UC3524DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524DW	Samples
UC3524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1524, UC3524 :

- Catalog: [UC3524](#)
- Military: [UC1524](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3524DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3524DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

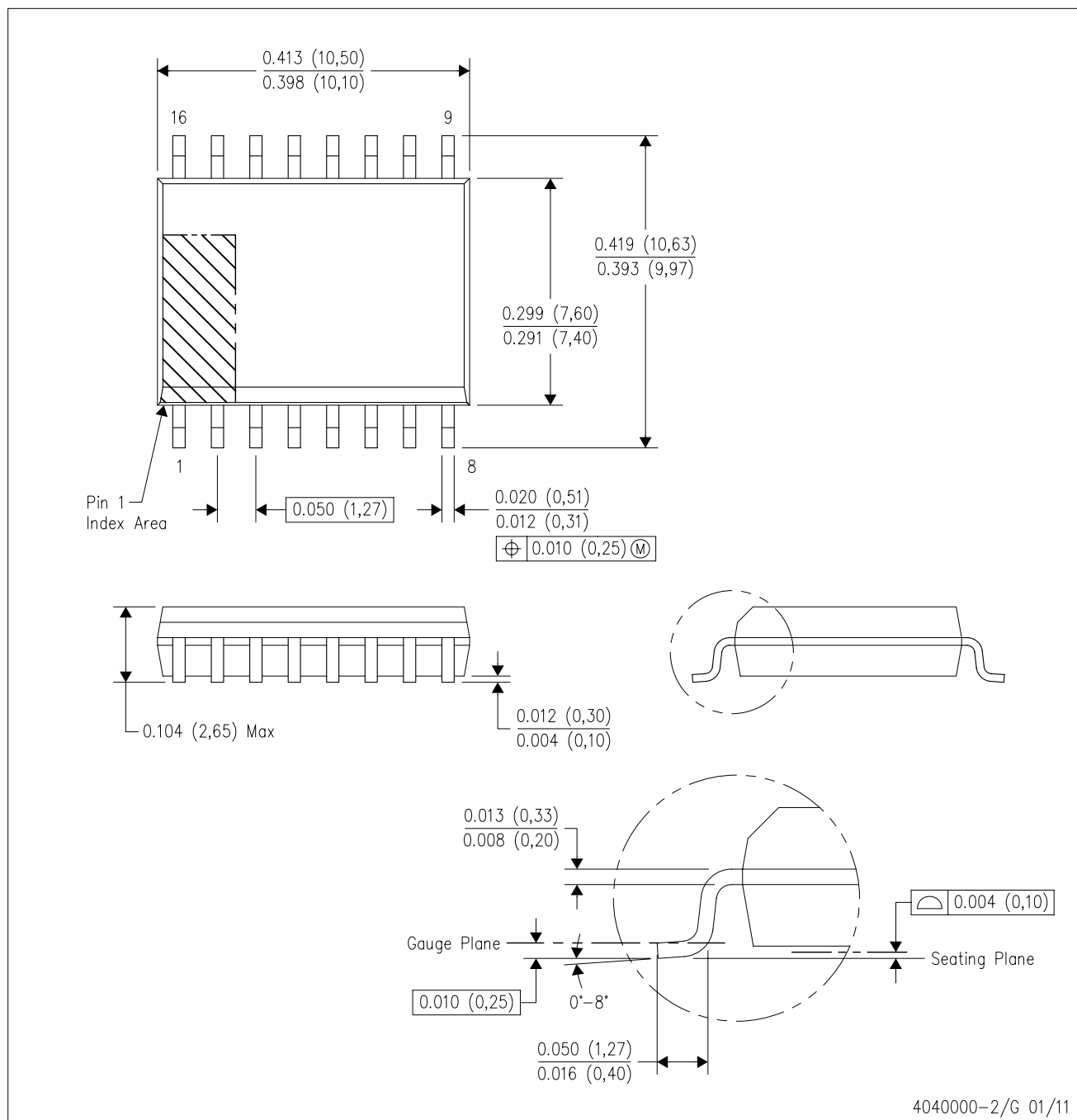
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G16)

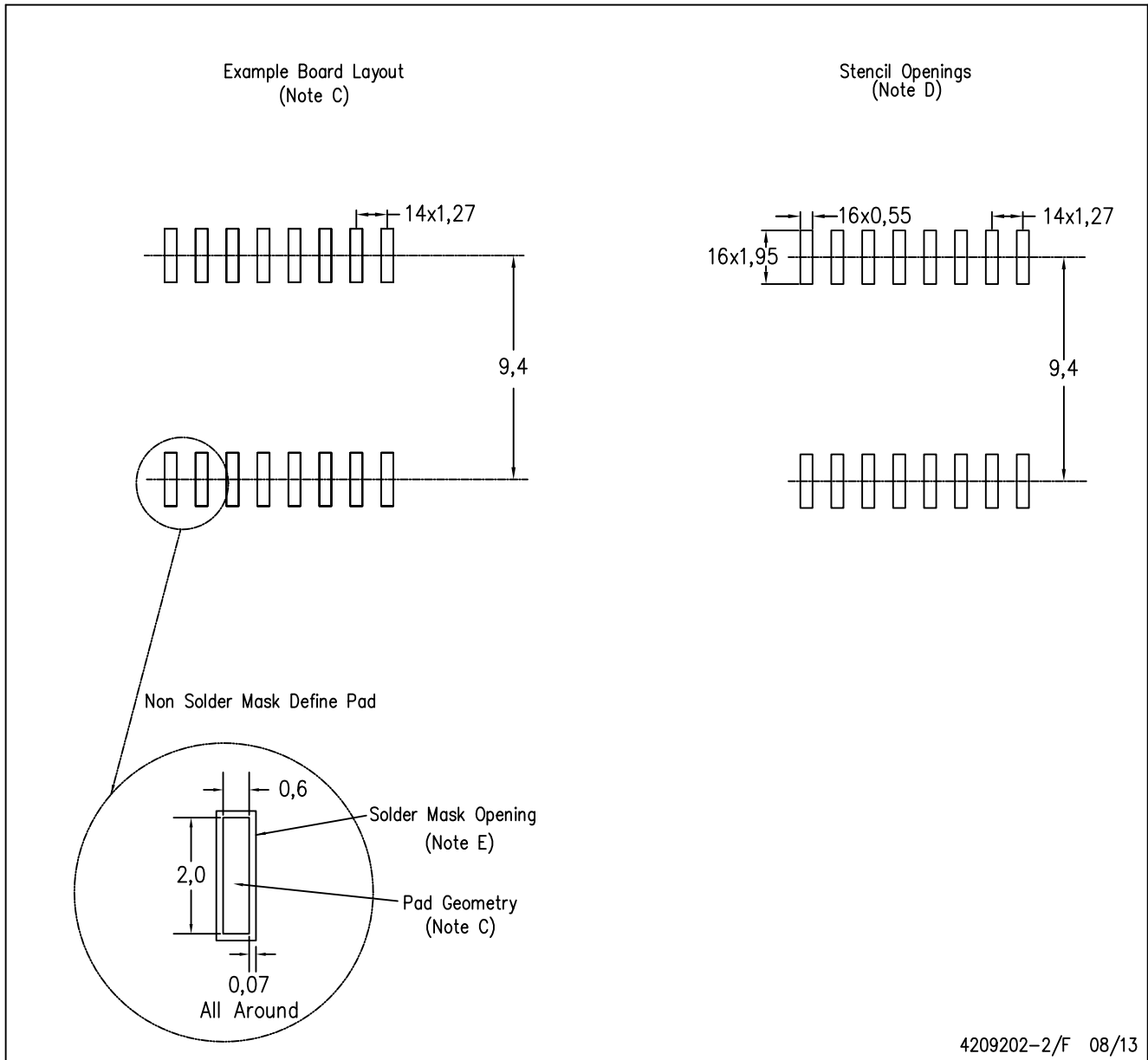
PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ View [UC2524DWTR](#) on WIN SOURCE

⊖ [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management