





## OFF-LINE POWER SUPPLY CONTROLLER

### FEATURES

- Transformerless Off-Line Power Supply
- Wide 100-VDC to 400-VDC Allowable Input Range
- Fixed 5-VDC or Adjustable Low-Voltage Output
- Output Sinks 200 mA, Sources 150 mA Into a MOSFET Gate
- Uses Low-Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

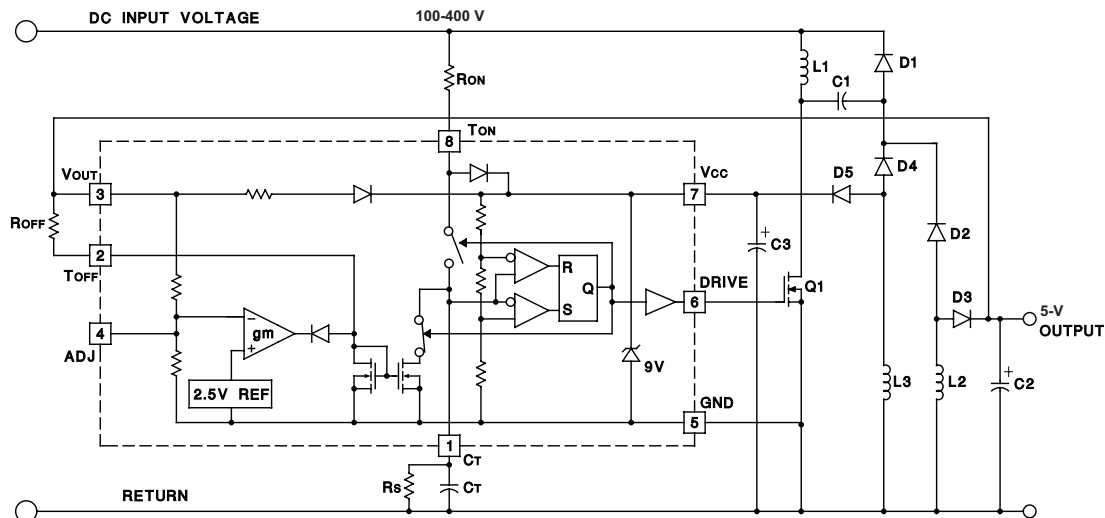
### DESCRIPTION

The UCC3888 controller is optimized for use as an off-line, low-power, low-voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios as high as 400 V to 2.7 V with no transformer and low internal losses.

The control algorithm utilized by the UCC3888 sets the switch on time inversely proportional to the input line voltage and sets the switch off time inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400 V to 2.7 V to be achieved with a switch duty cycle of 7.6%. This topology also offers inherent short circuit protection because as the output voltage falls to zero, the switch-off time approaches infinity.

The output voltage is set internally to 5 V. It can be programmed for other output voltages with two external resistors. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

### TYPICAL APPLICATION



Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

UDG-96013



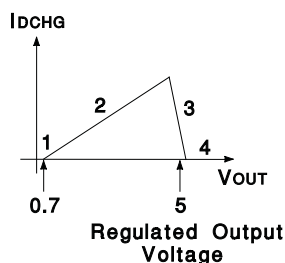
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## THEORY OF OPERATION

With reference to the application diagram below, when input voltage is first applied, the current through  $R_{ON}$  into  $T_{ON}$  is directed to  $V_{CC}$  where it charges the external capacitor,  $C_3$ , connected to  $V_{CC}$ . As voltage builds on  $V_{CC}$ , an internal undervoltage lockout holds the circuit off and the output at DRIVE low until  $V_{CC}$  reaches 8.4 V. At this time, DRIVE goes high, turning on the power switch, Q1, and redirecting the current into  $T_{ON}$  to the timing capacitor,  $C_T$ .  $C_T$  charges to a fixed threshold with a current  $I_{CHG} = 0.8 \cdot (V_{IN} - 4.5 \text{ V})/R_{ON}$ . Because DRIVE is high only as long as  $C_T$  charges, the power switch on time will be inversely proportional to line voltage. This provides a constant (line voltage) • (switch on time) product.

At the end of the on time, Q1 is turned off, and the current through  $R_{ON}$  is again diverted to  $V_{CC}$ . Thus the current through  $R_{ON}$ , which charges  $C_T$  during the on time, contributes to supplying power to the chip during the off time.

The power switch off time is controlled by the discharge of  $C_T$ , which, in turn, is programmed by the regulated output voltage. The relationship between  $C_T$  discharge current,  $I_{DCHG}$ , and output voltage is illustrated as follows:



Region 1. When  $V_{OUT} = 0$ , the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high-value resistor,  $R_S$ , is placed in parallel with  $C_T$  to establish a minimum switching frequency.

Region 2. As  $V_{OUT}$  rises above approximately 0.7 V to its regulated value,  $I_{DCHG}$  is defined by  $R_{OFF}$ , and is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As  $V_{OUT}$  increases,  $I_{DCHG}$  increases reducing off time. The operating frequency increases and  $V_{OUT}$  rises quickly to its regulated value.

Region 3. In this region, a transconductance amplifier reduces  $I_{DCHG}$  to maintain a regulated  $V_{OUT}$ .

Region 4. If  $V_{OUT}$  should rise above its regulation range,  $I_{DCHG}$  falls to zero and the circuit returns to the minimum frequency established by  $R_S$  and  $C_T$ .

The range of switching frequencies is established by  $R_{ON}$ ,  $R_{OFF}$ ,  $R_S$ , and  $C_T$  as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \cdot C_T \cdot 4.6 \text{ V}/(V_{IN} - 4.5 \text{ V})$$

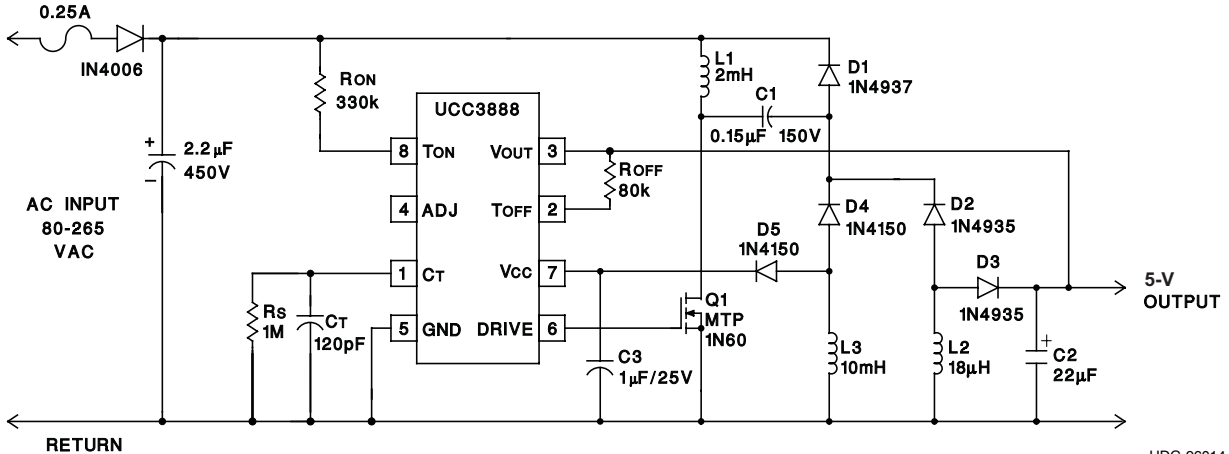
$$T_{OFF} (\text{max}) = 1.4 \cdot R_S \cdot C_T \text{ Regions 1 and 4}$$

$$T_{OFF} = R_{OFF} \cdot C_T \cdot 3.7 \text{ V}/(V_{OUT} - 0.7 \text{ V}) \text{ Region 2, excluding the effects of } R_S, \text{ which have a minimal impact on } T_{OFF}.$$

The above equations assume that  $V_{CC}$  equals 9 V. The voltage at  $T_{ON}$  increases from approximately 2.5 V to 6.5 V while  $C_T$  is charging. To take this into account,  $V_{IN}$  is adjusted by 4.5 V in the calculation of  $T_{ON}$ . The voltage at  $T_{OFF}$  is approximately 0.7 V.

## DESIGN EXAMPLE

The UCC3888 regulates a 5 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.2 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100 kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.



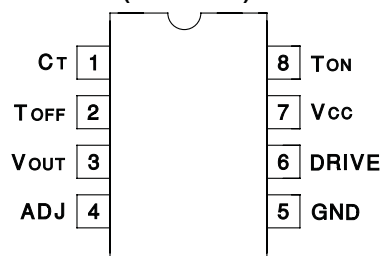
UDG-96014

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

	VALUE	UNIT
$I_{CC}$	8	mA
Current into T <sub>ON</sub> Pin	1.5	
Voltage on V <sub>OUT</sub> Pin	20	V
Current into T <sub>OFF</sub> Pin	250	µA
Storage temperature	-65 to 150	°C

(1) Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

### N OR J, D PACKAGE (TOP VIEW)



## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for the UCC3888, and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the UCC2888. No load at DRIVE pin ( $C_{LOAD} = 0$ ).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>General</b>					
$V_{CC}$ Zener voltage	$I_{CC} < 1.5 \text{ mA}$	8.6	9	9.3	V
Startup current	$V_{OUT} = 0$		150	250	$\mu\text{A}$
Operating current $I(V_{CC})$	$V_{CC} = V_{CC(\text{zener})} - 100 \text{ mV}$ , $F = 150 \text{ kHz}$		1.2	2.5	$\text{mA}$
<b>Under-Voltage-Lockout</b>					
Start threshold	$V_{OUT} = 0$	8	8.4	8.8	V
Minimum operating voltage after start	$V_{OUT} = 0$	6	6.3	6.6	
Hysteresis	$V_{OUT} = 0$	1.8			
<b>Oscillator</b>					
Amplitude	$V_{CC} = 9 \text{ V}$	3.5	3.7	3.9	V
$C_T$ to DRIVE high propagation delay	Overdrive = 0.2 V		100	200	ns
$C_T$ to DRIVE low propagation delay	Overdrive = 0.2 V		50	100	
<b>Driver</b>					
VOL	$I = 20 \text{ mA}$ , $V_{CC} = 9 \text{ V}$		0.15	0.4	V
	$I = 100 \text{ mA}$ , $V_{CC} = 9 \text{ V}$		0.7	1.8	
VOH	$I = -20 \text{ mA}$ , $V_{CC} = 9 \text{ V}$	8.5	8.8		
	$I = -100 \text{ mA}$ , $V_{CC} = 9 \text{ V}$	6.1	7.8		
Rise time	$C_{LOAD} = 1 \text{ nF}$		35	70	ns
Fall time	$C_{LOAD} = 1 \text{ nF}$		30	60	
<b>Line Voltage Detection</b>					
Charge coefficient: $I_{CHG}/I(T_{ON})$	$V_{CT} = 3 \text{ V}$ , DRIVE = High, $I(T_{ON}) = 1 \text{ mA}$	0.73	0.79	0.85	
Minimum line voltage for fault	$R_{ON} = 330\text{k}$	60	80	100	V
Minimum current $I(T_{ON})$ for fault	$R_{ON} = 330\text{k}$		220		$\mu\text{A}$
On time during fault	$C_T = 150 \text{ pF}$ , $V_{LINE} = \text{Min} - 1 \text{ V}$		2		$\mu\text{s}$
Oscillator restart delay after fault			0.5		ms
<b><math>V_{OUT}</math> Error Amp</b>					
$V_{OUT}$ regulated 5 V (ADJ open)	$V_{CC} = 9 \text{ V}$ , $I_{DCHG} = I(T_{OFF})/2$	4.5	5	5.5	V
Discharge ratio: $I_{DCHG} / I(T_{OFF})$	$I(T_{OFF}) = 50 \mu\text{A}$	0.9	1	1.1	
Voltage at $T_{OFF}$	$I(T_{OFF}) = 50 \mu\text{A}$	0.6	0.95	1.3	
Regulation $gm^{(1)}$	Max $I_{DCHG} = 50 \mu\text{A}$		2.4		$\text{mA/V}$
	Max $I_{DCHG} = 125 \mu\text{A}$	1.9	4.1	7	

(1)  $gm$  is defined as

$$\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$$

for the values of  $V_{OUT}$  when  $V_{OUT}$  is in regulation. The two points used to calculate  $gm$  are for  $I_{DCHG}$  at 65% and 35% of its maximum value.

## PIN DESCRIPTIONS

**ADJ:** The ADJ pin is used to provide a 5-V regulated supply without additional external components. Other output voltages can be obtained by connecting a resistor divider between  $V_{OUT}$ , ADJ and GND. Use the formula:

$$V_{OUT} = 2.5 \text{ V} \cdot \frac{R1+R2}{R2}$$

where R1 is connected between  $V_{OUT}$  and ADJ, and R2 is connected between ADJ and GND.  $R1 \parallel R2$  should be less than 1 k $\Omega$  to minimize the effect of the temperature coefficient of the internal 30-k $\Omega$  resistors, which also connect to  $V_{OUT}$ , ADJ, and GND. See [Figure 1](#).

**$C_T$  (timing capacitor):** The signal voltage at  $C_T$  has a peak-to-peak swing of 3.7 V for 9 V  $V_{CC}$ . As the voltage at  $C_T$  crosses the oscillator upper threshold, DRIVE goes low. As the voltage on  $C_T$  crosses the oscillator lower threshold, DRIVE goes high.

**DRIVE:** This output is a CMOS stage capable of sinking 200 mA peak and sourcing 150 mA peak. The output voltage swing is 0 to  $V_{CC}$ .

**GND (chip ground):** All voltages are measured with respect to GND.

**$T_{OFF}$  (regulated output control):**  $T_{OFF}$  sets the discharge current of the timing capacitor through an external resistor connected between  $V_{OUT}$  and  $T_{OFF}$ .

**$T_{ON}$  (line voltage control):**  $T_{ON}$  serves three functions. When  $C_T$  is discharging (off time), the current through  $T_{ON}$  is routed to  $V_{CC}$ . When  $C_T$  is charging (on time), the current through  $T_{ON}$  is split 80% to set the  $C_T$  charge time and 20% to sense minimum line voltage, which occurs for a  $T_{ON}$  current of 220  $\mu$ A. For a minimum line voltage of 80 V,  $R_{ON}$  is 330 k $\Omega$ .

The  $C_T$  voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the  $T_{ON}$  pin increases from 2.5 V to 6.5 V.

**$V_{CC}$  (chip supply voltage):** The supply voltage of the device at pin  $V_{CC}$  is internally clamped at 9 V. The device needs an external supply, from a source such as the rectified ac line or derived from the switching circuit. Precautions must be taken to ensure that total ICC does not exceed 8 mA.

**$V_{OUT}$  (regulated output):** The  $V_{OUT}$  pin is directly connected to the power supply output voltage. When  $V_{OUT}$  is greater than  $V_{CC}$ ,  $V_{OUT}$  bootstraps  $V_{CC}$ .

PIN DESCRIPTIONS (continued)

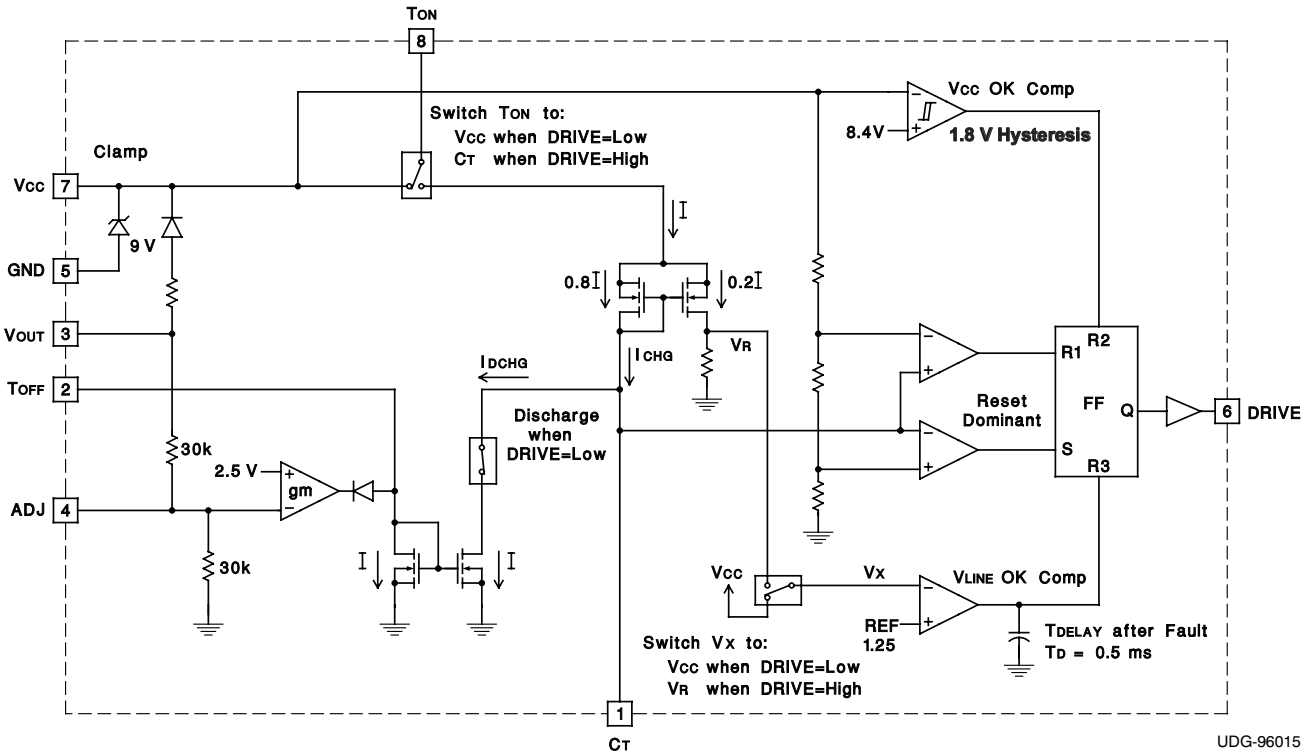
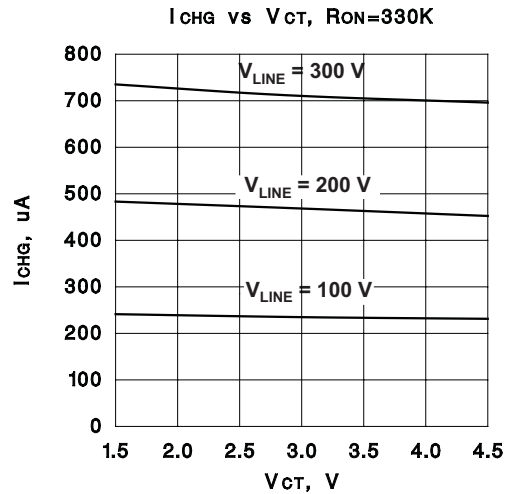
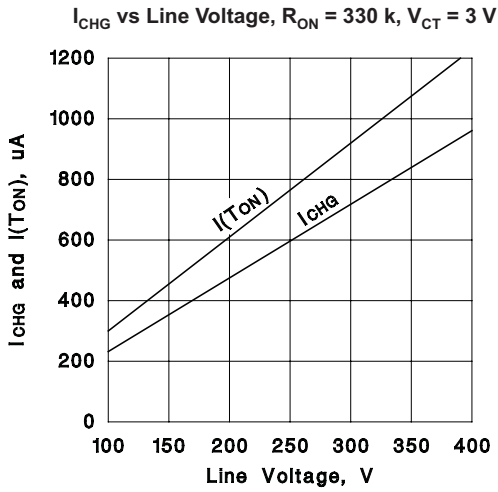


Figure 1. Block Diagram

TYPICAL CHARACTERISTICS



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
UCC2888D	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
UCC2888DG4	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
UCC3888D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
UCC3888DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
UCC3888N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	<a href="#">Request Free Samples</a>
UCC3888NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	<a href="#">Request Free Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

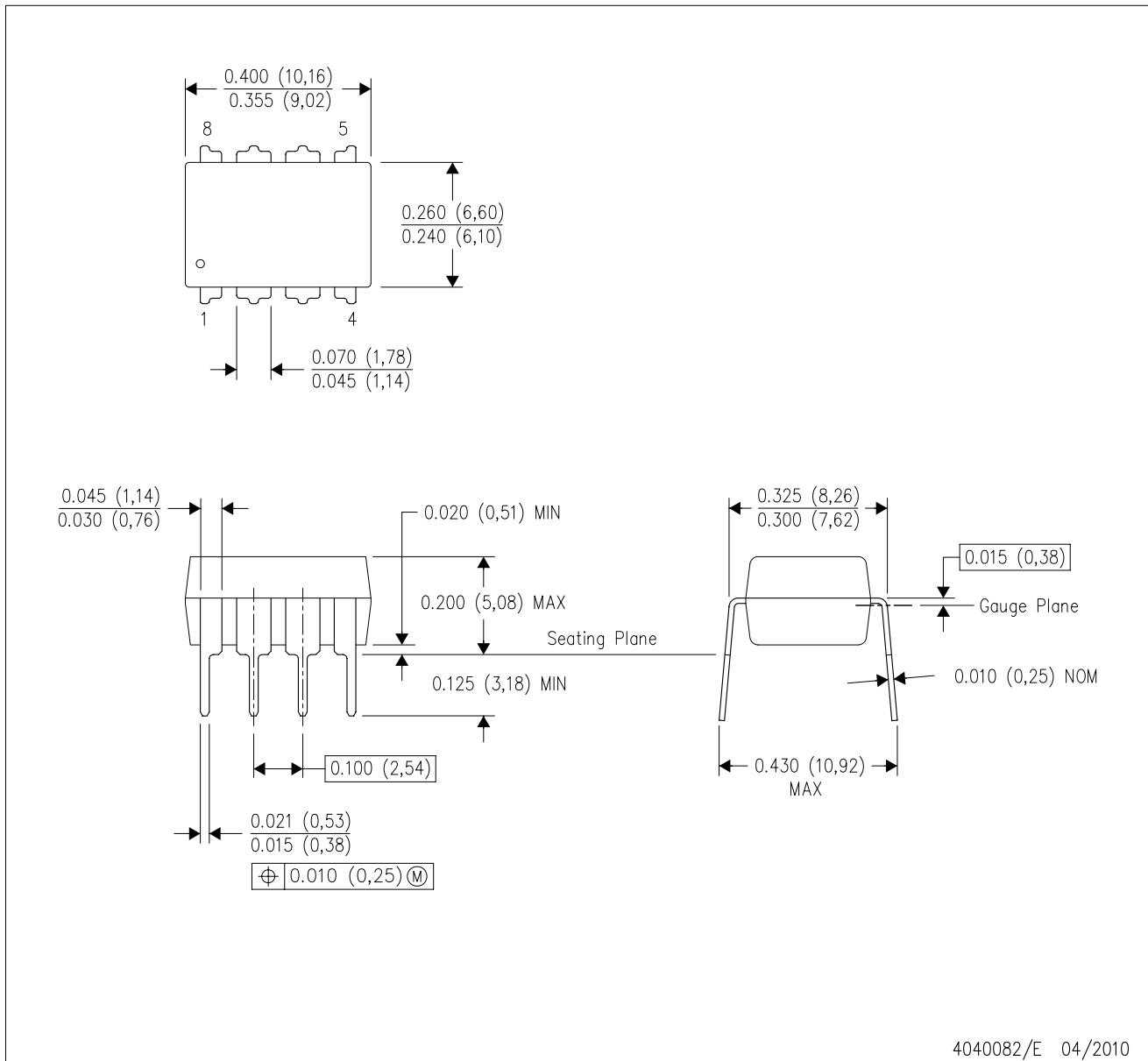
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

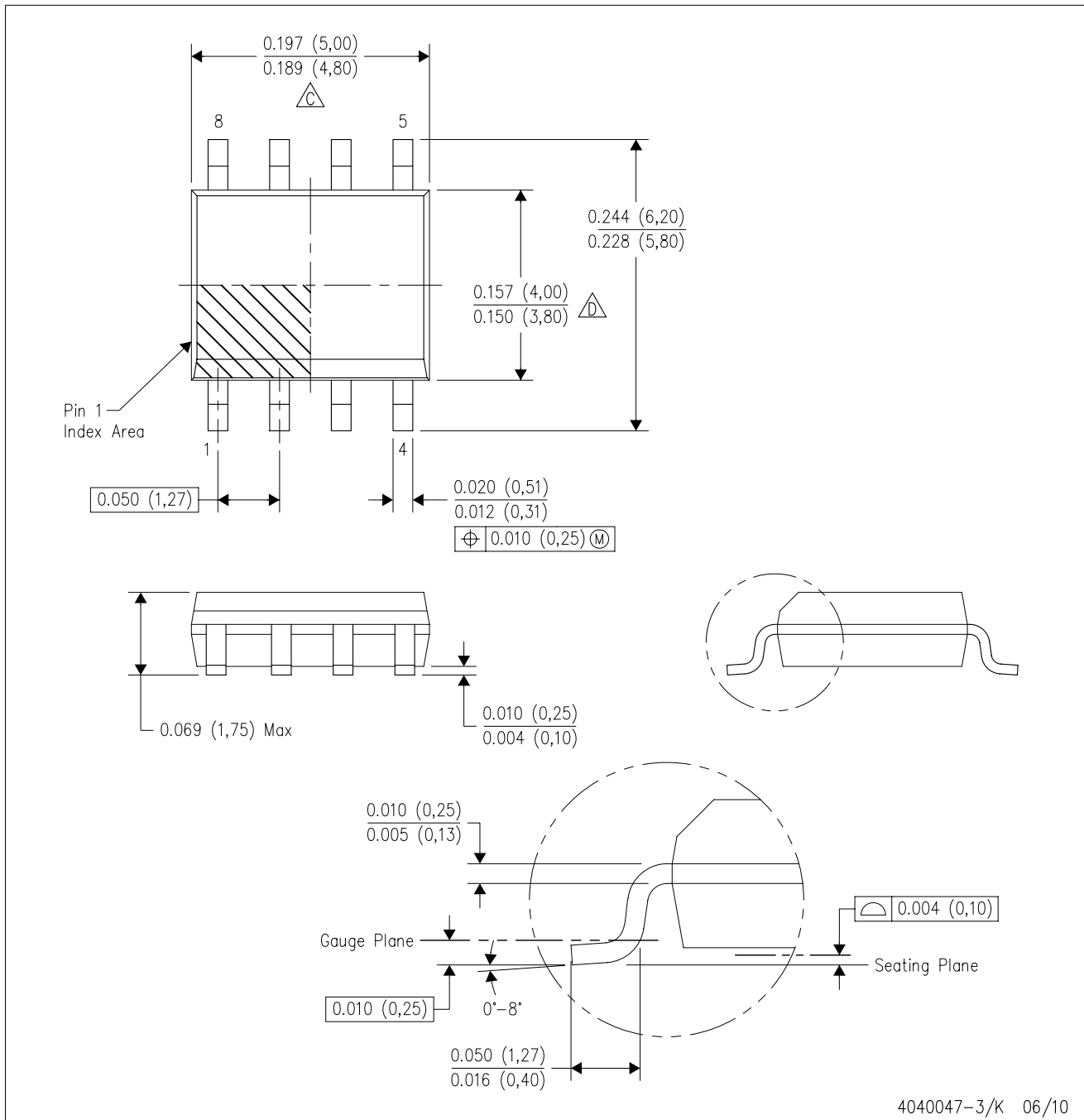
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
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  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

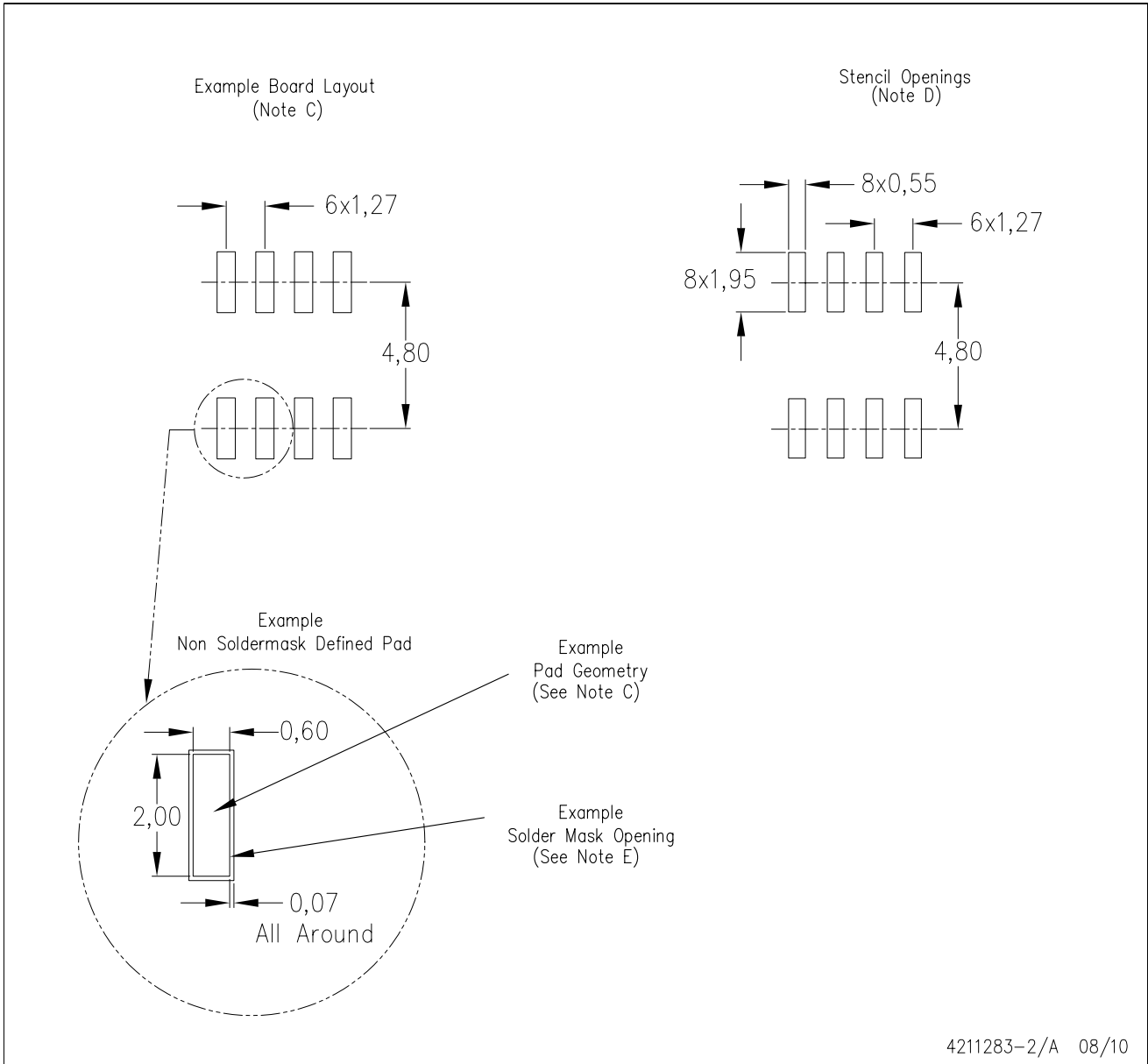
PLASTIC SMALL-OUTLINE PACKAGE



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  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
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