THE DATASHEET OF

AD9201ARSZRL

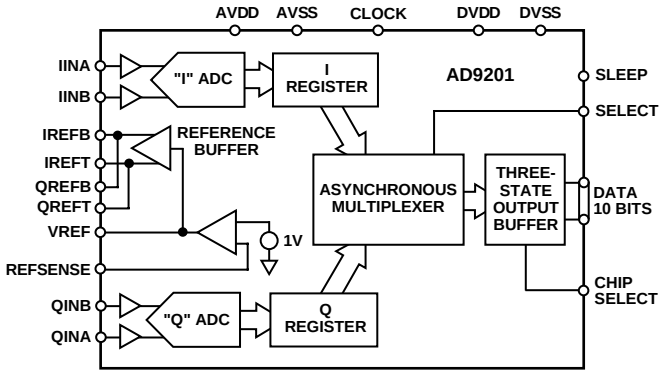
Dual Channel, 20 MHz 10-Bit Resolution CMOS ADC

AD9201

FEATURES

Complete Dual Matching ADCs
Low Power Dissipation: 215 mW (+3 V Supply)
Single Supply: 2.7 V to 5.5 V
Differential Nonlinearity Error: 0.4 LSB
On-Chip Analog Input Buffers
On-Chip Reference
Signal-to-Noise Ratio: 57.8 dB
Over Nine Effective Bits
Spurious-Free Dynamic Range: –73 dB
No Missing Codes Guaranteed
28-Lead SSOP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9201 is a complete dual channel, 20 MSPS, 10-bit CMOS ADC. The AD9201 is optimized specifically for applications where close matching between two ADCs is required (e.g., I/Q channels in communications applications). The 20 MHz sampling rate and wide input bandwidth will cover both narrowband and spread-spectrum channels. The AD9201 integrates two 10-bit, 20 MSPS ADCs, two input buffer amplifiers, an internal voltage reference and multiplexed digital output buffers.

Each ADC incorporates a simultaneous sampling sample-and-hold amplifier at its input. The analog inputs are buffered; no external input buffer op amp will be required in most applications. The ADCs are implemented using a multistage pipeline architecture that offers accurate performance and guarantees no missing codes. The outputs of the ADCs are ported to a multiplexed digital output buffer.

The AD9201 is manufactured on an advanced low cost CMOS process, operates from a single supply from 2.7 V to 5.5 V, and consumes 215 mW of power (on 3 V supply). The AD9201 input structure accepts either single-ended or differential signals, providing excellent dynamic performance up to and beyond its 10 MHz Nyquist input frequencies.

PRODUCT HIGHLIGHTS

1. Dual 10-Bit, 20 MSPS ADCs
   A pair of high performance 20 MSPS ADCs that are optimized for spurious free dynamic performance are provided for encoding of I and Q or diversity channel information.
2. Low Power
   Complete CMOS Dual ADC function consumes a low 215 mW on a single supply (on 3 V supply). The AD9201 operates on supply voltages from 2.7 V to 5.5 V.
3. On-Chip Voltage Reference
   The AD9201 includes an on-chip compensated bandgap voltage reference pin programmable for 1 V or 2 V.
4. On-chip analog input buffers eliminate the need for external op amps in most applications.
5. Single 10-Bit Digital Output Bus
   The AD9201 ADC outputs are interleaved onto a single output bus saving board space and digital pin count.
6. Small Package
   The AD9201 offers the complete integrated function in a compact 28-lead SSOP package.
7. Product Family
   The AD9201 dual ADC is pin compatible with a dual 8-bit ADC (AD9281) and has a companion dual DAC product, the AD9761 dual DAC.

REV. D

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AD9201–SPECIFICATIONS

(AVDD = +3 V, DVDD = +3 V, F_{SAMPLE} = 20 MSPS, VREF = 2 V, INB = 0.5 V, T_{MIN} to T_{MAX}, internal ref, differential input signal, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Condition
RESOLUTION			10		Bits	
CONVERSION RATE	F_S			20	MHz	
DC ACCURACY						
Differential Nonlinearity	DNL		±0.4		LSB	REFT = 1 V, REFB = 0 V
Integral Nonlinearity	INL		1.2		LSB	
Differential Nonlinearity (SE)	DNL		±0.5	±1	LSB	REFT = 1 V, REFB = 0 V
Integral Nonlinearity (SE)	INL		±1.5	±2.5	LSB	
Zero-Scale Error, Offset Error	E_{ZS}		±1.5	±3.8	% FS	
Full-Scale Error, Gain Error	E_{FS}		±3.5	±5.4	% FS	
Gain Match			±0.5		LSB	
Offset Match			±5		LSB	
ANALOG INPUT						
Input Voltage Range	AIN	–0.5		AVDD/2	V	
Input Capacitance	C_{IN}		2		pF	
Aperture Delay	t_{AP}		4		ns	
Aperture Uncertainty (Jitter)	t_{AJ}		2		ps	
Aperture Delay Match			2		ps	
Input Bandwidth (–3 dB)	BW					
Small Signal (–20 dB)			240		MHz	
Full Power (0 dB)			245		MHz	
INTERNAL REFERENCE						
Output Voltage (1 V Mode)	VREF		1		V	REFSENSE = VREF
Output Voltage Tolerance (1 V Mode)			±10		mV	
Output Voltage (2 V Mode)	VREF		2		V	REFSENSE = GND
Output Voltage Tolerance (2 V Mode)			±15		mV	
Load Regulation (1 V Mode)				±28	mV	1 mA Load Current
Load Regulation (2 V Mode)			±15		mV	1 mA Load Current
POWER SUPPLY						
Operating Voltage	AVDD	2.7	3	5.5	V	AVDD – DVDD ≤ 2.3 V
	DRVDD	2.7	3	5.5	V	
Supply Current	I_{AVDD}		71.6		mA	AVDD = 3 V
	I_{DRVDD}		0.1		mA	
Power Consumption	P_D		215	245	mW	AVDD = DVDD = 3 V
Power-Down			15.5		mW	STBY = AVDD, Clock = AVSS
Power Supply Rejection	PSR		0.8	1.3	% FS	
DYNAMIC PERFORMANCE[1]						
Signal-to-Noise and Distortion	SINAD					
f = 3.58 MHz		55.6	57.3		dB	
f = 10 MHz			55.8		dB	
Signal-to-Noise	SNR					
f = 3.58 MHz		55.9	57.8		dB	
f = 10 MHz			56.2		dB	
Total Harmonic Distortion	THD					
f = 3.58 MHz			–69	–63.3	dB	
f = 10 MHz			–66.3		dB	
Spurious Free Dynamic Range	SFDR					
f = 3.58 MHz		–66	–73		dB	
f = 10 MHz			–70.5		dB	
Two-Tone Intermodulation Distortion[2]	IMD		–62		dB	f = 44.49 MHz and 45.52 MHz
Differential Phase	DP		0.1		Degree	NTSC 40 IRE Mod Ramp
Differential Gain	DG		0.05		%	F_S = 14.3 MHz
Crosstalk Rejection			68		dB	

Parameter	Symbol	Min	Typ	Max	Units	Condition
DYNAMIC PERFORMANCE (SE)[3]						
Signal-to-Noise and Distortion	SINAD					
f = 3.58 MHz			52.3		dB	
Signal-to-Noise	SNR					
f = 3.58 MHz			55.5		dB	
Total Harmonic Distortion	THD					
f = 3.58 MHz			–55		dB	
Spurious Free Dynamic Range	SFDR					
f = 3.58 MHz			–58		dB	
DIGITAL INPUTS						
High Input Voltage	V_{IH}	2.4			V	
Low Input Voltage	V_{IL}			0.3	V	
DC Leakage Current	I_{IN}		±6		µA	
Input Capacitance	C_{IN}		2		pF	
LOGIC OUTPUT (with DVDD = 3 V)						
High Level Output Voltage						
(I_{OH} = 50 µA)	V_{OH}		2.88		V	
Low Level Output Voltage						
(I_{OL} = 1.5 mA)	V_{OL}		0.095		V	
LOGIC OUTPUT (with DVDD = 5 V)						
High Level Output Voltage						
(I_{OH} = 50 µA)	V_{OH}		4.5		V	
Low Level Output Voltage						
(I_{OL} = 1.5 mA)	V_{OL}		0.4		V	
Data Valid Delay	t_{OD}		11		ns	
MUX Select Delay	t_{MD}		7		ns	
Data Enable Delay	t_{ED}		13		ns	C_L = 20 pF. Output Level to 90% of Final Value
Data High-Z Delay	t_{DHZ}		13		ns	
CLOCKING						
Clock Pulsewidth High	t_{CH}	22.5			ns	
Clock Pulsewidth Low	t_{CL}	22.5			ns	
Pipeline Latency			3.0		Cycles	

NOTES
[1]AIN differential 2 V p-p, REFT = 1.5 V, REFB = –0.5 V.
[2]IMD referred to larger of two input signals.
[3]SE is single ended input, REFT = 1.5 V, REFB = –0.5 V.
Specifications subject to change without notice.

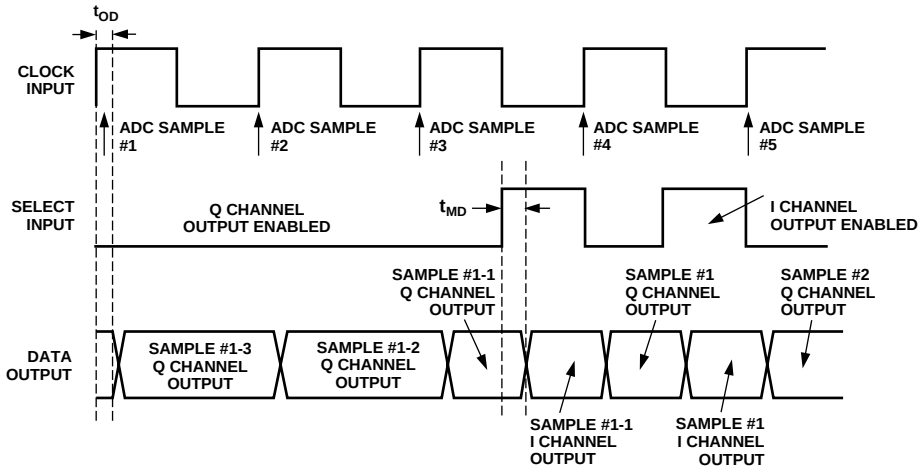


Figure 1. ADC Timing

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
AINA, AINB	AVSS	–1.0	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
REFSENSE	AVSS	–0.3	AVDD + 0.3	V
REFT, REFB	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature 10 sec			+300	°C

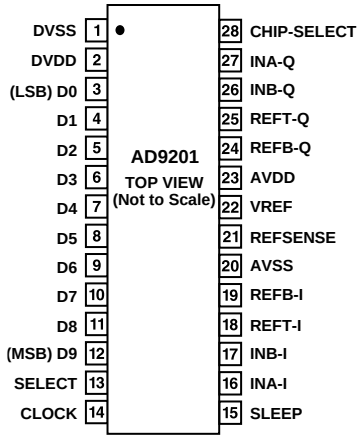
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9201ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9201-EVAL		Evaluation Board	

*RS = Shrink Small Outline.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DVSS	Digital Ground
2	DVDD	Digital Supply
3	D0	Bit 0 (LSB)
4	D1	Bit 1
5	D2	Bit 2
6	D3	Bit 3
7	D4	Bit 4
8	D5	Bit 5
9	D6	Bit 6
10	D7	Bit 7
11	D8	Bit 8
12	D9	Bit 9 (MSB)
13	SELECT	Hi I Channel Out, Lo Q Channel Out
14	CLOCK	Clock
15	SLEEP	Hi Power Down, Lo Normal Operation
16	INA-I	I Channel, A Input
17	INB-I	I Channel, B Input
18	REFT-I	Top Reference Decoupling, I Channel
19	REFB-I	Bottom Reference Decoupling, I Channel
20	AVSS	Analog Ground
21	REFSENSE	Reference Select
22	VREF	Internal Reference Output
23	AVDD	Analog Supply
24	REFB-Q	Bottom Reference Decoupling, Q Channel
25	REFT-Q	Top Reference Decoupling, Q Channel
26	INB-Q	Q Channel, B Input
27	INA-Q	Q Channel, A Input
28	CHIP-SELECT	Hi-High Impedance, Lo-Normal Operation

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

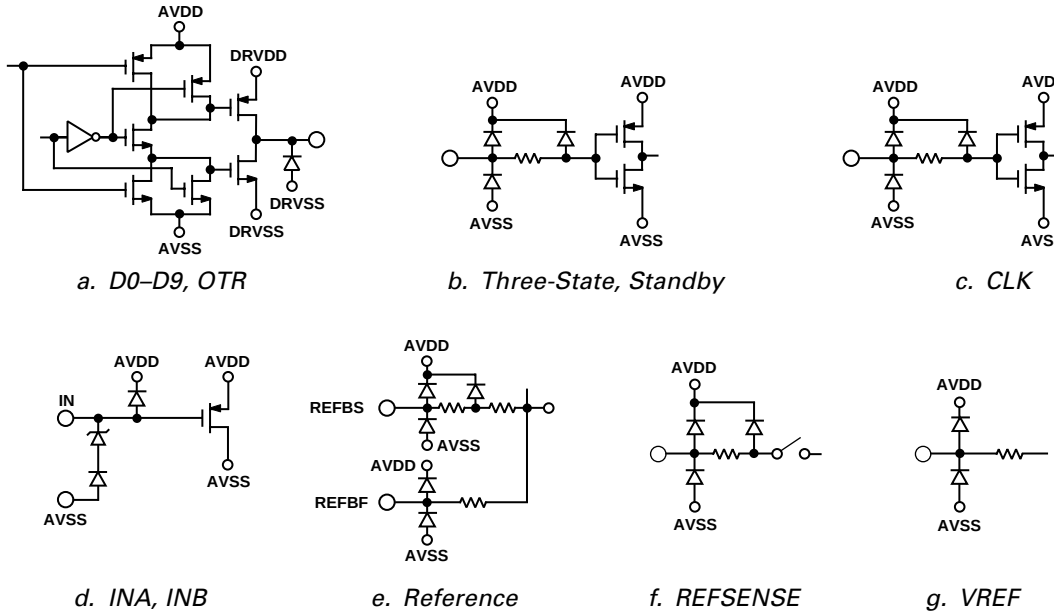
Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSBs beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) are guaranteed.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9201 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



a. D0–D9, OTR *b. Three-State, Standby* *c. CLK*

d. INA, INB *e. Reference* *f. REFSENSE* *g. VREF*

Figure 2. Equivalent Circuits

OFFSET ERROR
The first transition should occur at a level 1 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

OFFSET MATCH
The change in offset error between I and Q channels.

EFFECTIVE NUMBER OF BITS (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

It is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)
The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

GAIN ERROR
The first code transition should occur for an analog value 1 LSB above nominal negative full scale. The last transition should occur for an analog value 1 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

GAIN MATCH
The change in gain error between I and Q channels.

PIPELINE DELAY (LATENCY)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every rising clock edge.

MUX SELECT DELAY
The delay between the change in SELECT pin data level and valid data on output pins.

POWER SUPPLY REJECTION
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY
Aperture delay is a measure of the Sample-and-Hold Amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

AD9201–Typical Characteristic Curves

(AVDD = +3 V, DVDD = +3 V, F_S = 20 MHz (50% duty cycle), 2 V input span from –0.5 V to +1.5 V, 2 V internal reference unless otherwise noted)

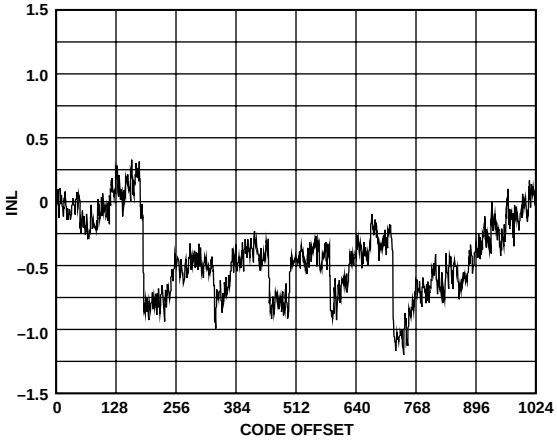


Figure 3. Typical INL (1 V Internal Reference)

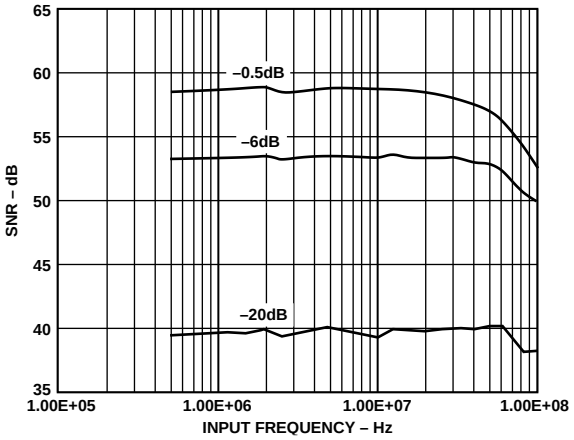


Figure 6. SNR vs. Input Frequency

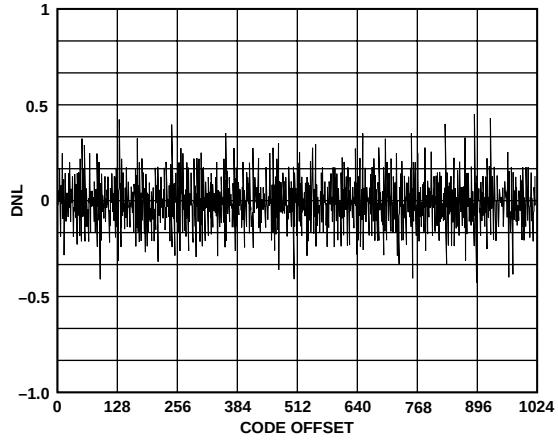


Figure 4. Typical DNL (1 V Internal Reference)

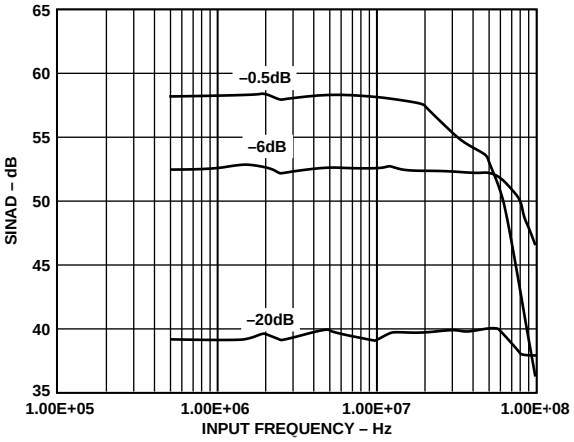


Figure 7. SINAD vs. Input Frequency

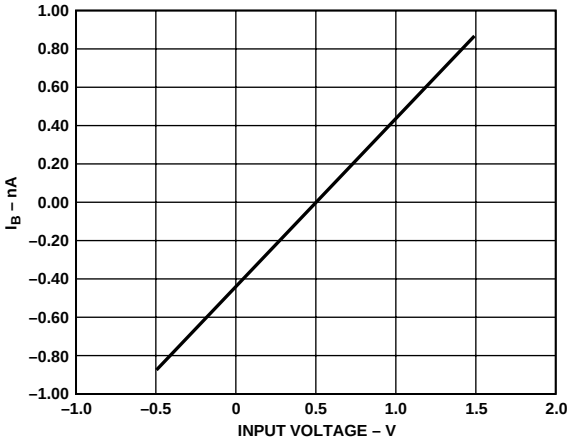


Figure 5. Input Bias Current vs. Input Voltage

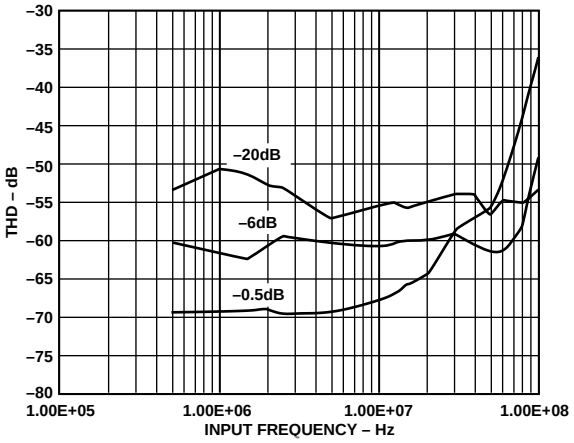


Figure 8. THD vs. Input Frequency

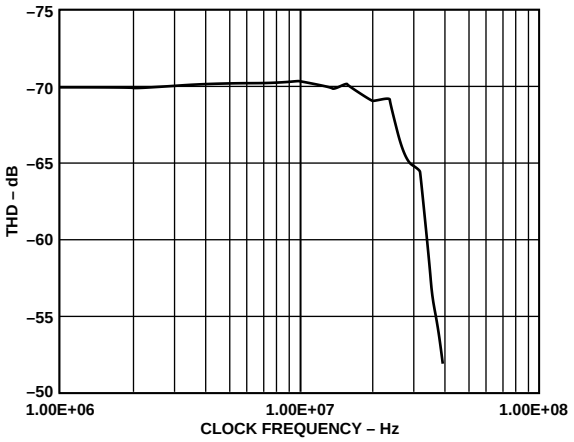


Figure 9. THD vs. Clock Frequency (f_{IN} = 1 MHz)

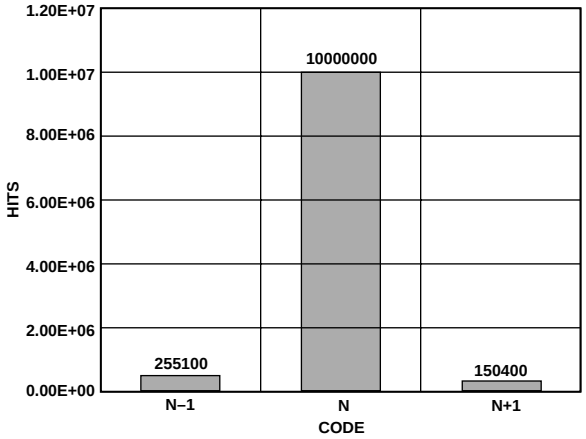


Figure 12. Grounded Input Histogram

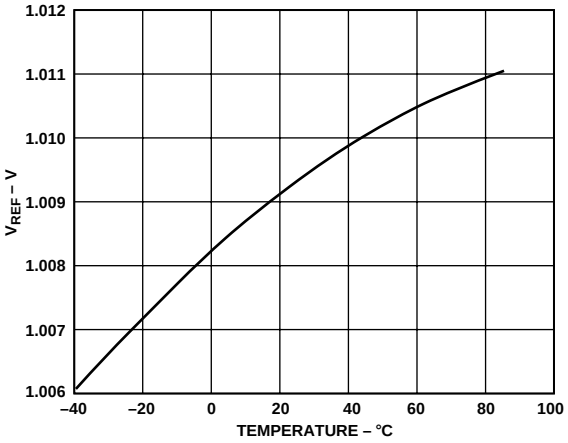


Figure 10. Voltage Reference Error vs. Temperature

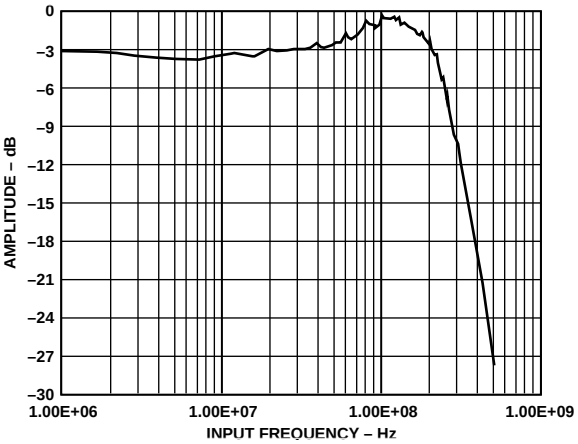


Figure 13. Full Power Bandwidth

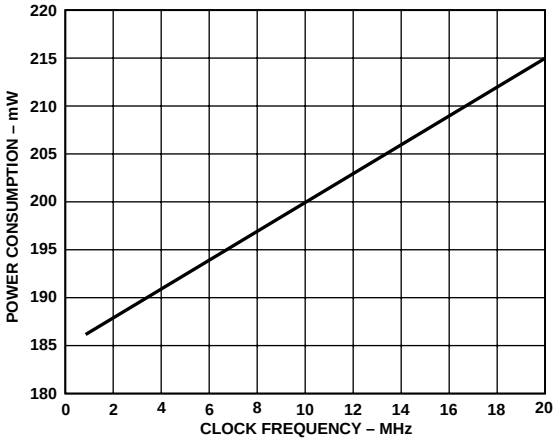


Figure 11. Power Consumption vs. Clock Frequency

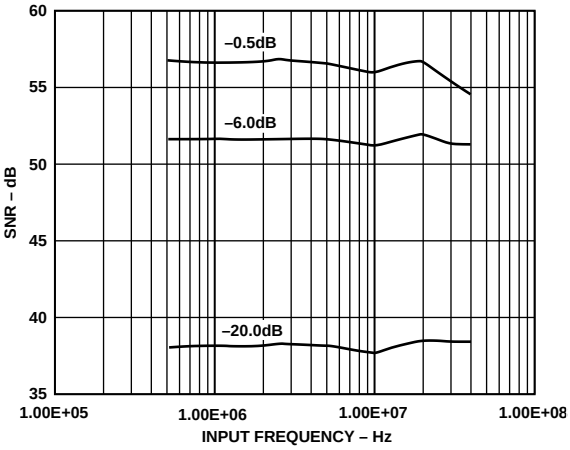


Figure 14. SNR vs. Input Frequency (Single Ended)

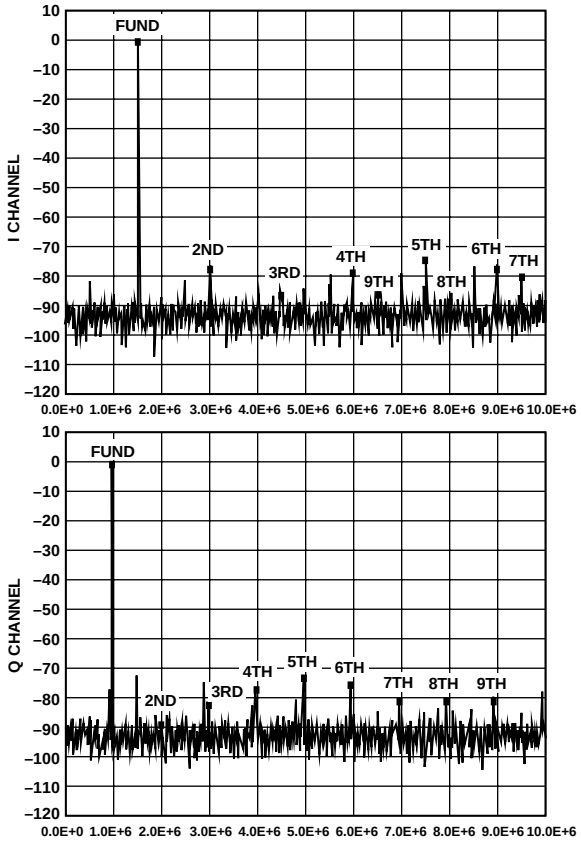


Figure 15. Simultaneous Operation of I and Q Channels (Differential Input)

THEORY OF OPERATION

The AD9201 integrates two A/D converters, two analog input buffers, an internal reference and reference buffer, and an output multiplexer. For clarity, this data sheet refers to the two converters as "I" and "Q." The two A/D converters simultaneously sample their respective inputs on the rising edge of the input clock. The two converters distribute the conversion operation over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the result from stage to stage. As a consequence of the distributed conversion, each converter requires a small fraction of the 1023 comparators used in a traditional flash-type 10-bit ADC. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the following stages continue to process previous samples. This results in a "pipeline processing" latency of three clock periods between when an input sample is taken and when the corresponding ADC output is updated into the output registers.

The AD9201 integrates input buffer amplifiers to drive the analog inputs of the converters. In most applications, these input amplifiers eliminate the need for external op amps for the input signals. The input structure is fully differential, but the SHA common-mode response has been designed to allow the converter to readily accommodate either single-ended or differential input signals. This differential structure makes the part capable of accommodating a wide range of input signals.

The AD9201 also includes an on-chip bandgap reference and reference buffer. The reference buffer shifts the ground-referred reference to levels more suitable for use by the internal circuits of the converter. Both converters share the same reference and reference buffer. This scheme provides for the best possible gain match between the converters while simultaneously minimizing the channel-to-channel crosstalk. (See Figure 16.)

Each A/D converter has its own output latch, which updates on the rising edge of the input clock. A logic multiplexer, controlled through the SELECT pin, determines which channel is passed to the digital output pins. The output drivers have their own supply (DVDD), allowing the part to be interfaced to a variety of logic families. The outputs can be placed in a high impedance state using the CHIP SELECT pin.

The AD9201 has great flexibility in its supply voltage. The analog and digital supplies may be operated from 2.7 V to 5.5 V, independently of one another.

ANALOG INPUT

Figure 16 shows an equivalent circuit structure for the analog input of one of the A/D converters. PMOS source-followers buffer the analog input pins from the charge kickback problems normally associated with switched capacitor ADC input structures. This produces a very high input impedance on the part, allowing it to be effectively driven from high impedance sources. This means that the AD9201 could even be driven directly by a passive antialias filter.

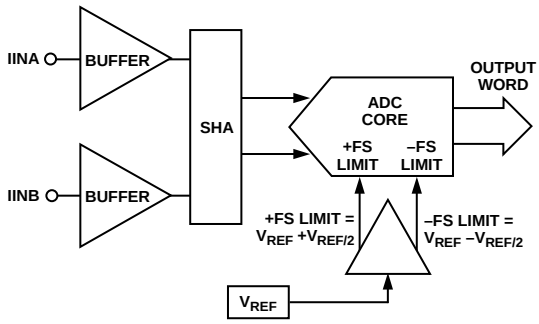


Figure 16. Equivalent Circuit for AD9201 Analog Inputs

The source followers inside the buffers also provide a level-shift function of approximately 1 V, allowing the AD9201 to accept inputs at or below ground. One consequence of this structure is that distortion will result if the analog input approaches the positive supply. For optimum high frequency distortion performance, the analog input signal should be centered according to Figure 29.

The capacitance load of the analog input Pin is 4 pF to the analog supplies (AVSS, AVDD).

Full-scale setpoints may be calculated according to the following algorithm (V_{REF} may be internally or externally generated):

$-F_S = (V_{REF} - V_{REF}/2)$
$+F_S = (V_{REF} + V_{REF}/2)$
$V_{SPAN} = V_{REF}$

The AD9201 can accommodate a variety of input spans between 1 V and 2 V. For spans of less than 1 V, expect a proportionate degradation in SNR . Use of a 2 V span will provide the best noise performance. 1 V spans will provide lower distortion when using a 3 V analog supply. Users wishing to run with larger full-scales are encouraged to use a 5 V analog supply (AVDD).

Single-Ended Inputs: For single-ended input signals, the signal is applied to one input pin and the other input pin is tied to a midscale voltage. This midscale voltage defines the center of the full-scale span for the input signal.

EXAMPLE: For a single-ended input range from 0 V to 1 V applied to IINA, we would configure the converter for a 1 V reference (See Figure 17) and apply 0.5 V to IINB.

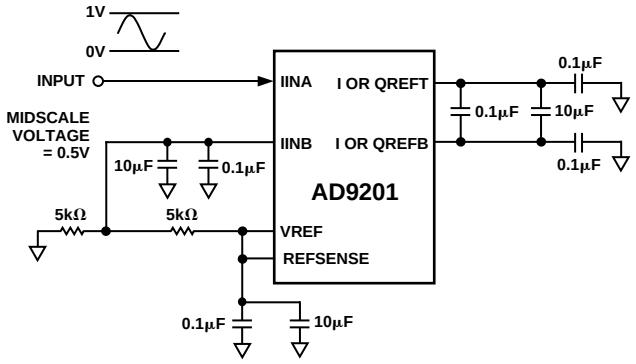


Figure 17. Example Configuration for 0 V–1 V Single-Ended Input Signal

Note that since the inputs are high impedance, this reference level can easily be generated with an external resistive divider with large resistance values (to minimize power dissipation). A decoupling capacitor is recommended on this input to minimize the high frequency noise-coupling onto this pin. Decoupling should occur close to the ADC.

Differential Inputs

Use of differential input signals can provide greater flexibility in input ranges and bias points, as well as offering improvements in distortion performance, particularly for high frequency input signals. Users with differential input signals will probably want to take advantage of the differential input structure.

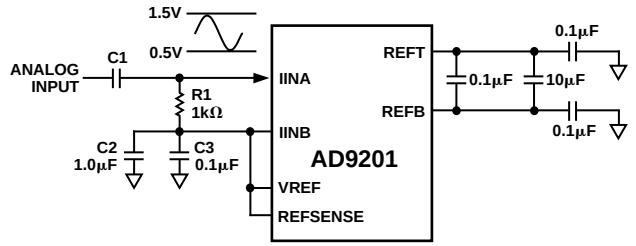


Figure 18. Example Configuration for 0.5 V–1.5 V ac Coupled Single-Ended Inputs

AC Coupled Inputs

If the signal of interest has no dc component, ac coupling can be easily used to define an optimum bias point. Figure 18 illustrates one recommended configuration. The voltage chosen for the dc bias point (in this case the 1 V reference) is applied to both IINA and IINB pins through 1 kΩ resistors (R1 and R2). IINA is coupled to the input signal through Capacitor C1, while IINB is decoupled to ground through Capacitor C2 and C3.

Transformer Coupled Inputs

Another option for input ac coupling is to use a transformer. This not only provides dc rejection, but also allows truly differential drive of the AD9201's analog inputs, which will provide the optimal distortion performance. Figure 19 shows a recommended transformer input drive configuration. Resistors R1 and R2 define the termination impedance of the transformer coupling. The center tap of the transformer secondary is tied to the common-mode reference, establishing the dc bias point for the analog inputs.

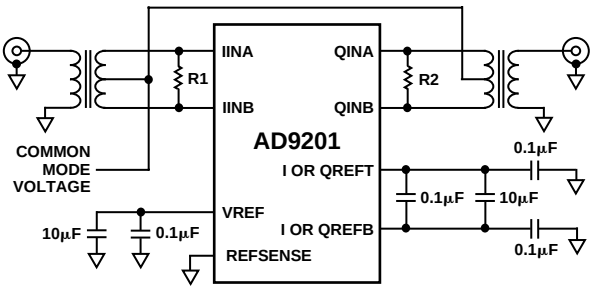


Figure 19. Example Configuration for Transformer Coupled Inputs

Crosstalk: The internal layout of the AD9201, as well as its pinout, was configured to minimize the crosstalk between the two input signals. Users wishing to minimize high frequency crosstalk should take care to provide the best possible decoupling for input pins (see Figure 20). R and C values will make a pole dependant on antialiasing requirements. Decoupling is also required on reference pins and power supplies (see Figure 21).

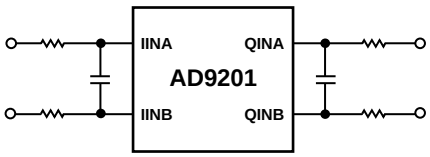


Figure 20. Input Loading

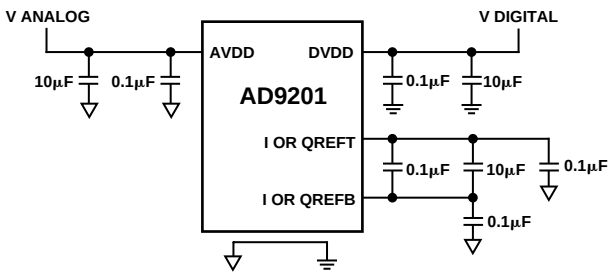


Figure 21. Reference and Power Supply Decoupling

REFERENCE AND REFERENCE BUFFER

The reference and buffer circuitry on the AD9201 is configured for maximum convenience and flexibility. An illustration of the equivalent reference circuit is show in Figure 26. The user can select from five different reference modes through appropriate pin-strapping (see Table I below). These pin strapping options cause the internal circuitry to reconfigure itself for the appropriate operating mode.

Table I. Table of Modes

Mode	Input Span	REFSENSE Pin	Figure
1 V	1 V	VREF	22
2 V	2 V	AGND	23
Programmable	1 + (R1/R2)	See Figure	24
External	= External Ref	AVDD	25

1 V Mode (Figure 22)—provides a 1 V reference and 1 V input full scale. Recommended for applications wishing to optimize high frequency performance, or any circuit on a supply voltage of less than 4 V. The part is placed in this mode by shorting the REFSENSE pin to the VREF pin.

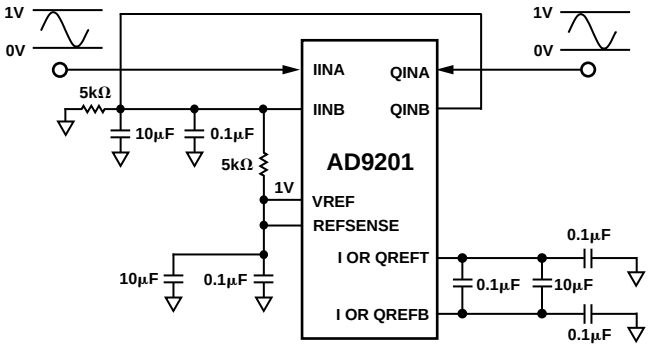


Figure 22. 0 V to 1 V Input

2 V Mode (Figure 23)—provides a 2 V reference and 2 V input full scale. Recommended for noise sensitive applications on 5 V supplies. The part is placed in 2 V reference mode by grounding (shorting to AVSS) the REFSENSE pin.

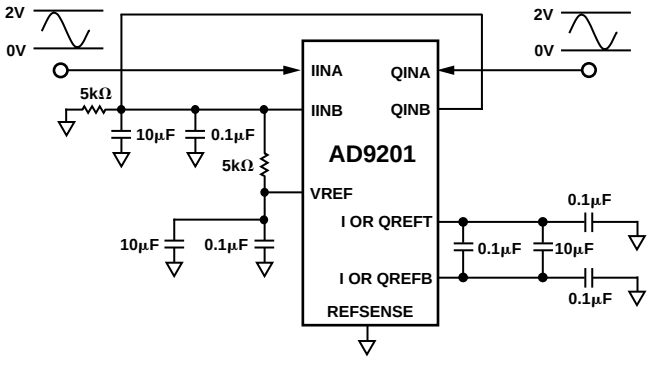


Figure 23. 0 V to 2 V Input

Externally Set Voltage Mode (Figure 24)—this mode uses the on-chip reference, but scales the exact reference level though the use of an external resistor divider network. VREF is wired to the top of the network, with the REFSENSE wired to the tap point in the resistor divider. The reference level (and input full scale) will be equal to 1 V × (R1 + R2)/R1. This method can be used for voltage levels from 0.7 V to 2.5 V.

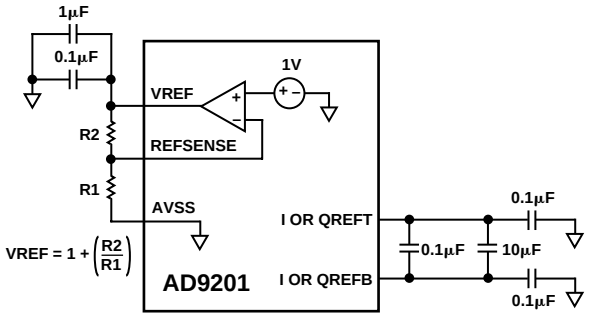


Figure 24. Programmable Reference

External Reference Mode (Figure 25)—in this mode, the on-chip reference is disabled, and an external reference is applied to the VREF pin. This mode is achieved by tying the REFSENSE pin to AVDD.

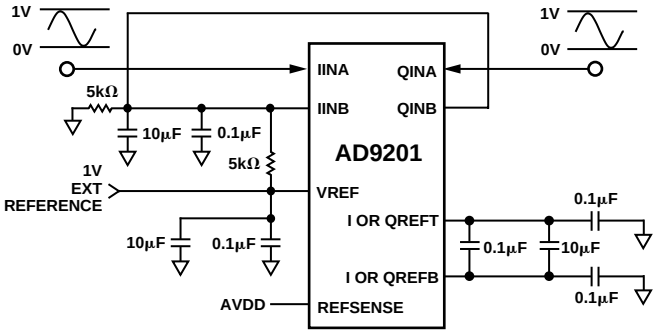


Figure 25. External Reference

Reference Buffer—The reference buffer structure takes the voltage on the VREF pin and level-shifts and buffers it for use by various subblocks within the two A/D converters. The two converters share the same reference buffer amplifier to maintain the best possible gain match between the two converters. In the interests of minimizing high frequency crosstalk, the buffered references for the two converters are separately decoupled on the IREFB, IREFT, QREFB and QREFT pins, as illustrated in Figure 26.

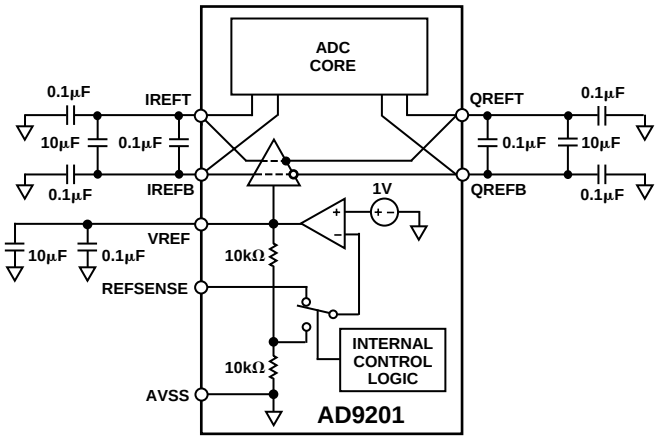


Figure 26. Reference Buffer Equivalent Circuit and External Decoupling Recommendation

For best results in both noise suppression and robustness against crosstalk, the 4 capacitor buffer decoupling arrangement shown in Figure 26 is recommended. This decoupling should feature chip capacitors located close to the converter IC. The capacitors are connected to either IREFT/IREFB or QREFT/QREFB. A connection to both sides is not required.

DRIVING THE AD9201

Figure 27 illustrates the use of an AD8051 to drive the AD9201. Even though the AD8051 is specified with 3 V and 5 V power, the best results are obtained at ±5 V power. The ADC input span is 2 V.

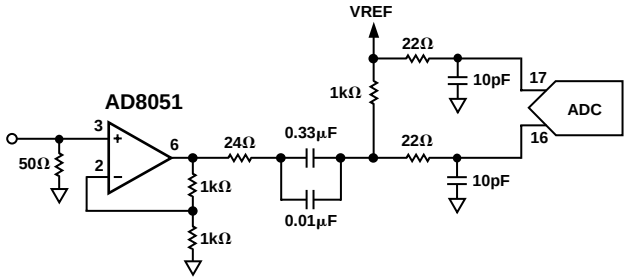


Figure 27.

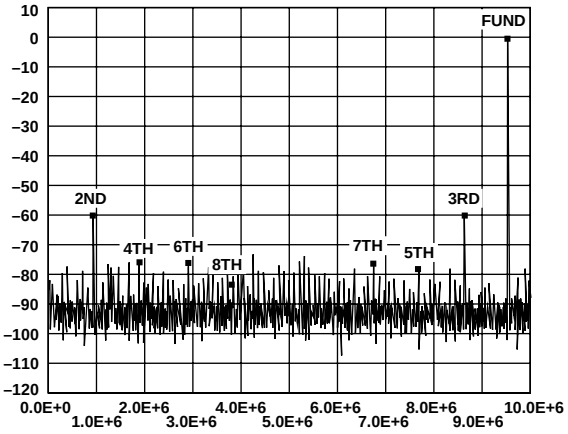


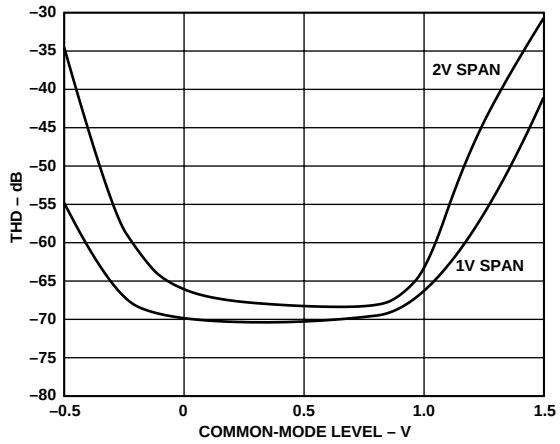
Figure 28. AD8051/AD9201 Performance

COMMON-MODE PERFORMANCE

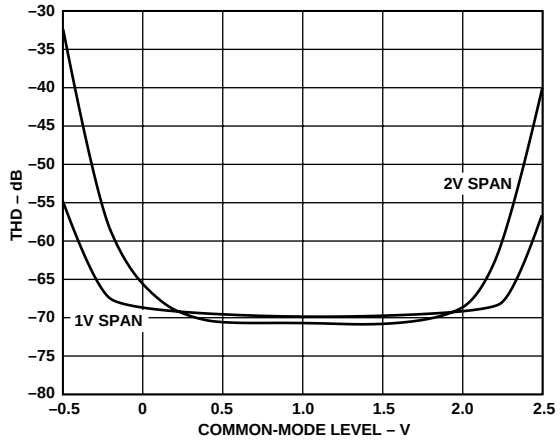
Attention to the common-mode point of the analog input voltage can improve the performance of the AD9201. Figure 29 illustrates THD as a function of common-mode voltage (center point of the analog input span) and power supply.

Inspection of the curves will yield the following conclusions:

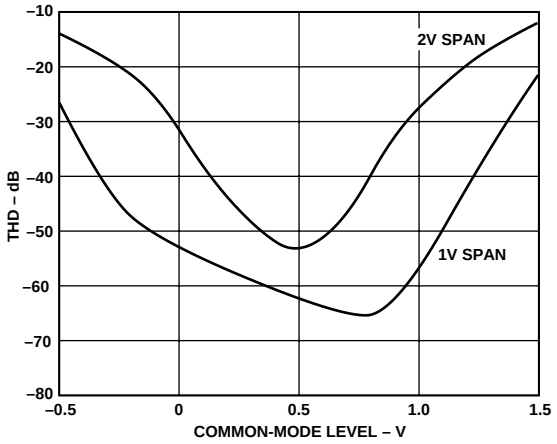
1. An AD9201 running with AVDD = 5 V is the easiest to drive.
2. Differential inputs are the most insensitive to common-mode voltage.
3. An AD9201 powered by AVDD = 3 V and a single ended input, should have a 1 V span with a common-mode voltage of 0.75 V.



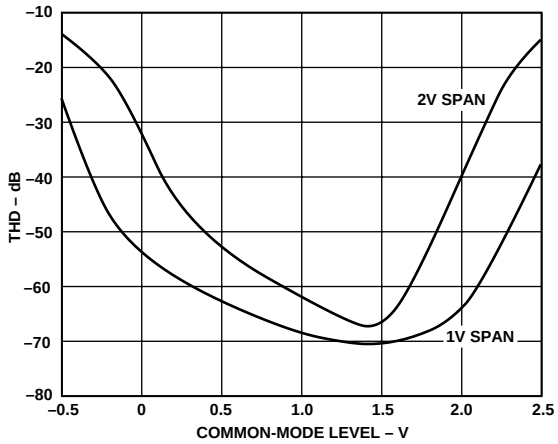
a. Differential Input, 3 V Supplies



b. Differential Input, 5 V Supplies



c. Single-Ended Input, 3 V Supplies



d. Single-Ended Input, 5 V Supplies

Figure 29. THD vs. CML Input Span and Power Supply (Analog Input = 1 MHz)

DIGITAL INPUTS AND OUTPUTS

Each of the AD9201 digital control inputs, CHIP SELECT, CLOCK, SELECT and SLEEP are referenced to AVDD and AVSS. Switching thresholds will be AVDD/2.

The format of the digital output is straight binary. A low power mode feature is provided such that for STBY = HIGH and the clock disabled, the static power of the AD9201 will drop below 22 mW.

CLOCK INPUT

The AD9201 clock input is internally buffered with an inverter powered from the AVDD pin. This feature allows the AD9201 to accommodate either +5 V or +3.3 V CMOS logic input signal swings with the input threshold for the CLK pin nominally at AVDD/2.

The pipelined architecture of the AD9201 operates on both rising and falling edges of the input clock. To minimize duty cycle variations the logic family recommended to drive the clock input is high speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 20 MSPS operation. Running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD9201 at slower clock rates.

The power dissipated by the output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a reduction in power consumption.

DIGITAL OUTPUTS

Each of the on-chip buffers for the AD9201 output bits (D0–D9) is powered from the DVDD supply pin, separate from AVDD. The output drivers are sized to handle a variety of logic families while minimizing the amount of glitch energy generated. In all cases, a fan-out of one is recommended to keep the capacitive load on the output data bits below the specified 20 pF level.

For DVDD = 5 V, the AD9201 output signal swing is compatible with both high speed CMOS and TTL logic families. For TTL, the AD9201 on-chip, output drivers were designed to support several of the high speed TTL families (F, AS, S). For applications where the clock rate is below 20 MSPS, other TTL families may be appropriate. For interfacing with lower voltage CMOS logic, the AD9201 sustains 20 MSPS operation with DVDD = 3 V. In all cases, check your logic family data sheets for compatibility with the AD9201's Specification table.

A 2 ns reduction in output delays can be achieved by limiting the logic load to 5 pF per output line.

THREE-STATE OUTPUTS

The digital outputs of the AD9201 can be placed in a high impedance state by setting the CHIP SELECT pin to HIGH. This feature is provided to facilitate in-circuit testing or evaluation.

SELECT

When the select pin is held LOW, the output word will present the "Q" level. When the select pin is held HIGH, the "I" level will be presented to the output word (see Figure 1).

The AD9201's select and clock pins may be driven by a common signal source. The data will change in 5 ns to 11 ns after the edges of the input pulse. The user must make sure the interface latches have sufficient hold time for the AD9201's delays (see Figure 30).

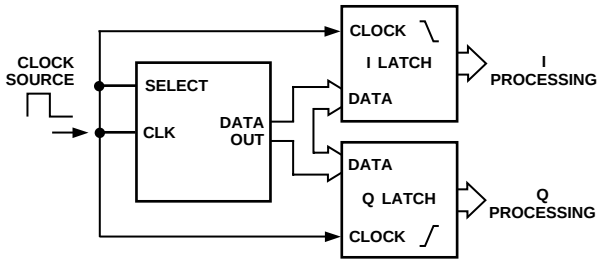


Figure 30. Typical De-Mux Connection

APPLICATIONS

USING THE AD9201 FOR QAM DEMODULATION

QAM is one of the most widely used digital modulation schemes in digital communication systems. This modulation technique can be found in both FDMA as well as spread spectrum (i.e., CDMA) based systems. A QAM signal is a carrier frequency which is both modulated in amplitude (i.e., AM modulation) and in phase (i.e., PM modulation). At the transmitter, it can be generated by independently modulating two carriers of identical frequency but with a 90° phase difference. This results in an inphase (I) carrier component and a quadrature (Q) carrier component at a 90° phase shift with respect to the I component. The I and Q components are then summed to provide a QAM signal at the specified carrier or IF frequency. Figure 31 shows a typical analog implementation of a QAM modulator using a dual 10-bit DAC with 2× interpolation, the AD9761. A QAM signal can also be synthesized in the digital domain thus requiring a single DAC to reconstruct the QAM signal. The AD9853 is an example of a complete (i.e., DAC included) digital QAM modulator.

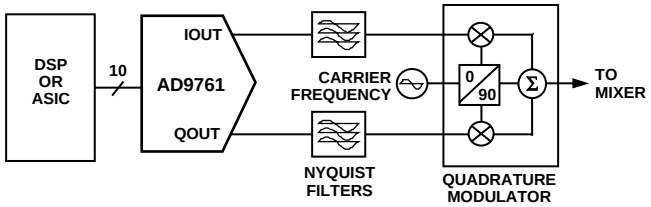


Figure 31. Typical Analog QAM Modulator Architecture

At the receiver, the demodulation of a QAM signal back into its separate I and Q components is essentially the modulation process explain above but in the reverse order. A common and traditional implementation of a QAM demodulator is shown in Figure 32. In this example, the demodulation is performed in the analog domain using a dual, matched ADC and a quadrature demodulator to recover and digitize the I and Q baseband signals. The quadrature demodulator is typically a single IC containing two mixers and the appropriate circuitry to generate the necessary 90° phase shift between the I and Q mixers' local oscillators. Before being digitized by the ADCs, the mixed down baseband I and Q signals are filtered using matched analog filters. These filters, often referred to as Nyquist or Pulse-Shaping filters, remove images-from the mixing process and any out-of-band. The characteristics of the matching Nyquist filters are well defined to provide optimum signal-to-noise (SNR) performance while minimizing intersymbol interference. The ADC's are typically simultaneously sampling their respective inputs at the QAM symbol rate or, most often, at a multiple of it if a digital filter follows the ADC. Oversampling and the use of digital filtering eases the implementation and complexity of the analog filter. It also allows for enhanced digital processing for both carrier and symbol recovery and tuning purposes. The use of a dual ADC such as the AD9201 ensures excellent gain, offset, and phase matching between the I and Q channels.

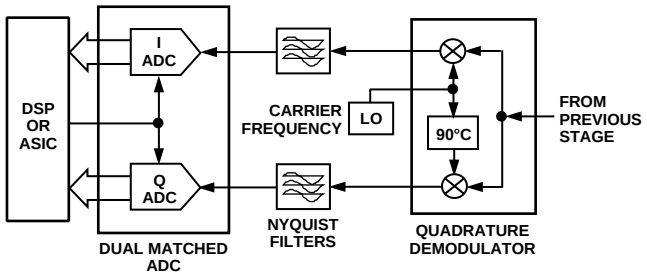


Figure 32. Typical Analog QAM Demodulator

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD9201 have been separated to optimize the management of return currents in a system. Grounds should be connected near the ADC. It is recommended that a printed circuit board (PCB) of at least four layers, employing a ground plane and power planes, be used with the AD9201. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. Separate analog and digital grounds should be joined together directly under the AD9201 in a solid ground plane. The power and ground return currents must be carefully managed. A general rule of thumb for mixed signal layouts dictates that the return currents from digital circuitry should not pass through critical analog circuitry.

Transients between AVSS and DVSS will seriously degrade performance of the ADC.

If the user cannot tie analog ground and digital ground together at the ADC, he should consider the configuration in Figure 33.

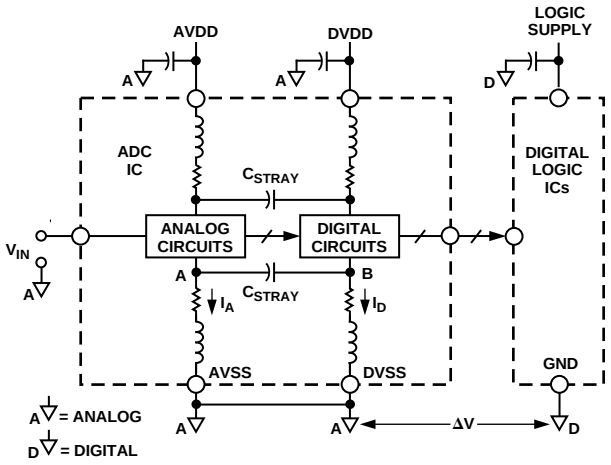


Figure 33. Ground and Power Consideration

Another input and ground technique is shown in Figure 34. A separate ground plane has been split for RF or hard to manage signals. These signals can be routed to the ADC differentially or single ended (i.e., both can either be connected to the driver or RF ground). The ADC will perform well with several hundred mV of noise or signals between the RF and ADC analog ground.

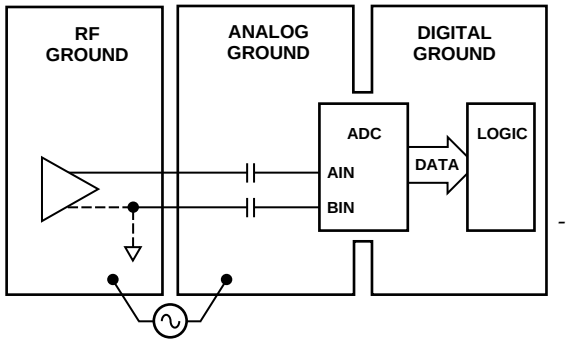


Figure 34. RF Ground Scheme

EVALUATION BOARD

The AD9201 evaluation board is shipped "ready to run." Power and signal generators should be connected as shown in Figure 35. Then the user can observe the performance of the Q channel. If the user wants to observe the I channel, then he should install a jumper at JP22 Pins 1 and 2. If the user wants to toggle between I and Q channels, then a CMOS level pulse train should be applied to the "strobe" jack after appropriate jumper connections.

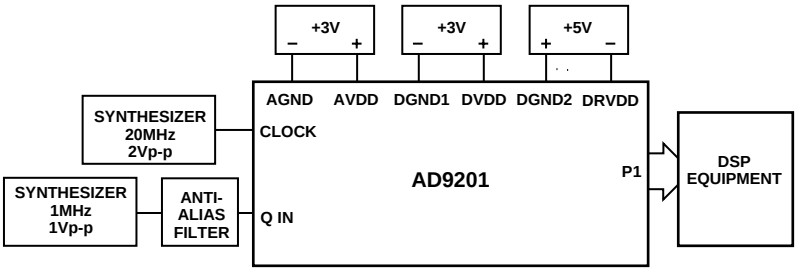


Figure 35. Evaluation Board Connections

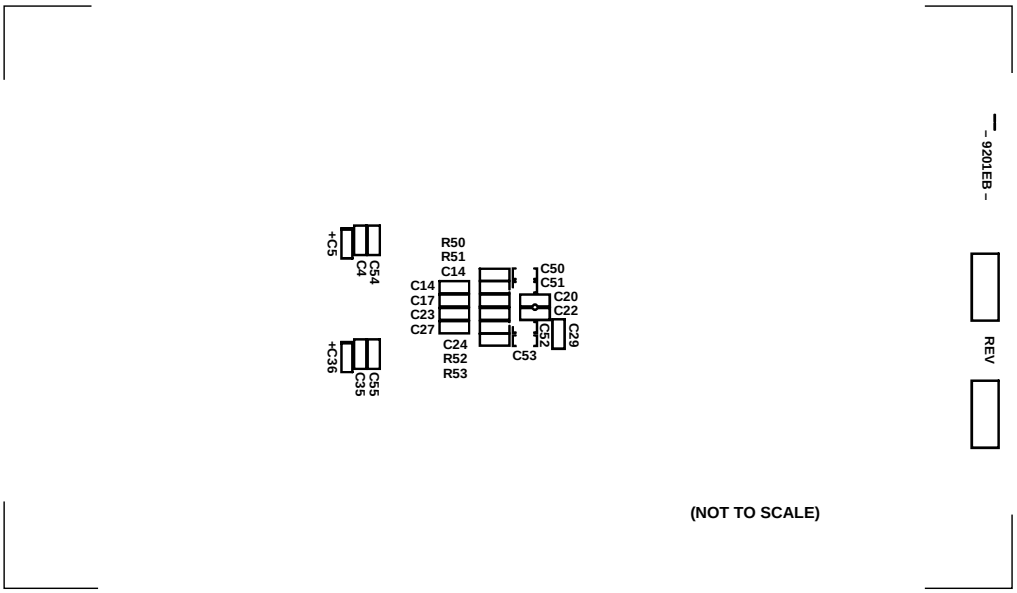


Figure 36. Evaluation Board Solder-Side Silkscreen

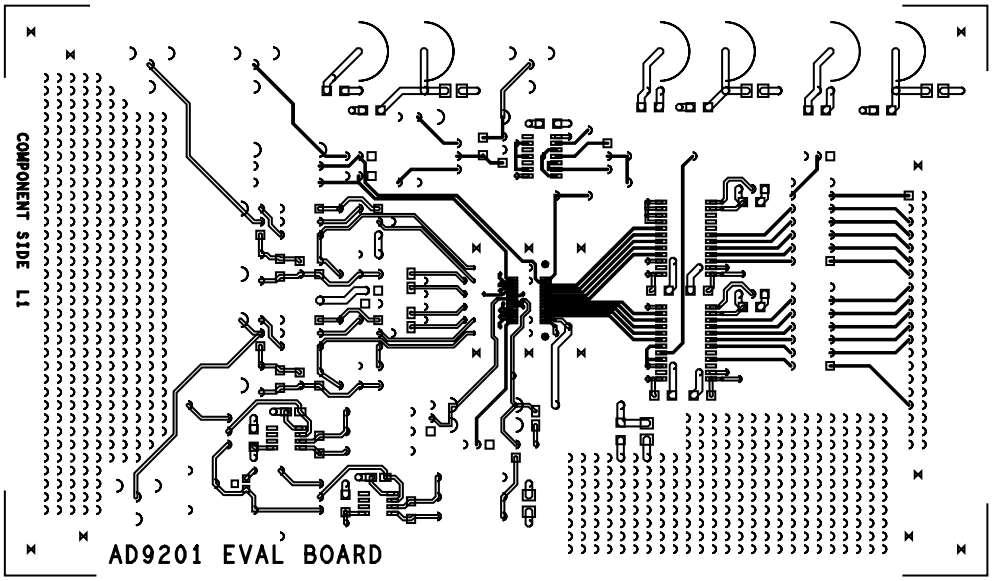


Figure 37. Evaluation Board Component-Side Layout

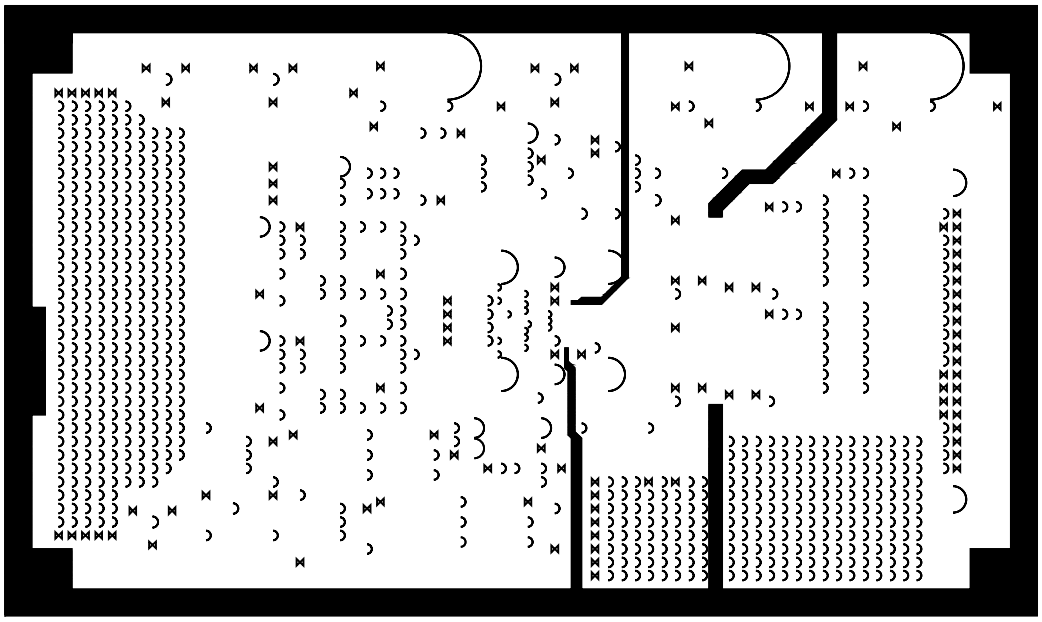


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Figure 38. Evaluation Board Ground Plane Layout

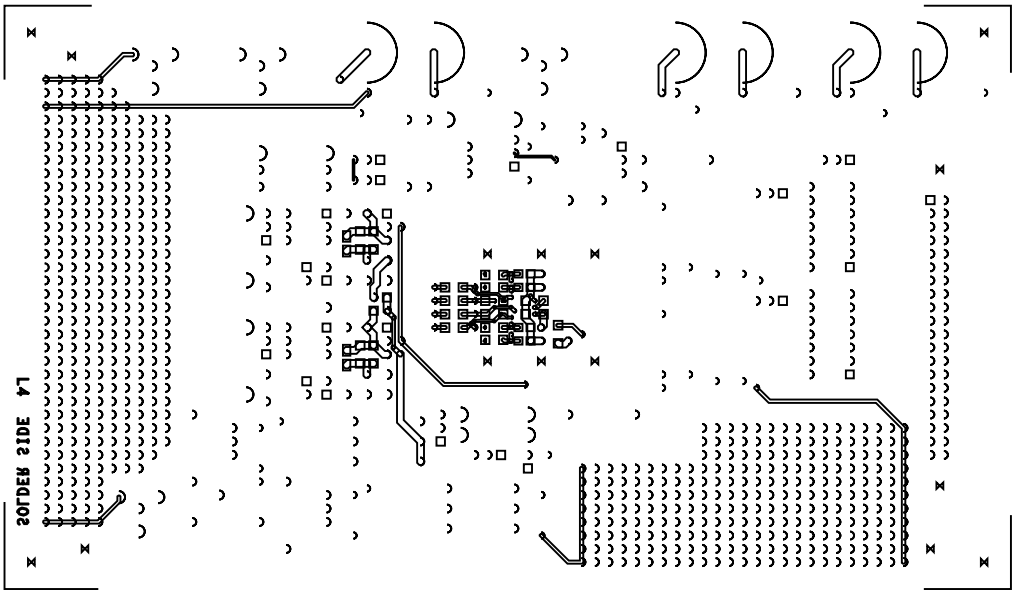

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Figure 39. Evaluation Board Solder-Side Layout

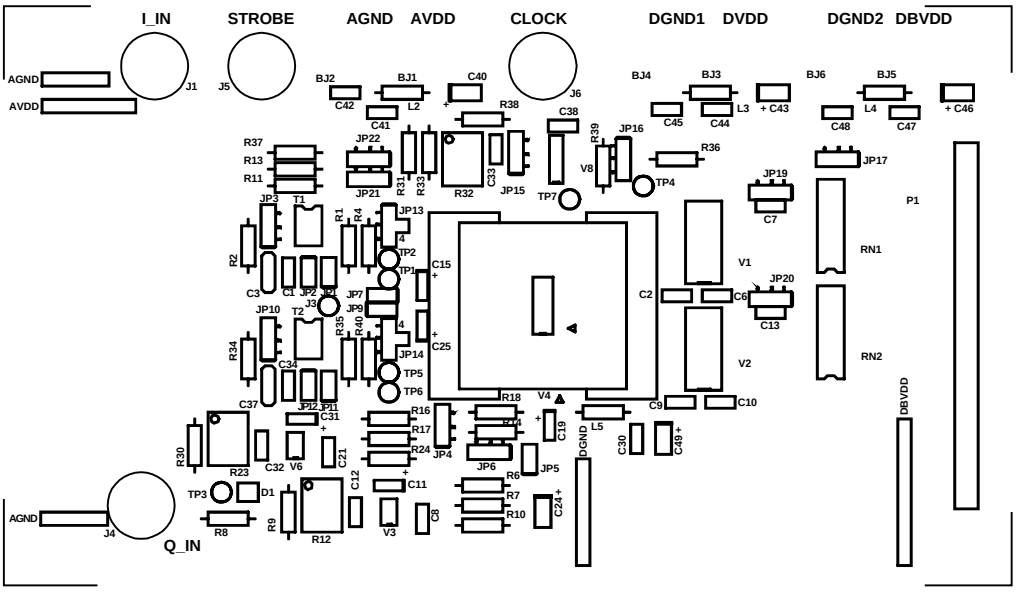

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Figure 40. Evaluation Board Component-Side Silkscreen

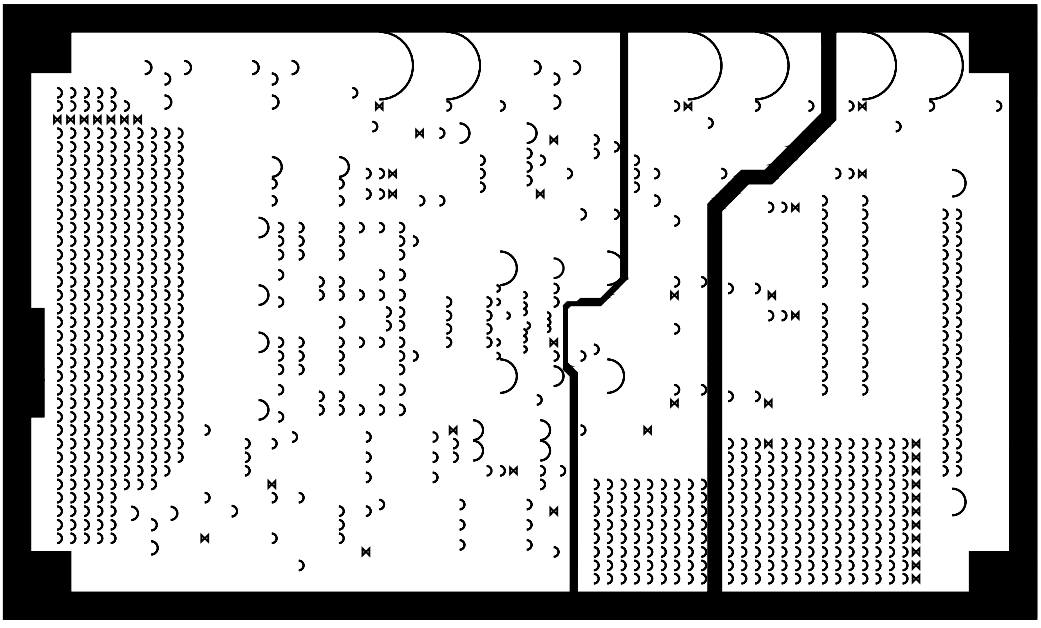

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Figure 41. Evaluation Board Power Plane Layout

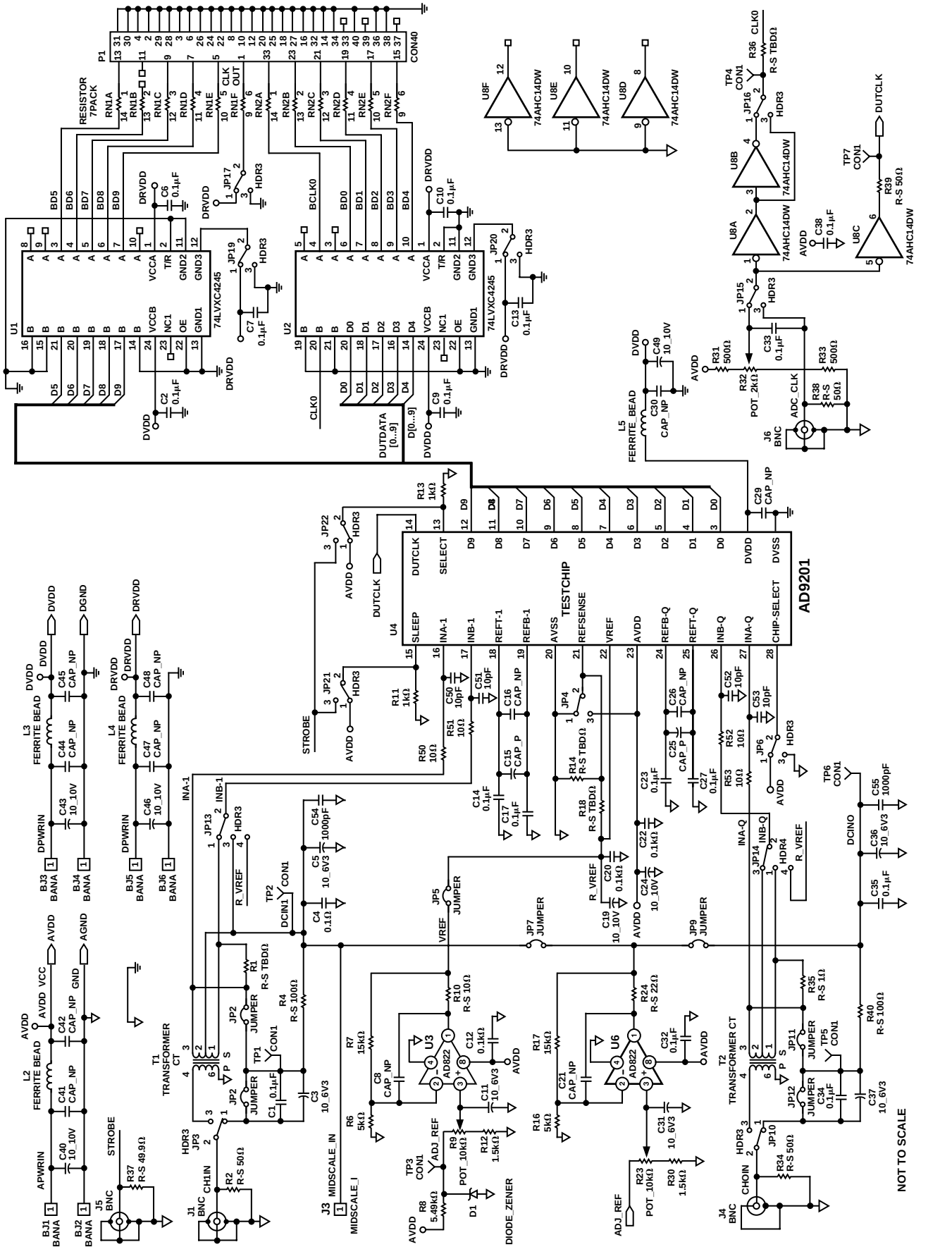
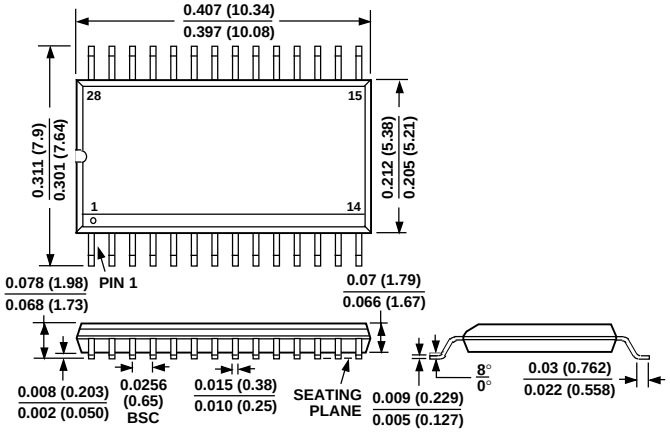


Figure 42. Evaluation Board

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline Package (SSOP)
(RS-28)



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