

OptiMOS® Power-Transistor

Feature

- N-Channel
- Enhancement mode
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

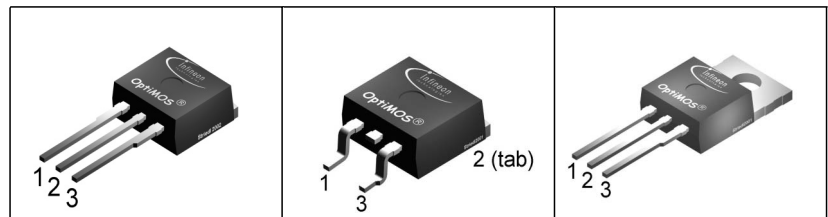
Product Summary

| | | |
|-------------------------------|-----|----|
| V_{DS} | 40 | V |
| $R_{DS(on)}$ max. SMD version | 3.4 | mΩ |
| I_D | 80 | A |

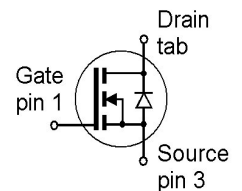
P- TO262 -3-1

P- TO263 -3-2

P- TO220 -3-1



| Type | Package | Ordering Code | Marking |
|---------------|---------------|---------------|---------|
| SPP80N04S2-04 | P- TO220 -3-1 | Q67040-S4260 | 2N0404 |
| SPB80N04S2-04 | P- TO263 -3-2 | Q67040-S4257 | 2N0404 |
| SPI80N04S2-04 | P- TO262 -3-1 | Q67060-S6173 | 2N0404 |



Maximum Ratings, at $T_j = 25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Value | Unit |
|---|----------------|-------------|-------|
| Continuous drain current ¹⁾ | I_D | 80 | A |
| $T_C=25\text{ °C}$ | | 80 | |
| $T_C=100\text{ °C}$ | | 80 | |
| Pulsed drain current | I_D puls | 320 | |
| $T_C=25\text{ °C}$ | | | |
| Avalanche energy, single pulse | E_{AS} | 810 | mJ |
| $I_D=80\text{ A}$, $V_{DD}=25\text{ V}$, $R_{GS}=25\text{ Ω}$ | | | |
| Repetitive avalanche energy, limited by T_{jmax} ²⁾ | E_{AR} | 30 | |
| Reverse diode dv/dt | dv/dt | 6 | kV/μs |
| $I_S=80\text{ A}$, $V_{DS}=32\text{ V}$, $di/dt=200\text{ A/μs}$, $T_{jmax}=175\text{ °C}$ | | | |
| Gate source voltage | V_{GS} | ±20 | V |
| Power dissipation | P_{tot} | 300 | W |
| $T_C=25\text{ °C}$ | | | |
| Operating and storage temperature | T_j, T_{stg} | -55... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | | 55/175/56 | |

Thermal Characteristics

| Parameter | Symbol | Values | | | Unit |
|---|------------|--------|------|----------|------|
| | | min. | typ. | max. | |
| Characteristics | | | | | |
| Thermal resistance, junction - case | R_{thJC} | - | 0.3 | 0.5 | K/W |
| Thermal resistance, junction - ambient, leaded | R_{thJA} | - | - | 62 | |
| SMD version, device on PCB: @ min. footprint @ 6 cm ² cooling area ³⁾ | R_{thJA} | - | - | 62 40 | |

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|---|---------------|--------|-----------|------------|------------|
| | | min. | typ. | max. | |
| Static Characteristics | | | | | |
| Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$ | $V_{(BR)DSS}$ | 40 | - | - | V |
| Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=250\mu A$ | $V_{GS(th)}$ | 2.1 | 3 | 4 | |
| Zero gate voltage drain current $V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$ | I_{DSS} | - | 0.01 1 | 1 100 | μA |
| Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$ | I_{GSS} | - | 1 | 100 | nA |
| Drain-source on-state resistance ⁴⁾ $V_{GS}=10V, I_D=80A$ $V_{GS}=10V, I_D=80A, \text{ SMD version}$ | $R_{DS(on)}$ | - | 3 2.7 | 3.7 3.4 | m Ω |

¹Current limited by bondwire ; with an $R_{thJC} = 0.5K/W$ the chip is able to carry $I_D = 208A$ at 25°C , for detailed information see app.-note ANPS071E available at www.infineon.com/optimos

²Defined by design. Not subject to production test.

³Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

⁴Diagrams are related to straight lead versions

Electrical Characteristics

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic Characteristics

| | | | | | | |
|------------------------------|--------------|---|----|------|------|----|
| Transconductance | g_{fs} | $V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 80A$ | 60 | 125 | - | S |
| Input capacitance | C_{iss} | $V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$ | - | 5250 | 6980 | pF |
| Output capacitance | C_{oss} | | - | 1870 | 2490 | |
| Reverse transfer capacitance | C_{rss} | | - | 420 | 630 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 20V$, $V_{GS} = 10V$, $I_D = 80A$, $R_G = 2.2\Omega$ | - | 16 | 24 | ns |
| Rise time | t_r | | - | 45 | 68 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 50 | 75 | |
| Fall time | t_f | | - | 40 | 60 | |

Gate Charge Characteristics

| | | | | | | |
|-----------------------|-----------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD} = 32V$, $I_D = 80A$ | - | 25 | 35 | nC |
| Gate to drain charge | Q_{gd} | | - | 50 | 75 | |
| Gate charge total | Q_g | $V_{DD} = 32V$, $I_D = 80A$, $V_{GS} = 0$ to $10V$ | - | 135 | 170 | |
| Gate plateau voltage | $V_{(plateau)}$ | $V_{DD} = 32V$, $I_D = 80A$ | - | 5.3 | - | V |

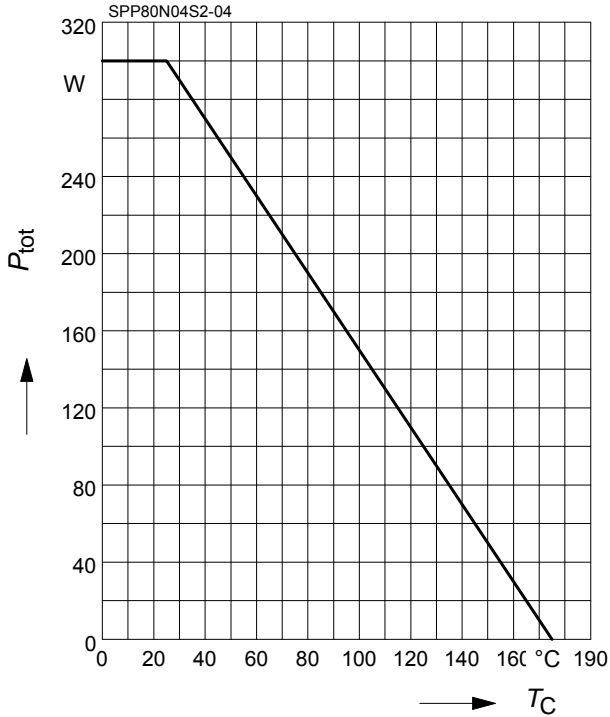
Reverse Diode

| | | | | | | |
|--|----------|---|---|-----|-----|----|
| Inverse diode continuous forward current | I_S | $T_C = 25^\circ C$ | - | - | 80 | A |
| Inv. diode direct current, pulsed | I_{SM} | | - | - | 320 | |
| Inverse diode forward voltage | V_{SD} | $V_{GS} = 0V$, $I_F = 80A$ | - | 0.9 | 1.3 | V |
| Reverse recovery time | t_{rr} | $V_R = 20V$, $I_F = I_S$, $di_F/dt = 100A/\mu s$ | - | 60 | 75 | ns |
| Reverse recovery charge | Q_{rr} | | - | 100 | 125 | nC |

1 Power dissipation

$$P_{tot} = f(T_C)$$

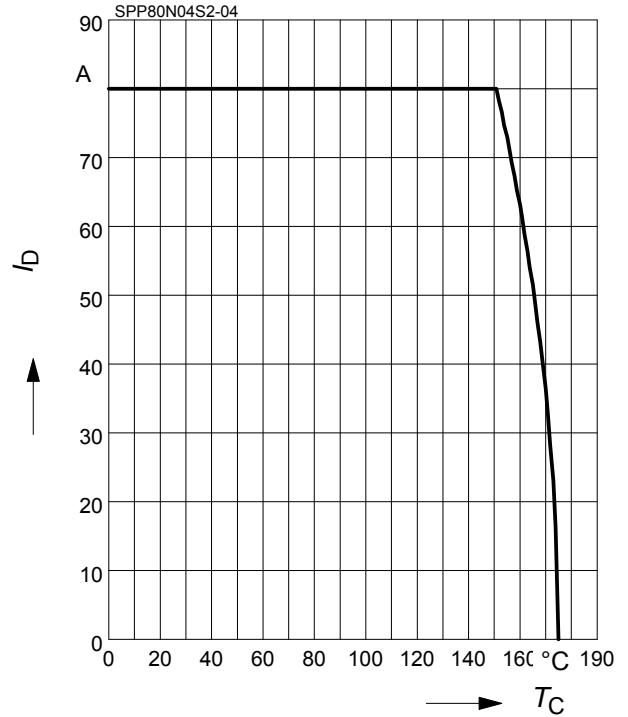
parameter: $V_{GS} \geq 6\text{ V}$



2 Drain current

$$I_D = f(T_C)$$

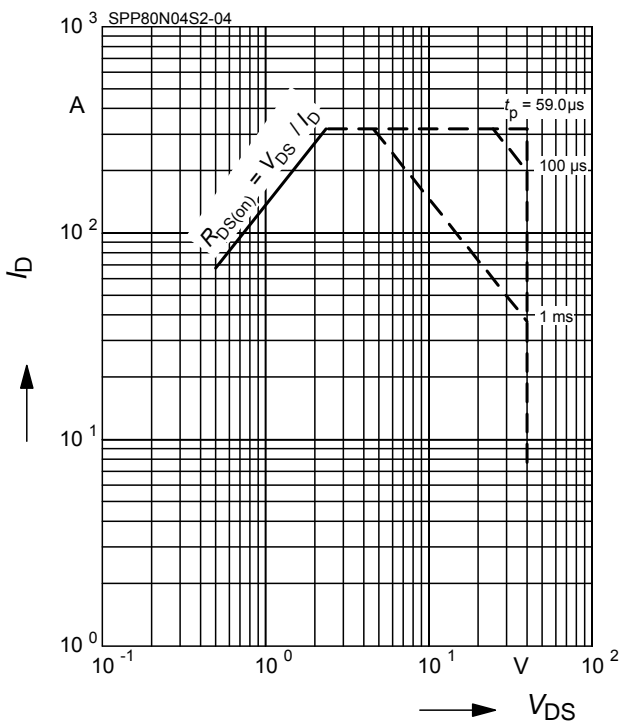
parameter: $V_{GS} \geq 10\text{ V}$



3 Safe operating area

$$I_D = f(V_{DS})$$

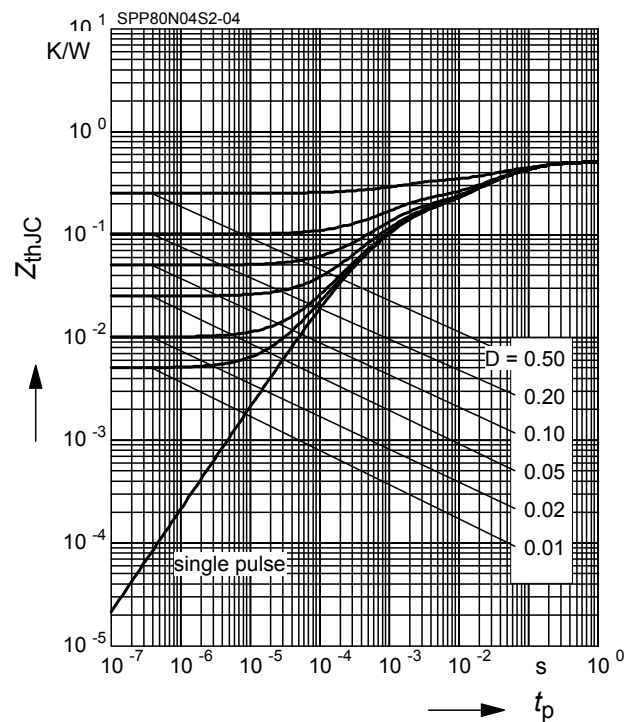
parameter: $D = 0, T_C = 25\text{ °C}$



4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

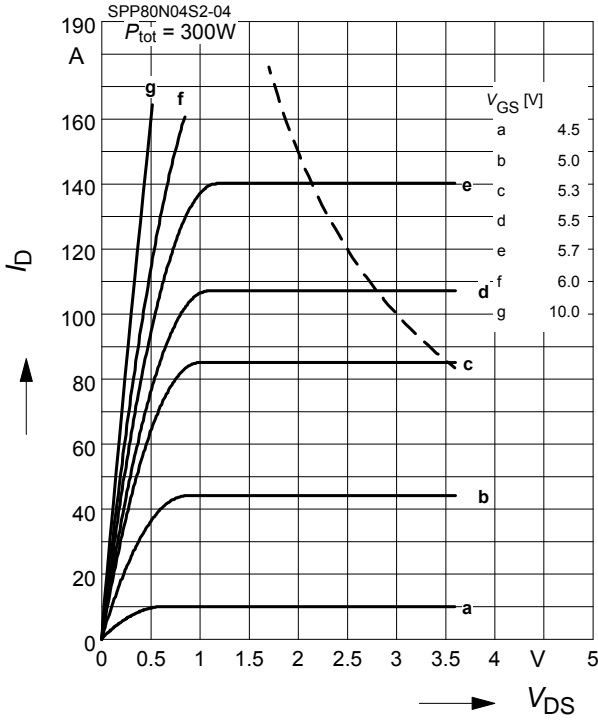
parameter: $D = t_p/T$



5 Typ. output characteristic

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

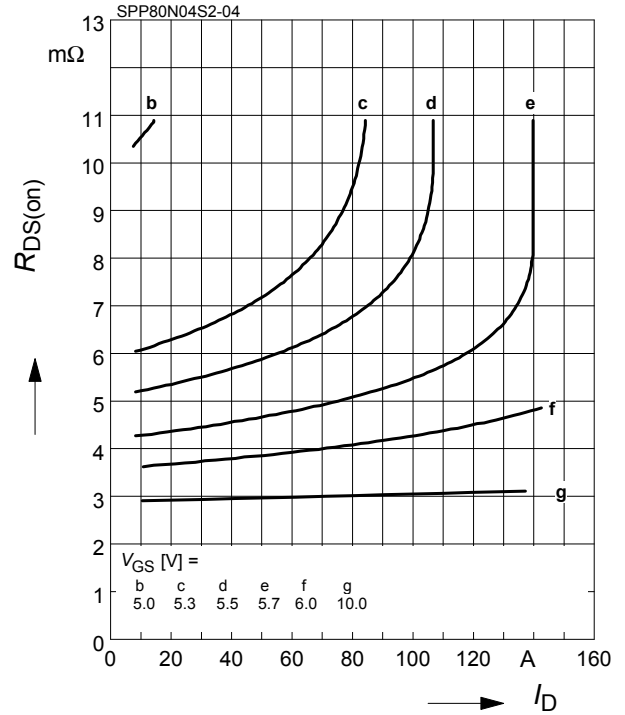
parameter: $t_p = 80 \mu\text{s}$



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$

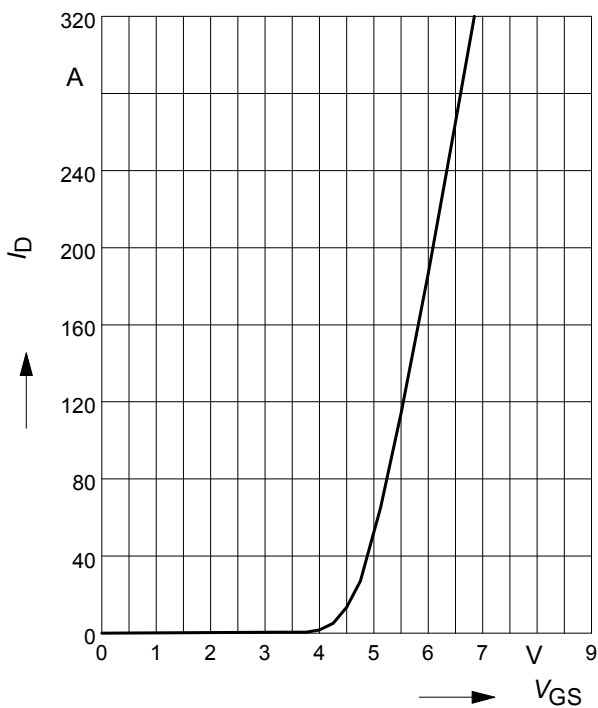
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

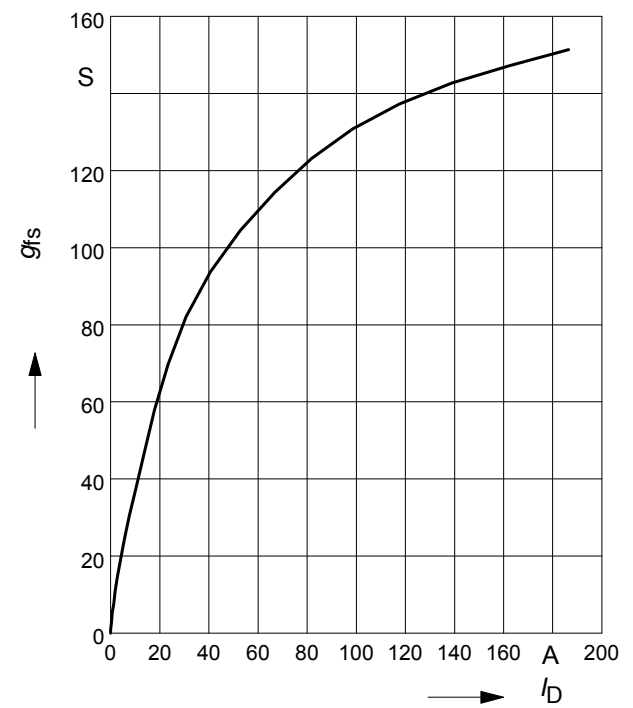
parameter: $t_p = 80 \mu\text{s}$



8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

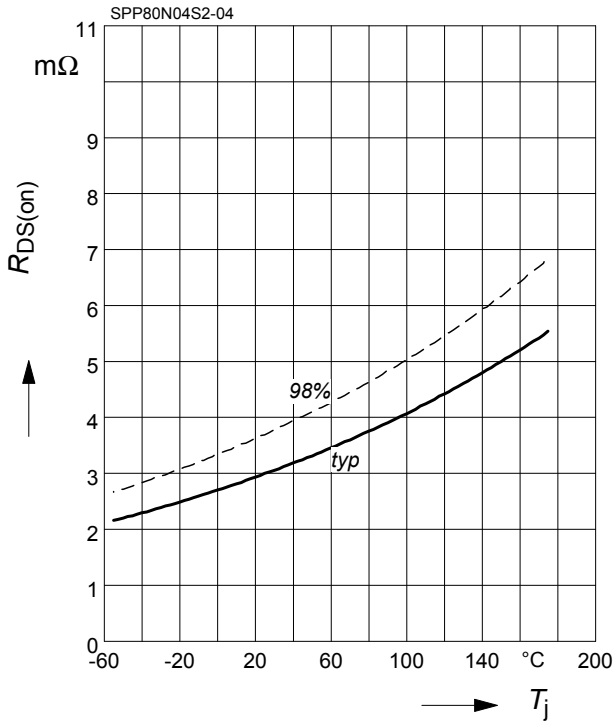
parameter: g_{fs}



9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

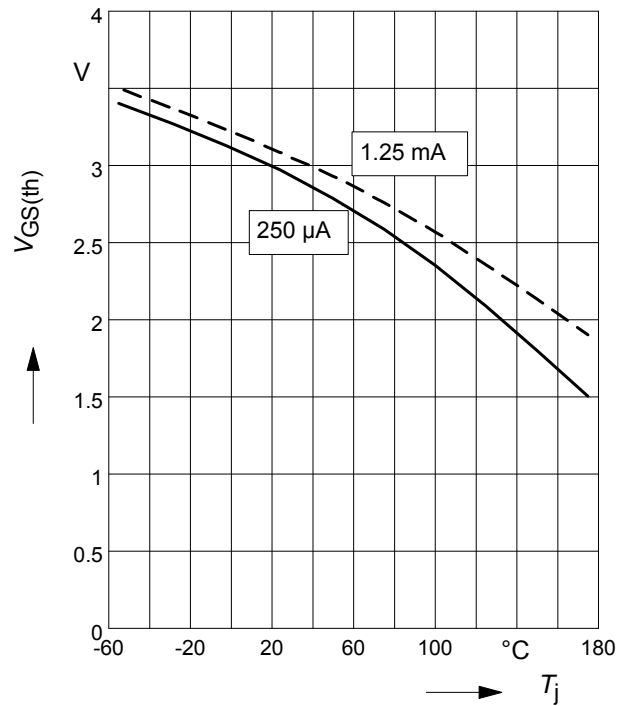
parameter: $I_D = 80\text{ A}$, $V_{GS} = 10\text{ V}$



10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

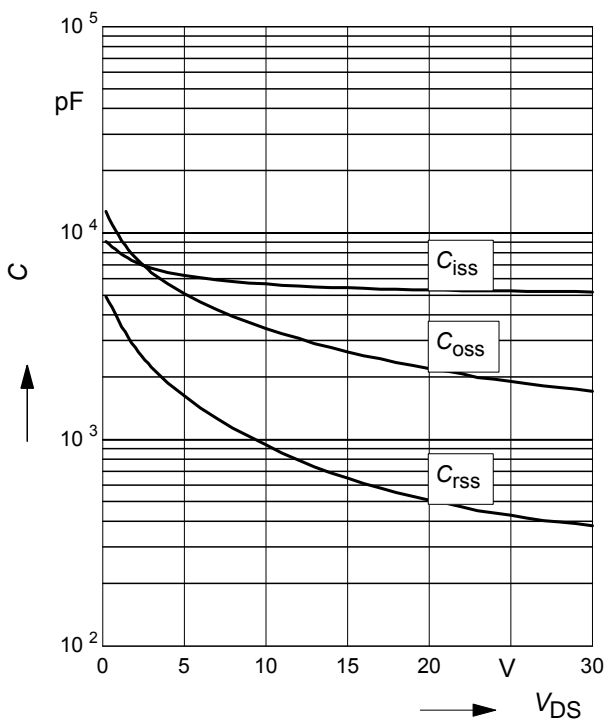
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$$C = f(V_{DS})$$

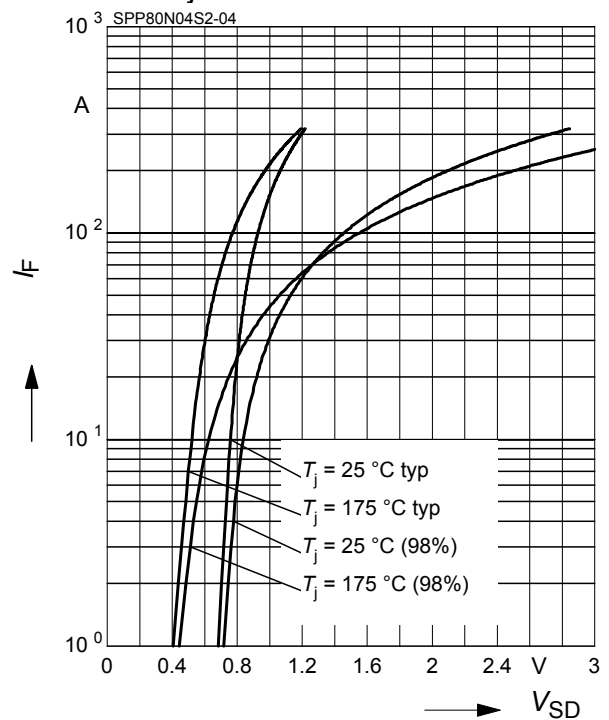
parameter: $V_{GS}=0\text{ V}$, $f=1\text{ MHz}$



12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

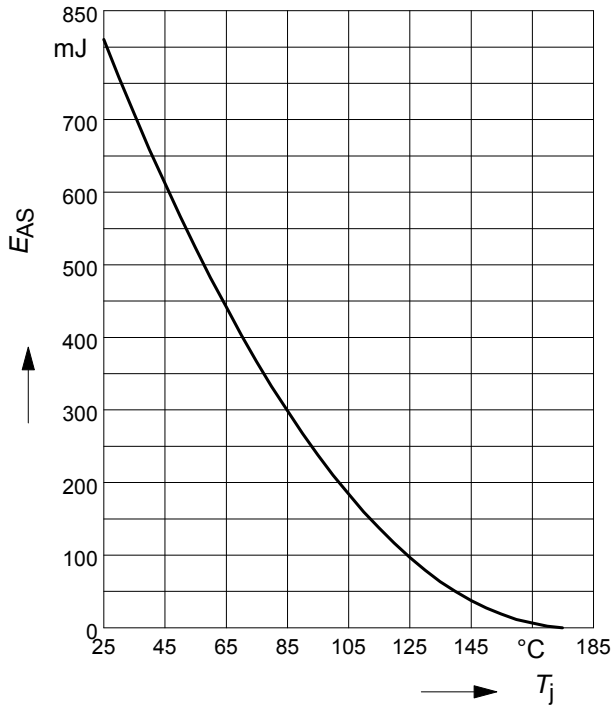
parameter: T_j , $t_p = 80\text{ μs}$



13 Typ. avalanche energy

$$E_{AS} = f(T_j)$$

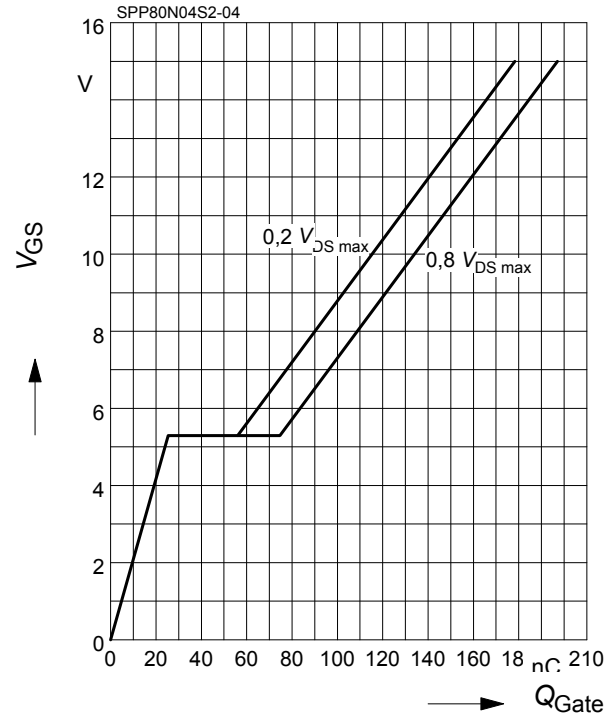
par.: $I_D = 80\text{ A}$, $V_{DD} = 25\text{ V}$, $R_{GS} = 25\ \Omega$



14 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

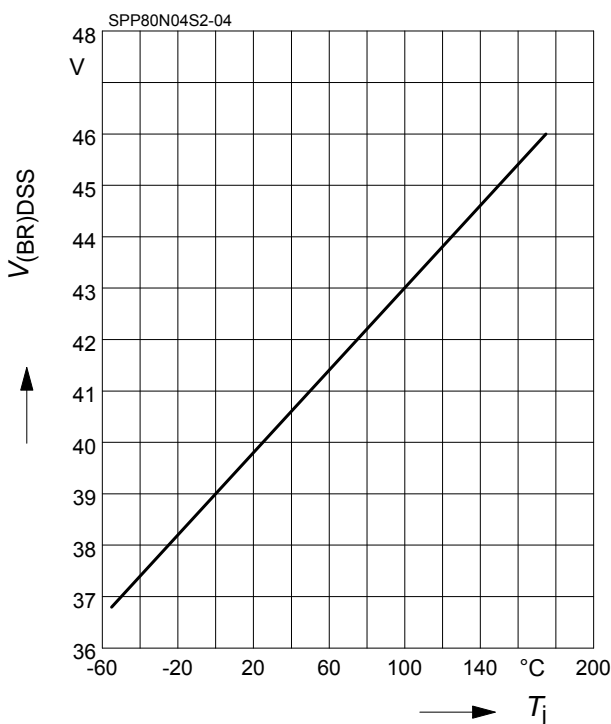
parameter: $I_D = 80\text{ A}$ pulsed



15 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$

parameter: $I_D = 10\text{ mA}$



Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 53,
D-81541 München
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Further information

Please notice that the part number is **BSPP80N04S2-04** and **BSPB80N04S2-04**, for simplicity the device is referred to by the term **SPP80N04S2-04** and **SPB80N04S2-04** throughout this documentation.

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