THE DATASHEET OF

AD664JPZ

Monolithic, 12-Bit Quad DAC

Data Sheet **AD664**

FEATURES

Four complete voltage-output DACs
Data register readback feature
Reset to zero override
Multiplying operation
Double buffered latches
Surface-mount (LCC, PLCC, and JLCC) and PDIP and SBDIP packages
MIL-STD-883 compliant versions available

APPLICATIONS

Automatic test equipment
Robotics
Process control
Disk drives
Instrumentation
Avionics

GENERAL DESCRIPTION

The AD664 is four complete 12-bit, voltage-output digital-to-analog converters (DACs) on one monolithic IC chip. Each DAC has a double buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible input/output (I/O) port.

The I/O port accommodates 4-bit, 8-bit, or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier, and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital input/output port and may be set to unipolar (UNI) or bipolar (BIP) range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

The functional completeness of the AD664 results from the combination of the Analog Devices, Inc., BiMOS II process, laser trimmed thin film resistors, and double level metal interconnects.

PRODUCT HIGHLIGHTS

1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit DAC function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.
4. The asynchronous reset control returns all DAC outputs to 0 V.
5. DAC to DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2 LSB at room temperature and 3/4 LSB maximum for the K, B, and T grades.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have tristate outputs.
9. Multiplying mode operation allows use with fixed, variable, positive, or negative external references.
10. The AD664 is available in versions compliant with MILSTD-883.

Rev. E Document Feedback

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11/2018—Rev. D to Rev. E

Updated Format ... Universal
Reorganized Layout ... Universal
Changed 28-Pin to 28-Lead ... Universal
Changed 44-Pin to 44-Lead and 44-Terminal ... Universal
Added 39-Pad Bare Die ... Universal
Removed AD345 ... Universal
Removed AD689 ... Universal
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2/2012—Rev. C to Rev. D

12/91—Rev. B to Rev. C

FUNCTIONAL BLOCK DIAGRAMS

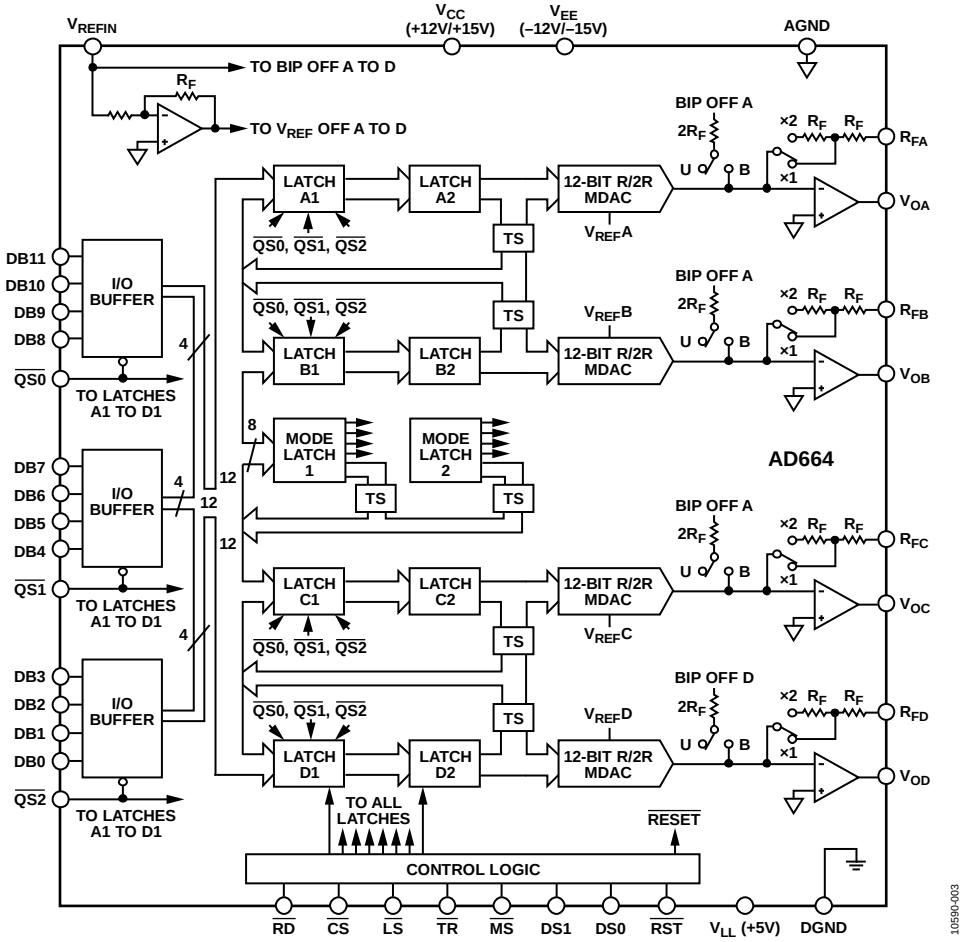


Figure 1. 44-Lead JLCC and PLCC and 44-Terminal LCC Functional Block Diagram

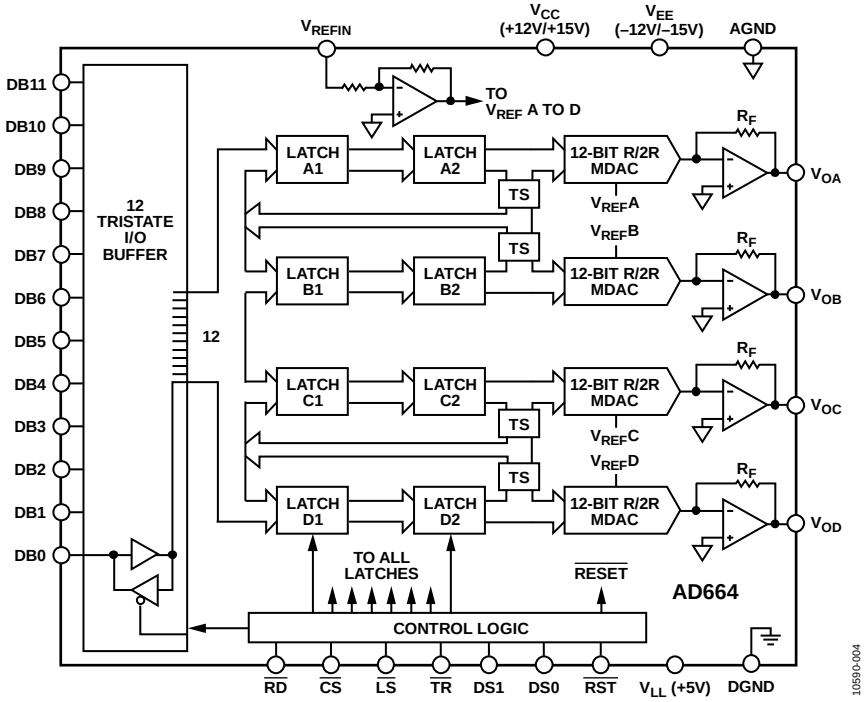


Figure 2. 28-Lead PDIP and SBDIP Functional Block Diagram

SPECIFICATIONS

V_{LL} = +5 V, V_{CC} = +15 V, V_{EE} = −15 V, V_{REF} = +10 V, and T_A = +25°C, unless otherwise noted.

Table 1.

	AD664Jx/AD664Ax/AD664SD			AD664Kx/AD664Bx/AD664TD/AD664TE			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12	12		12	12	Bits
ANALOG OUTPUT							
Voltage Range[1]							
UNI Versions	0		V_{CC} − 2.0[2]	0		V_{CC} − 2.0[2]	V
BIP Versions	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	V
Output Current	5			5			mA
Load Resistance		2			2		kΩ
Load Capacitance			500			500	pF
Short-Circuit Current		25	40		25	40	mA
ACCURACY							
Gain Error	−7	±3	+7	−5	±2	+5	LSB
UNI Offset	−2	±1/2	+2	−1	±1/4	+1	LSB
BIP Zero[3]	−3	±3/4	+3	−2	±1/2	+2	LSB
Linearity Error[4]	−3/4	±1/2	+3/4	−1/2	±1/4	+1/2	LSB
Linearity T_{MIN} to T_{MAX}	−1	±3/4	+1	−3/4	±1/2	+3/4	LSB
Differential Linearity	−3/4		+3/4	−1/2		+1/2	LSB
Differential Linearity T_{MIN} to T_{MAX}		Monotonic[5]			Monotonic[5]		
Gain Error Drift							
UNI 0 V to +10 V Mode	−12	±7	+12	−10	±5	+10	ppm of FSR[6]/°C
BIP −5 V to +5 V Mode	−12	±7	+12	−10	±5	+10	ppm of FSR/°C
BIP −10 V to +10 V Mode	−12	±7	+12	−10	±5	+10	ppm of FSR/°C
UNI Offset Drift							
UNI 0 V to +10 V Mode	−3	±1.5	+3	−2	±1	+2	ppm of FSR/°C
BIP Zero Drift							
BIP −5 V to +5 V Mode	−12	±7	+12	−10	±5	+10	ppm of FSR/°C
BIP −10 V to +10 V Mode	−12	±7	+12	−10	±5	+10	ppm of FSR/°C
REFERENCE INPUT							
Input Resistance	1.3		2.6	1.3		2.6	kΩ
Voltage Range[7]	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	V
POWER REQUIREMENTS							
V_{LL}	4.5	5.0	5.5	4.5	5.0	5.5	V
I_{LL}							
At V_{IH}, V_{IL} = 5 V, 0 V		0.1	1		0.1	1	mA
At V_{IH}, V_{IL} = 2.4 V, 0.4 V		3	6		3	6	mA
V_{CC}/V_{EE}	±11.4		±16.5	±11.4		±16.5	V
I_{CC}		12	15		12	15	mA
I_{EE}		15	19		15	19	mA
Total Power		400	525		400	525	mW

Parameter	AD664Jx/AD664Ax/AD664SD Min	Typ	Max	AD664Kx/AD664Bx/AD664TD/AD664TE Min	Typ	Max	Unit
ANALOG GROUND CURRENT[8]	−600	±400	+600	−600	±400	+600	µA
MATCHING PERFORMANCE							
Gain Error[9]	−6	±3	+6	−4	±2	+4	LSB
Offset Error[10]	−2	±1/2	+2	−1	±1/4	+1	LSB
BIP Zero Error[11]	−3	±1	+3	−2	±1	+2	LSB
Linearity Error[12]	−1.5	±1/2	+1.5	−1	±1/2	+1	LSB
CROSSTALK							
Analog			−90			−90	dB
Digital			−60			−60	dB
DYNAMIC PERFORMANCE (R_L = 2 kΩ, C_L = 500 pF)							
Settling Time to ±1/2 LSB							
All Bits Switched from 0 to 1 or 1 to 0, Gain = 1, V_{REF} = 10		8	10		8	10	µs
Settling Time to ±1/2 LSB							
V_{REF} (−10 V to 10 V), Gain = 1, Bits On		10			10		µs
Glitch Impulse			500			500	nV-sec
MULTIPLYING MODE PERFORMANCE							
Reference Feedthrough at 1 kHz		−75			−75		dB
Reference −3 dB Bandwidth		70			70		kHz
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} (11.4 V to 16.5 V)		±2	±5		±2	±5	ppm/%
V_{EE} (−16.5 V to −11.4 V)		±2	±5		±2	±5	ppm/%
V_{LL} (4.5 V to 5.5 V)		±2	±5		±2	±5	ppm/%
DIGITAL INPUTS							
V_{IH}	2.0			2.0			V
V_{IL}	0		0.8	0		0.8	V
Data Inputs							
I_{IH} at V_{IN} = V_{LL}	−10	±1	+10	−10	±1	+10	µA
I_{IL} at V_{IN} = DGND	−10	±1	+10	−10	±1	+10	µA
$\overline{CS}$/DS0/DS1/$\overline{RST}$/$\overline{RD}$/$\overline{LS}$							
I_{IH} at V_{IN} = V_{LL}	−10	±1	+10	−10	±1	+10	µA
I_{IL} at V_{IN} = V_{LL}	−10	±1	+10	−10	±1	+10	µA
$\overline{MS}$/$\overline{TR}$[13]							
I_{IH} at V_{IN} = V_{LL}	−10	+5	+10	−10	+5	+10	µA
I_{IL} at V_{IN} = DGND	−10	−5	0	−10	−5	0	µA
$\overline{QS0}$/$\overline{QS1}$/$\overline{QS2}$[13]							
I_{IH} at V_{IN} = V_{LL}	−10	+5	+10	−10	+5	+10	µA
I_{IL} at V_{IN} = DGND	−10	±1	+10	−10	±1	+10	µA
DIGITAL OUTPUTS							
V_{OL} at 1.6 mA Sink			0.4			0.4	V
V_{OH} at 0.5 mA Source	2.4			2.4			V

Parameter	AD664Jx/AD664Ax/AD664SD Min	Typ	Max	AD664Kx/AD664Bx/AD664TD/AD664TE Min	Typ	Max	Unit
TEMPERATURE RANGE							
AD664Jx/AD664Kx	0		70	0		70	°C
AD664Ax/AD664Bx	−40		+85	−40		+85	°C
AD664SD/AD664TD/AD664TE/AD664TJ	−55		+125	−55		+125	°C

[1] A minimum power supply of ±12.0 V is required for 0 V to +10 V and ±10 V operation. A minimum power supply of ±11.4 V is required for −5 V to +5 V operation.
[2] For V_{CC} < +12 V and V_{EE} > −12 V. Voltage not to exceed 10 V maximum.
[3] BIP zero error is the difference from the ideal output (0 V) and the actual output voltage with code 100 000 000 000 applied to the inputs.
[4] Linearity error is defined as the maximum deviation of the actual DAC output from the ideal output (a straight line drawn from zero scale to full-scale (FS) − 1 LSB).
[5] Monotonic at all temperatures. Differential linearity specifications are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
[6] Full-scale range (FSR) is +20 V for a ±10 V range and +10 V for a ±5 V range.
[7] A minimum power supply of ±12.0 V is required for a +10 V reference voltage.
[8] Analog ground current is input code dependent.
[9] Gain error matching is the largest difference in gain error between any two DACs in one package.
[10] Offset error matching is the largest difference in offset error between any two DACs in one package.
[11] BIP zero error matching is the largest difference in BIP zero error between any two DACs in one package.
[12] Linearity error matching is the difference in the worst ease linearity error between any two DACs in one package.
[13] 44-lead (JLCC and PLCC) and 44-terminal (LCC) versions only.

ABSOLUTE MAXIMUM RATINGS

Table 2.

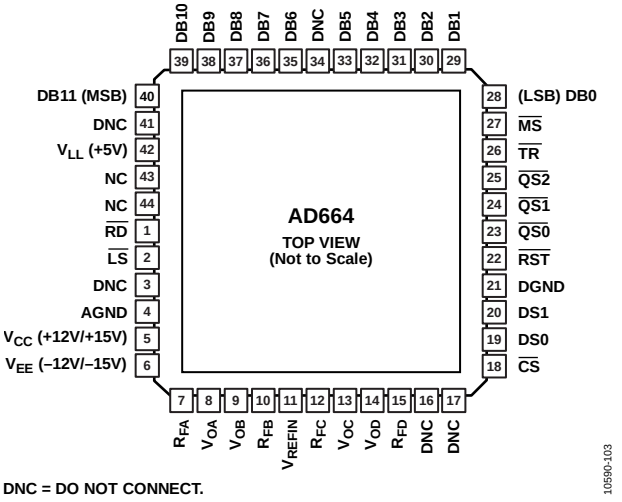
Parameter	Rating
V_{LL} to DGND	0 V to 7 V
V_{CC} to DGND	0 V to 18 V
V_{EE} to DGND	−18 V to 0 V
Soldering	300°C, 10 sec
Power Dissipation	1000 mW
AGND to DGND	−1 V to +1 V
Reference Input	$V_{REFIN} \leq \pm 10$ V and $V_{REFIN} \leq (V_{CC} - 2$ V, $V_{EE} + 2$ V)
V_{CC} to V_{EE}	0 V to 36 V
Digital Inputs	−0.3 V to +7 V
Analog Inputs	Indefinite shorts to V_{CC}, V_{LL}, V_{EE}, and AGND

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

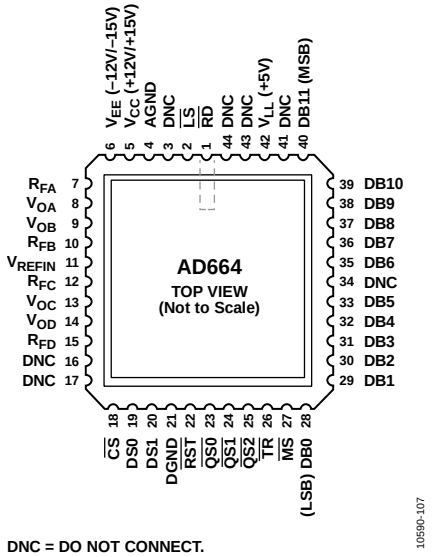
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



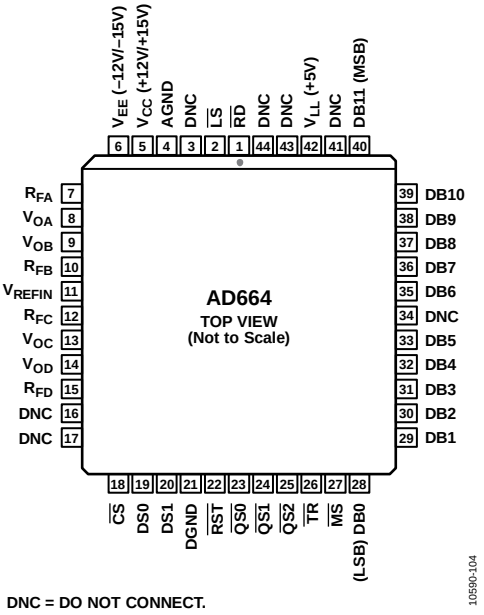
DNC = DO NOT CONNECT.

Figure 3. 44-Lead JLCC Pin Configuration



DNC = DO NOT CONNECT.

Figure 5. 44-Terminal LCC Pad Configuration



DNC = DO NOT CONNECT.

Figure 4. 44-Lead PLCC Pin Configuration

Table 3. 44-Lead JLCC, 44-Lead PLCC, and 44-Terminal LCC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{RD}$	Readback Pin (Active Low).
2	$\overline{LS}$	Latch Select Pin (Active Low).
3, 16, 17, 34, 41, 43, 44	DNC	Do Not Connect.
4	AGND	Analog Ground Pin.
5	V_{CC} (+12V/+15V)	Positive Analog Supply Connection.
6	V_{EE} (−12V/−15V)	Negative Analog Supply Connection.
7	R_{FA}	Feedback Connection for DAC A.
8	V_{OA}	Analog Output Voltage from DAC A.
9	V_{OB}	Analog Output Voltage from DAC B.
10	R_{FB}	Feedback Connection for DAC B.

Pin No.	Mnemonic	Description
11	V_{REFIN}	Reference Input Voltage Pin.
12	R_{FC}	Feedback Connection for DAC C.
13	V_{OC}	Analog Output Voltage from DAC C.
14	V_{OD}	Analog Output Voltage from DAC D.
15	R_{FD}	Feedback Connection for DAC D.
18	$\overline{CS}$	Chip Select Pin (Active Low).
19	DS0	DAC Address Data 0.
20	DS1	DAC Address Data 1.
21	DGND	Digital Ground.
22	$\overline{RST}$	Reset Pin (Active Low).
23	$\overline{QS0}$	4-Bit Nibble Data.
24	$\overline{QS1}$	8-Bit Nibble Data.
25	$\overline{QS2}$	12-Bit Nibble Data.
26	$\overline{TR}$	Transfer Register Pin (Active Low).
27	$\overline{MS}$	Mode Select Pin (Active Low).
28 to 33, 35 to 40	DB0 to DB11	Data Input/Outputs. DB11 is MSB.
42	V_{LL} (+5V)	Digital Supply.

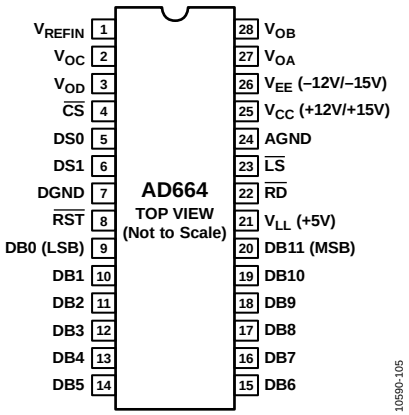


Figure 6. 28-Lead SBDIP Pin Configuration

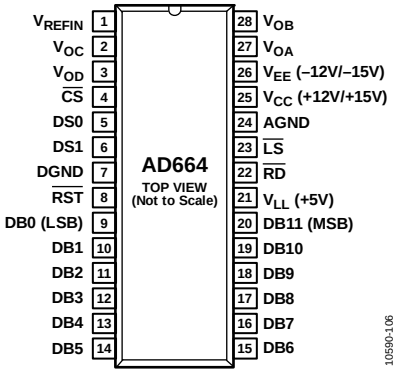


Figure 7. 28-Lead PDIP Pin Configuration

Table 4. 28-Lead SBDIP and 28-Lead PDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{REFIN}	Reference Input Voltage Pin.
2	V_{OC}	Analog Output Voltage from DAC C.
3	V_{OD}	Analog Output Voltage from DAC D.
4	$\overline{CS}$	Chip Select Pin (Active Low).
5	DS0	DAC Address Data 0.
6	DS1	DAC Address Data 1.
7	DGND	Digital Ground.
8	$\overline{RST}$	Reset Pin (Active Low).
9 to 20	DB0 to DB11	Data Input/Outputs. DB11 is MSB.
21	V_{LL} (+5V)	Digital Supply.
22	$\overline{RD}$	Readback Pin (Active Low).
23	$\overline{LS}$	Latch Select Pin (Active Low).
24	AGND	Analog Ground Pin.
25	V_{CC} (+12V/+15V)	Positive Analog Supply Connection.
26	V_{EE} (−12 V/−15 V)	Negative Analog Supply Connection.
27	V_{OA}	Analog Output Voltage from DAC A.
28	V_{OB}	Analog Output Voltage from DAC B.

TERMINOLOGY

Linearity Error
Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from zero scale to full-scale − 1 LSB) for any bit combination. This is also referred to as relative accuracy. The AD664 is laser trimmed to typically maintain linearity errors at less than ±1/4 LSB.

Monotonicity
A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output is always a nondecreasing function of input. All versions of the AD664 are monotonic over their full operating temperature range.

Differential Linearity
Monotonic behavior requires that the differential linearity error be less than 1 LSB both at 25°C as well as over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. For example, for a 10 V full-scale output, a change of 1 LSB in digital input code results in a 2.44 mV change in the analog output (V_{REF} = 10 V, Gain = 1, 1 LSB = 10 V × 1/4096 = 2.44 mV). If in actual use, a 1 LSB change in the input code results in a change of only 0.61 mV (1/4 LSB) in analog output, the differential nonlinearity error is −1.83 mV, or −3/4 LSB.

Gain Error
DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

UNI Offset Error
UNI offset error is the difference between the ideal output (0 V) and the actual output of a DAC when the input is loaded with all 0s and the mode is UNI.

BIP Zero Error
BIP zero error is the difference between the ideal output (0 V) and the actual output of a DAC when the input code is loaded with the MSB = 1 and the rest of the bits = 0 and the mode is BIP.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

Crosstalk
Crosstalk is the change in an output caused by a change in one or more of the other outputs. Crosstalk is due to capacitive and thermal coupling between outputs.

Reference Feedthrough
The portion of an ac reference signal that appears at an output when all input bits are low. Feedthrough is due to capacitive coupling between the reference input and the output, and is specified in decibels at a particular frequency.

Reference 3 dB Bandwidth
The frequency of the ac reference input signal at which the amplitude of the full-scale output response falls 3 dB from the ideal response.

Glitch Impulse
Glitch impulse is an undesired output voltage transient caused by asymmetrical switching times in the switches of a DAC. These transients are specified by their net area (in nV-sec) of the voltage vs. time characteristic.

THEORY OF OPERATION

The AD664 combines four complete 12-bit voltage output DAC converters with a fast, flexible digital I/O port on one monolithic chip. The AD664 is available in three forms. The device is available in a 44-lead version (JLCC and PLCC), a 44-terminal version (LCC) (all shown in Figure 1), and a 28-lead version (shown in Figure 2).

44-LEAD (JLCC/PLCC) VERSION AND 44-TERMINAL (LCC) VERSION

Each DAC offers flexibility, accuracy, and good dynamic performance. The R/2R structure is fabricated from thin film resistors, which are laser trimmed to achieve 1/2 LSB linearity and guaranteed monotonicity. The output amplifier combines the best features of the bipolar (BIP) and metal-oxide semiconductor (MOS) devices to achieve good dynamic performance and low offset. Settling time is under 10 µs and each output can drive a 5 mA, 500 pF load. Short-circuit protection allows indefinite shorts to V_{LL}, V_{CC}, V_{EE}, and AGND. The output and span resistor pins are available separately. This feature allows a user to insert current boosting elements to increase the drive capability of the system, as well as to overcome parasitics.

Digital circuitry is implemented in complementary metal-oxide semiconductor (CMOS) logic. The fast, low power, digital interface allows the AD664 to be interfaced with most microprocessors. Through this interface, the wide variety of features on each chip may be accessed. For example, the input data for each DAC is programmed by way of 4-bit, 8-bit, 12-bit, or 16-bit words. The double buffered input structure of this latch allows all four DACs to be updated simultaneously. A readback feature allows the internal registers to be read back through the same digital port, as either 4-bit, 8-bit, or 12-bit words. When disabled, the readback drivers are placed in a high impedance (tristate) mode. A transparent mode allows the input data to pass straight through both ranks of input registers and appear at the DAC with a minimum of delay. One DAC may be placed in the transparent mode at a time, or all four may be made transparent at once. The mode select feature allows the output range and mode of the DACs to be selected via the data bus inputs. An internal mode select register stores the selections. This register may also be read back to check its contents. A reset to zero feature allows all DACs to be reset to 0 V output by strobing a single pin.

28-LEAD VERSIONS

The 28-lead versions are dedicated versions of the 44-lead (JLCC and PLCC) and 44-terminal (LCC) AD664. Each offers a reduced set of features from those offered in the 44-lead version (JLCC and PLCC) and 44-terminal version (LCC). This accommodates the reduced number of package pins available. Data is written and read with 12-bit words only. Output range and mode select functions are also not available in 28-lead versions. As an alternative, users specify either the UNI (zero scale to V_{REFIN}) models or the BIP ($-V_{REFIN}$ to V_{REFIN}) models depending on the application requirements. Finally, the transparent mode is not available on the 28-lead versions.

Table 5. Transfer Functions

Gain	Mode = UNI	Mode = BIP
1	000000000000 = 0 V 100000000000 = $V_{REFIN}/2$ 111111111111 = V_{REFIN} − 1 LSB	000000000000 = − $V_{REFIN}/2$ 100000000000 = 0 V 111111111111 = $V_{REFIN}/2$ − 1 LSB
2	000000000000 = 0 V 100000000000 = V_{REFIN} 111111111111 = 2 × V_{REFIN} − 1 LSB	000000000000 = V_{REFIN} 100000000000 = 0 V 111111111111 = +V_{REFIN} − 1 LSB

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD664 has two pins, designated analog and digital ground. The analog ground pin is the high quality ground reference point for the device. A unique internal design has resulted in low analog ground current, which greatly simplifies management of ground current and the associated induced voltage drops. The analog ground pin is connected to the analog ground point in the system. The external reference and any external loads are also returned to analog ground.

The digital ground pin is connected to the digital ground point in the circuit. This pin returns current from the logic portions of the AD664 circuitry to ground.

Analog and digital grounds are connected at one point in the system. If there is a possibility that this connection be broken or otherwise disconnected, then two diodes are connected between the analog and digital ground pins of the AD664 to limit the maximum ground voltage difference.

POWER SUPPLIES AND DECOUPLING

The AD664 requires three power supplies for proper operation. V_{LL} powers the logic portions of the device and requires 5 V. V_{CC} and V_{EE} power the remaining portions of the circuitry and require +12 V to +15 V and −12 V to −15 V, respectively. V_{CC} and V_{EE} must also be a minimum of 2 V greater than the maximum reference and output voltages anticipated.

Decoupling capacitors are used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins. V_{LL} is bypassed to digital ground. V_{CC} and V_{EE} are decoupled to analog ground.

DRIVING THE REFERENCE INPUT

The reference input of the AD664 can have an impedance as low as 1.3 kΩ. The external reference voltage must be able to source up to 7.7 mA of load current. Suitable choices include the 5 V AD586 and the 10 V AD587.

The architecture of the AD664 derives an inverted version of the reference voltage for some portions of the internal circuitry. This means that the power supplies must be at least 2 V greater than both the external reference and the inverted external reference.

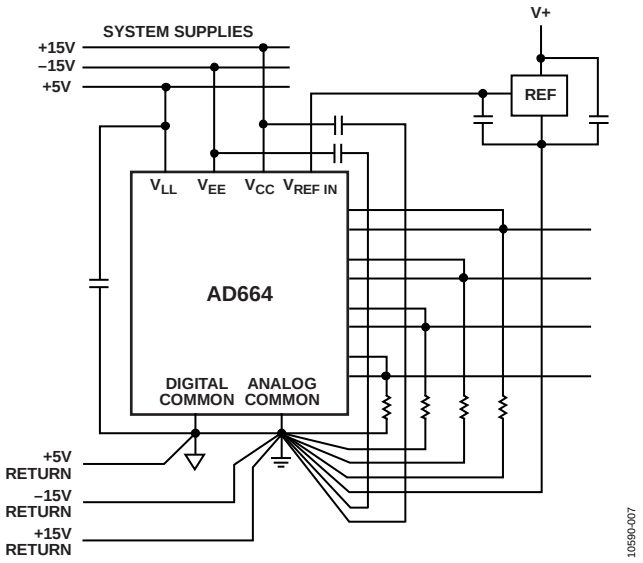


Figure 8. Recommended Circuit Schematic

OUTPUT CONSIDERATIONS

Each DAC output can source or sink 5 mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40 mA. Load capacitance of up to 500 pF is accommodated with no effect on stability. When an application requires additional output current, a current boosting element is inserted into the output loop with no sacrifice in accuracy. Figure 9 details this method.

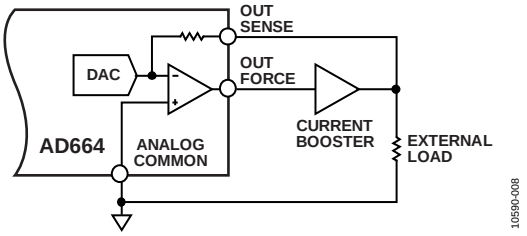


Figure 9. Current Boosting Scheme

Maximum AD664 output voltage settling time is 10 µs. Figure 10 shows the output voltage settling time with a fixed 10 V reference, gain = 1, and all bits switched from 1 to 0.

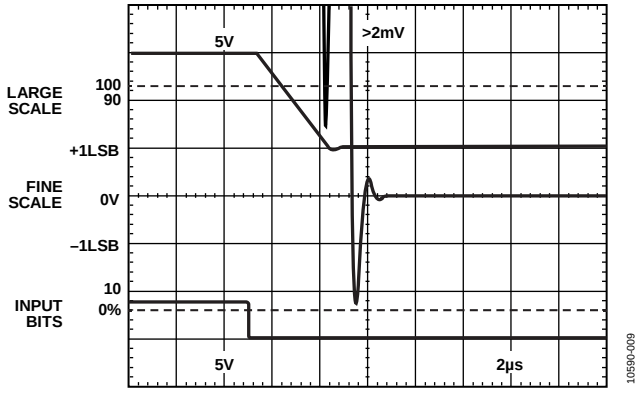


Figure 10. Settling Time, All Bits Switched from 1 to 0

Alternately, Figure 11 shows the settling characteristics when the reference is switched and the input bits remain fixed. In this case, all bits are on, the gain is 1, and the reference is switched from −5 V to +5 V.

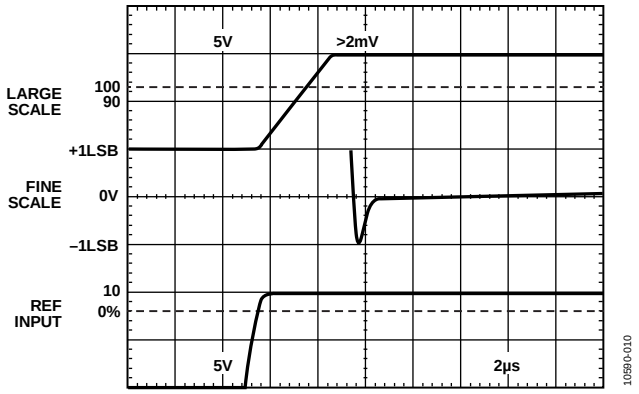


Figure 11. Settling Time, Input Bits Fixed, Reference Switched

MULTIPLYING MODE PERFORMANCE

Figure 12 illustrates the typical open-loop gain and phase performance of the output amplifiers of the AD664.

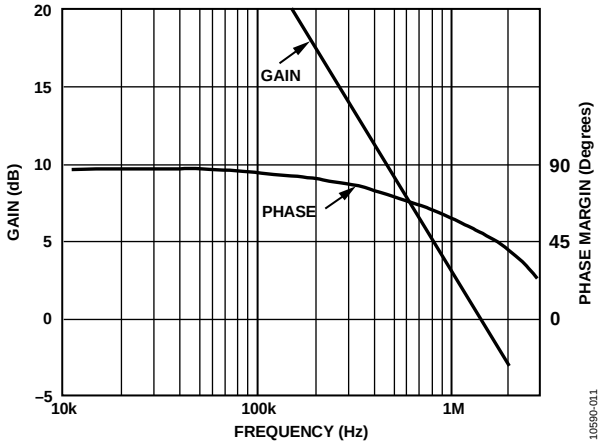


Figure 12. Gain and Phase Performance of AD664 Outputs

CROSSTALK

Crosstalk is a spurious signal on one DAC output caused by a change in the output of one or more of the other DACs.

Crosstalk is induced by capacitive, thermal, or load current induced feedthrough. Figure 13 shows typical crosstalk. DAC B is set to output 0 V. The outputs of DAC A, DAC C, and DAC D switch 2 kΩ loads from 10 V to 0 V. The first disturbance in the output of DAC B is caused by digital feedthrough from the input data lows. The second disturbance is caused by analog feedthrough from the other DAC outputs.

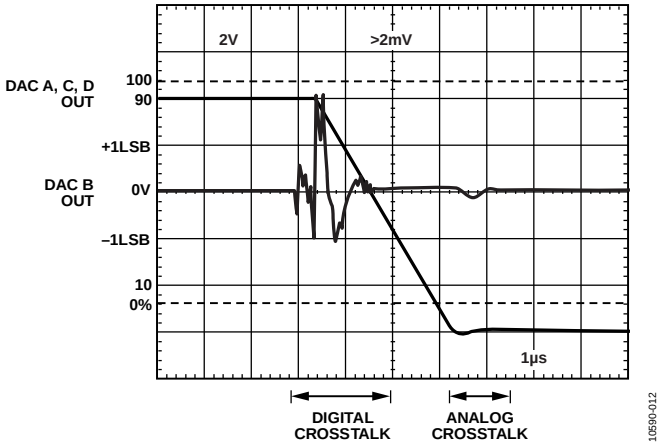


Figure 13. Output Crosstalk

OUTPUT NOISE

Wideband output noise is shown in Figure 14. This measurement was made with a 7 MHz noise bandwidth, gain = 1, and all bits on. The total rms noise is approximately 1/5 the visual peak-to-peak noise.

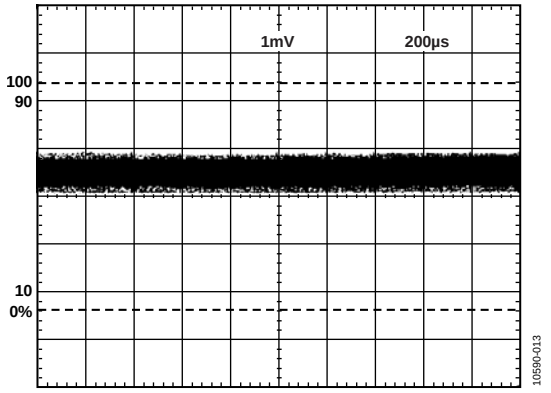


Figure 14. Typical Output Noise

DIGITAL INTERFACE

As Table 6 shows, the AD664 makes a wide variety of operating modes available to the user. These modes are accessed or programmed through the high speed digital port of the quad DAC. On-board registers program and store the DAC input codes and the DAC operating mode data. All registers are double buffered to allow for simultaneous updating of all outputs. Register data may be read back to verify the respective contents. The digital port also allows transparent operation. Data from the input pins is sent directly through both ranks of latches to the DAC.

Partial address decoding is performed by the DS0, DS1, $\overline{QS0}$, $\overline{QS1}$, and $\overline{QS2}$ address bits. $\overline{QS0}$, $\overline{QS1}$, and $\overline{QS2}$ allow the 44-lead versions (JLCC and PLCC) and the 44-terminal version (LCC) of the AD664 to be addressed in 4-bit nibble, 8-bit byte or 12-bit parallel words.

The $\overline{RST}$ pin provides a simple method to reset all output voltages to 0. Its advantages are speed and low software overhead.

Table 6. Digital Truth Table[1]

Function	DS1, DS0	$\overline{LS}$	$\overline{MS}$	$\overline{TR}$	$\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$[2]	$\overline{RD}$	$\overline{CS}$	$\overline{RST}$
Load First Rank (Data)								
DACA	00	0	1	1	Select quad	1	1 to 0	1
DACB	01	0	1	1	Select quad	1	1 to 0	1
DACC	10	0	1	1	Select quad	1	1 to 0	1
DACD	11	0	1	1	Select quad	1	1 to 0	1
Load Second Rank (Data)	X	1	1	1	X	1	1 to 0	1
Readback Second Rank (Data)	Select DAC	X	1	1	Select quad	0	1 to 0	1
Reset	X	X	X	X	X	X	X	0
Transparent[2]								
All DACs	X	1	1	0	000	1	1 to 0	1
DACA	00	0	1	0	000	1	1 to 0	1
DACB	01	0	1	0	000	1	1 to 0	1
DACC	10	0	1	0	000	1	1 to 0	1
DACD	11	0	1	0	000	1	1 to 0	1
Mode Select[2, 3]								
First Rank	X	0	0	1	00X	1	1 to 0	
Second Rank	X	1	0	1	X	1	1 to 0	1
Readback Mode[2]	X	X	0	1	00X	0	1 to 0	1
Update Second Rank and Mode	X	1	0	0	X	1	1 to 0	1

[1] X means don't care.
[2] For 44-lead versions (JLCC and PLCC) and 44-terminal version (LCC) only. Allow the AD664 to be addressed in 4-bit nibble, 8-bit byte, or 12-bit parallel words.
[3] For $\overline{MS}$, $\overline{TR}$, $\overline{LS}$ = 0, an $\overline{MS}$ first write occurs.

INPUT DATA

In general, two types of data are input to the registers of the AD664, input code data, and mode select data. Input code data sets the DAC inputs while the mode select data sets the gain and range of each DAC.

The versatile I/O port of the AD664 allows many different types of data input schemes. For example, the input code for just one of the DACs may be loaded and the output may or may not be updated. Alternatively, the input codes for all four DACs may be written, and the outputs may or may not be updated.

The same applies for mode selection. The mode of just one or many of the DACs may be rewritten and the user can choose to immediately update the outputs or wait until a later time to transfer the mode information to the outputs.

A user may also write both input code and mode information into their respective first ranks and then update all second ranks at once.

Finally, transparent operation allows data to be transferred from the inputs to the outputs using a single control line. This feature is useful, for example, in a situation where one of the DACs is used in an analog-to-digital converter (ADC). The successive approximation register (SAR) ADC is connected directly to a DAC by using the transparent mode of operation. Another use for this feature is during system calibration where the endpoints of the transfer function of each DAC is measured. For example, if the full-scale voltages of each DAC are measured, then by making all four DACs transparent and putting all ones on the input port, all four DACs are full-scale. This requires far less software overhead than loading each register individually.

TIMING REQUIREMENTS

The following sections detail the timing requirements for various data loading schemes. All of the timing specifications shown assume V_{IH} = +2.4 V, V_{IL} = +0.4 V, V_{CC} = +15 V, V_{EE} = −15 V, and V_{LL} = +5 V.

LOAD AND UPDATE ONE DAC OUTPUT

In this first example, the object is simply to change the output of one of the four DACs on the AD664 chip. The procedure is to select the address bits that indicate the DAC to be programmed, pull latch select ($\overline{LS}$) low, pull chip select ($\overline{CS}$) low, release $\overline{LS}$ and then release $\overline{CS}$. When $\overline{CS}$ goes low, data enters the first rank of the input latch. As soon as $\overline{LS}$ goes high, the data is transferred into the second rank and produces the new output voltage. During this transfer, mode select ($\overline{MS}$), transparent ($\overline{TR}$), readback ($\overline{RD}$), and reset ($\overline{RST}$) are held high.

PRELOADING THE FIRST RANK OF ONE DAC

In this case, the object is to load new data into the first rank of one of the DACs but not the output. As in the previous case, the address and data inputs are placed on the appropriate pins, $\overline{LS}$ is brought to 0, and $\overline{CS}$ is asserted. Note that in this situation, $\overline{CS}$ goes high before $\overline{LS}$ goes high. The input data is prevented from getting to the second rank and affecting the output voltage.

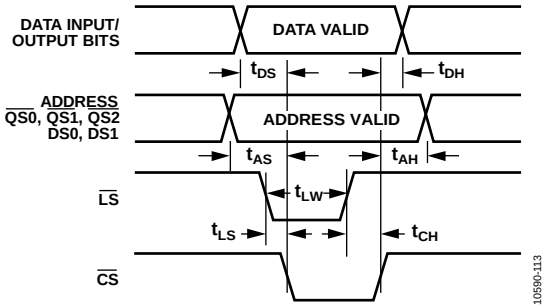


Figure 15. Update Output of a Single DAC

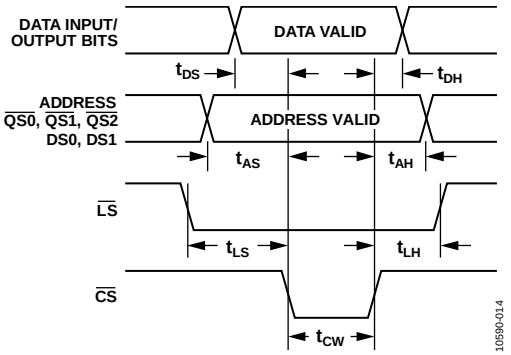


Figure 16. Preload First Rank of a DAC

This method shown in Figure 16 allows the user to preload the data to a DAC and strobe it into the output latch, which can be done by reproducing the sequence of signals illustrated in the Update Second Rank of a DAC section.

Table 7. Update Output of a Single DAC Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
$\overline{LS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{LS}[1])	0	0
Data Transition to $\overline{CS}$ Falling Edge (t_{DS})	0	0
$\overline{CS}$ Rising Edge to Data Transition (t_{DH})	0	0
$\overline{LS}$ Low Time (t_{LW})	60	80
$\overline{LS}$ Rising Edge to $\overline{CS}$ Rising Edge (t_{CH})	30	50
Address Transition to $\overline{CS}$ Falling Edge (t_{AS})	0	0
$\overline{CS}$ Rising Edge to Address Transition (t_{AH})	0	0

[1] For $t_{LS} > 0$, the width of $\overline{LS}$ must be increased by the same amount that t_{LS} is greater than 0 ns.

Table 8. Preload First Rank of a DAC Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
$\overline{LS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{LS})	0	0
$\overline{CS}$ Rising Edge to $\overline{LS}$ Rising Edge (t_{LH})	15	15
$\overline{CS}$ Low Time (t_{CW})	80	100
Data Transition to $\overline{CS}$ Falling Edge (t_{DS})	0	0
$\overline{CS}$ Rising Edge to Data Transition (t_{DH})	15	15
Address Transition to $\overline{CS}$ Falling Edge (t_{AS})	0	0
$\overline{CS}$ Rising Edge to Address Transition (t_{AH})	15	15

UPDATE SECOND RANK OF A DAC

Assuming that a new input code had previously been placed into the first rank of the input latches, the user can update the output of the DAC by simply pulling $\overline{CS}$ low while keeping $\overline{LS}$, $\overline{MS}$, $\overline{TR}$, $\overline{RD}$, and $\overline{RST}$ high. Address data is not needed in this case. All second ranks are updated by this procedure, but only the second ranks that receive data differently from the data that was originally there manifest a change. Updating the second rank does not change the contents of the first rank.

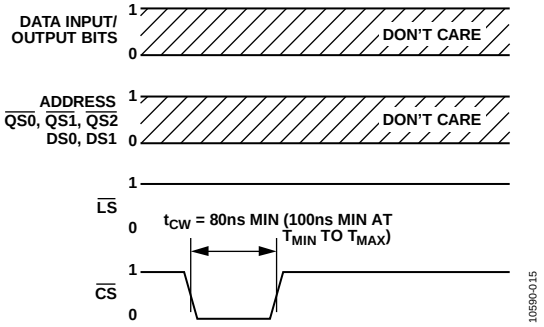


Figure 17. Update Second Rank of a DAC

The same options that exist for individual DAC input loading also exist for multiple DAC input loading. That is, the user can choose to update the first and second ranks of the registers or preload the first ranks and then update them at a future time.

PRELOAD MULTIPLE FIRST RANK REGISTERS

The first ranks of the DAC input registers may be preloaded with new input data without disturbing the second rank data. This is done by transferring the data into the first rank by bringing $\overline{CS}$ low while $\overline{LS}$ is low. $\overline{CS}$ must return high before $\overline{LS}$. This prevents the data from the first rank from getting into the second rank. A simple second rank update cycle as shown in Figure 17 moves the preloaded information to the DACs.

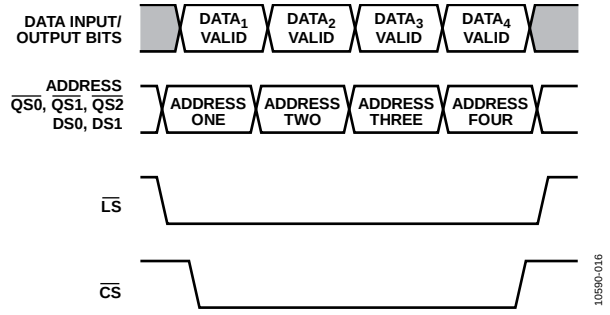


Figure 18. Preload First Rank Registers

LOAD AND UPDATE MULTIPLE DAC OUTPUTS

The following examples demonstrate two ways to update all DAC outputs. The first method involves doing all data transfers during one long $\overline{CS}$ low period. Note that in this case, shown in Figure 19, $\overline{LS}$ returns high before $\overline{CS}$ goes high. Data hold time, relative to an address change, is 70 ns. This updates the outputs of all DACs simultaneously.

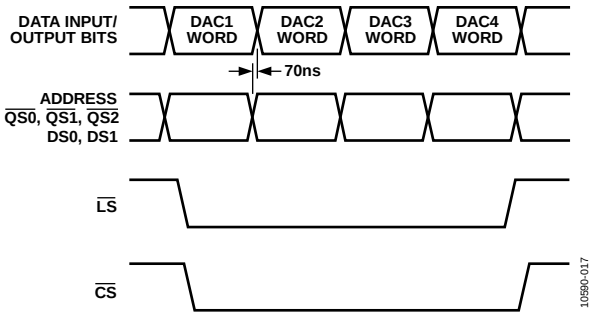


Figure 19. Update All DAC Outputs

The second method involves doing a $\overline{CS}$ assertion (low) and an $\overline{LS}$ toggle separately for each DAC. This method is a series of preload operations (Figure 16 and Table 8). In this case, illustrated in Figure 20, two $\overline{LS}$ signals are shown. One, labeled $\overline{LS}$, goes high before $\overline{CS}$ returns high. This transfers the new input word to the DAC outputs sequentially. The second $\overline{LS}$ signal, labeled alternate $\overline{LS}$, stays low until $\overline{CS}$ returns high. Using this sequence loads the first ranks with each new input word but does not update the DAC outputs. Then, to update all DAC outputs simultaneously requires the signals illustrated in Figure 17.

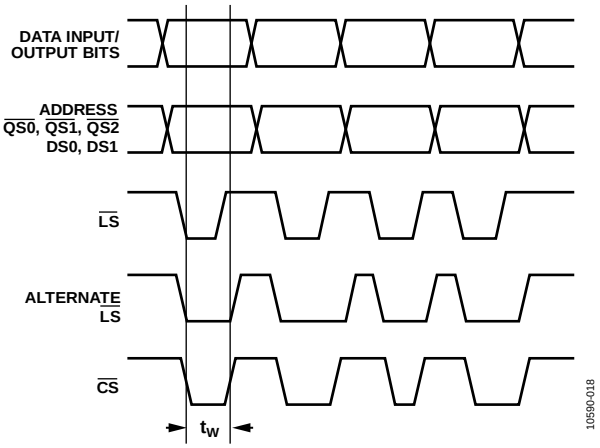


Figure 20. Load and Update Multiple DACs

SELECTING GAIN RANGE AND MODES (44-LEAD VERSIONS (JLCC AND PLCC) AND 44-TERMINAL VERSION (LCC))

The mode select feature of the AD664 allows a user to configure the gain ranges and output modes of each of the four DACs.

On-board switches take the place of up to eight external relays that are normally required to accomplish this task. The switches are programmed by the mode select word entered via the data I/O port. The mode select word is 8-bits wide and occupies the topmost eight bits of the input word. The last four bits of the input word are don't care bits.

Figure 21 shows the format of the mode select word. The first four bits determine the gain range of the DAC. When set to be a gain of 1, the output of the DAC spans a voltage of one times the reference. When set to a gain of 2, the output of the DAC spans a voltage of two times the reference.

The next four bits determine the mode of the DAC. When set to UNI, the output goes from 0 V to V_{REFIN}, or 0 V to 2 V V_{REFIN}. When the BIP mode is selected, the output goes from − V_{REFIN}/2 to V_{REFIN}/2 or − V_{REFIN} to V_{REFIN}.

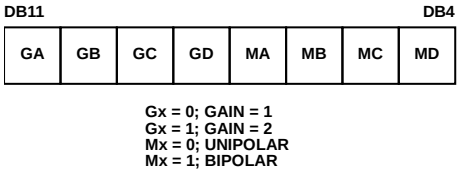


Figure 21. Mode Select Word Format

LOAD AND UPDATE MODE OF ONE DAC

In this next example, the object is to load new mode information for one of the DACs into the first rank of latches and then immediately update the second rank. This mode is done by putting the new mode information (8-bit word length) onto the data bus. Then $\overline{MS}$ and $\overline{LS}$ are pulled low. Following the $\overline{MS}$ and $\overline{LS}$ being pulled low, $\overline{CS}$ is pulled low. This loads the mode information into the first rank of latches. $\overline{LS}$ is then brought high. This action updates the second rank of latches (and the DAC outputs). The load cycle ends when $\overline{CS}$ is brought high.

In reality, this load cycle really updates the modes of all the DACs, but the effect is to only change the modes of those DACs whose mode select information has actually changed.

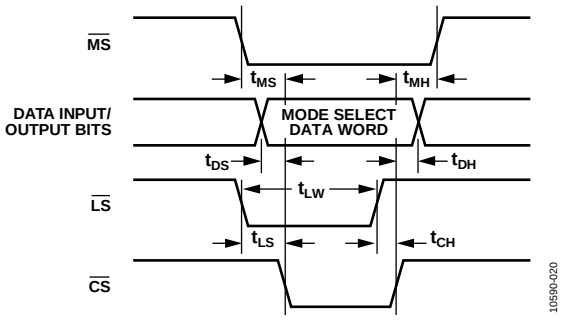


Figure 22. Load and Update Mode of One DAC

Table 9. Load and Update Mode of One DAC Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
$\overline{MS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{MS})	0	0
$\overline{LS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{LS}[1])	0	0
Data Transition to $\overline{CS}$ Falling Edge (t_{DS})	0	0
$\overline{LS}$ Low Time (t_{LW})	60	70
$\overline{LS}$ Rising Edge to $\overline{CS}$ Rising Edge (t_{CH})	70	80
$\overline{CS}$ Rising Edge to Data Transition (t_{DH})	0	0
$\overline{CS}$ Rising Edge to $\overline{MS}$ Rising Edge (t_{MH})	0	0

[1] For $t_{LS} > 0$, the width of $\overline{LS}$ must be increased by the same amount that t_{LS} is greater than 0 ns.

PRELOADING THE MODE SELECT REGISTER

Mode data is written into the first rank of the mode select latch without changing the modes currently being used. This feature is useful when a user wants to preload new mode information in anticipation of strobing it in at a future time. Figure 23 and Table 10 illustrate the correct sequence and timing of control signals to accomplish this task, which allows the user to preload the data to a DAC and strobe it into the output latch at some future time. The user can do this by reproducing the sequence of signals illustrated in Figure 24 and Table 11.

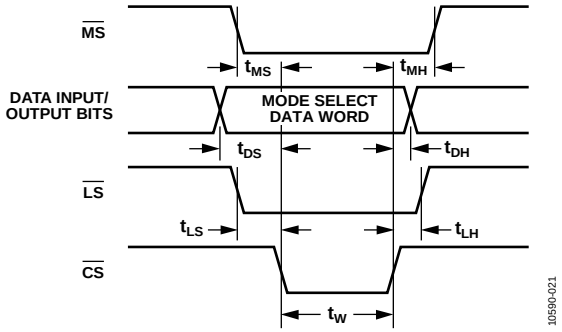


Figure 23. Preload Mode Select Register

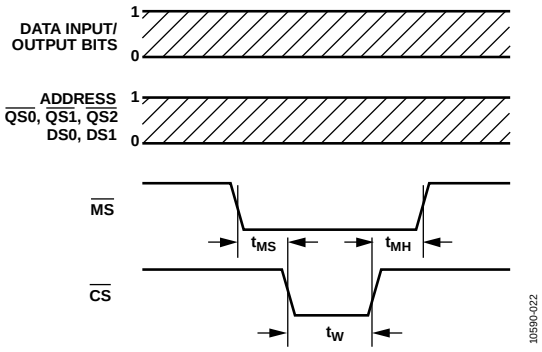


Figure 24. Update Second Rank of Mode Select Latch

Table 10. Preload Mode Select Register Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
$\overline{CS}$ Rising Edge to $\overline{MS}$ Rising Edge (t_{MH})	15	15
$\overline{MS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{MS})	0	0
$\overline{LS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{LS})	0	0
Data Transition to $\overline{CS}$ Falling Edge (t_{DS})	0	0
$\overline{CS}$ Low Time (t_W)	80	100
$\overline{CS}$ Rising Edge to $\overline{LS}$ Rising Edge (t_{LH})	15	15
$\overline{CS}$ Rising Edge to Data Transition (t_{DH})	15	15

Table 11. Update Second Rank of Mode Select Latch Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
$\overline{MS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{MS})	0	0
$\overline{CS}$ Rising Edge to $\overline{MS}$ Rising Edge (t_{MH})	0	0
$\overline{CS}$ Low Time (t_W)	80	100

TRANSPARENT OPERATION (44-LEAD VERSIONS (JLCC AND PLCC) AND 44-TERMINAL VERSION (LCC))

Transparent operation allows data from the inputs of the AD664 to be transferred into the DAC registers without the intervening step of being latched into the first rank of latches. Two modes of transparent operation exist, the partially transparent mode and a fully transparent mode. In the partially transparent mode, one of the DACs is transparent, while the remaining three continue to use the data latched into their respective input registers. Both modes require a 12-bit wide input word.

Fully transparent operation is a simultaneous load of data from Figure 15, in which replacing $\overline{LS}$ with $\overline{TR}$ causes all four DACs to be loaded at once.

The fully transparent mode is achieved by asserting lows on $\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$, $\overline{TR}$, and $\overline{CS}$ while keeping $\overline{LS}$ high, in addition to $\overline{MS}$ and $\overline{RD}$. Figure 25 illustrates the necessary timing relationships. Fully transparent operation also works with $\overline{TR}$ tied low (enabled).

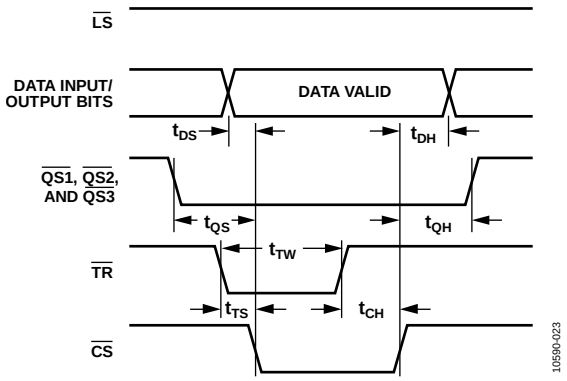


Figure 25. Fully Transparent Mode

Partially transparent operation is preloading the first rank in Figure 16 without requiring the additional $\overline{CS}$ pulse from Figure 17.

The partially transparent mode is achieved by setting $\overline{CS}$, $\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$, $\overline{LS}$, and $\overline{TR}$ low while keeping $\overline{RD}$ and $\overline{MS}$ high. The address of the transparent DAC is asserted on DS0 and DS1. Figure 26 illustrates the necessary timing relationships. Partially transparent operation also works with $\overline{TR}$ tied low (enabled).

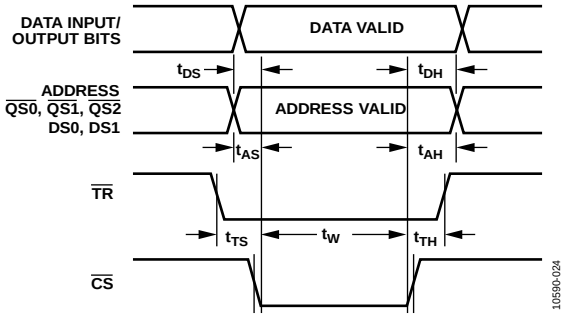


Figure 26. Partially Transparent

Table 12. Fully Transparent Mode Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
Data Transition to $\overline{CS}$ Falling Edge (t_{DS})	0	0
$\overline{QS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{QS})	0	0
$\overline{TR}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{TS}[1])	0	0
$\overline{TR}$ Low Time (t_{TW})	80	90
$\overline{TR}$ Rising Edge to $\overline{CS}$ Rising Edge (t_{CH})	90	110
$\overline{CS}$ Rising Edge to Data Transition (t_{DH})	0	0
$\overline{CS}$ Rising Edge to $\overline{QS}$ Rising Edge (t_{QH})	0	0

[1] For $t_{TS} > 0$, the width of $\overline{TR}$ must be increased by the same amount that t_{TS} is greater than 0 ns.

Table 13. Partially Transparent Mode Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
Data Transition to $\overline{CS}$ Falling Edge (t_{DS})	0	0
Address Transition to $\overline{CS}$ Falling Edge (t_{AS})	0	0
$\overline{TR}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{TS})	0	0
$\overline{CS}$ Low Time (t_W)	90	110
$\overline{CS}$ Rising Edge to Data Transition (t_{DH})	15	15
$\overline{CS}$ Rising Edge to Address Transition (t_{AH})	15	15
$\overline{CS}$ Rising Edge to $\overline{TR}$ Rising Edge (t_{TH})	15	15

OUTPUT DATA

Two types of outputs may be obtained from the internal data registers of the AD664 chip, mode select, and DAC input code data. Readback data may be in the same forms in which it is entered, namely, 4-bit, 8-bit, and 12-bit wide words (12 bits only for 28-lead versions).

DAC DATA READBACK

DAC input code readback data is obtained by setting the address of the DAC (DS0, DS1) and the quads ($\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$) on the address pins and bringing the $\overline{RD}$ and $\overline{CS}$ pins low. The timing diagram for a DAC code readback operation appears in Figure 27 and Table 14.

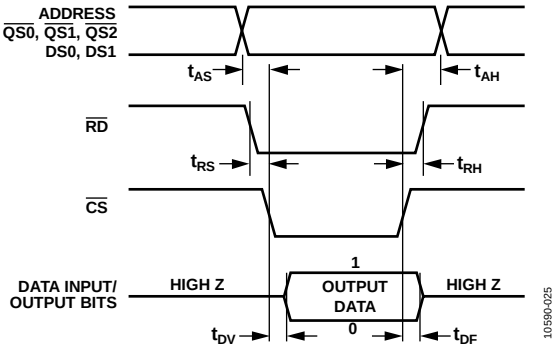


Figure 27. DAC Input Code Readback

MODE DATA READBACK

Mode data is read back in a similar fashion. By setting $\overline{MS}$, $\overline{QS0}$, $\overline{QS1}$, $\overline{RD}$, and $\overline{CS}$ low while setting $\overline{TR}$ and $\overline{RST}$ high, the mode select word is presented to the I/O port pins. Figure 28 and Table 15 show the timing diagram for a readback of the mode select data register.

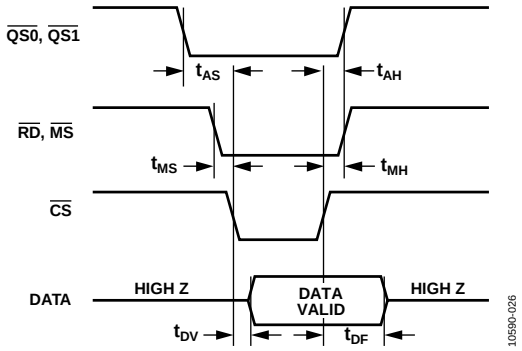


Figure 28. Mode Data Readback

Table 14. DAC Input Code Readback Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
Address Transition to $\overline{CS}$ Falling Edge (t_{AS})	0	0
$\overline{RD}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{RS})	0	0
$\overline{CS}$ Falling Edge to Data Transition (t_{DV})	150	180
$\overline{CS}$ Rising Edge to Data Transition (t_{DF})	60	75
$\overline{CS}$ Rising Edge to Address Transition (t_{AH})	0	0
$\overline{CS}$ Rising Edge to $\overline{RD}$ Rising Edge (t_{RH})	0	0

Table 15. DAC Mode Readback Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
$\overline{QS0}$, $\overline{QS1}$ to $\overline{CS}$ Falling Edge (t_{AS})	0	0
$\overline{RD}$, $\overline{MS}$ Falling Edge to $\overline{CS}$ Falling Edge (t_{MS})	0	0
$\overline{CS}$ Falling Edge to Data Transition (t_{DV})	150	180
$\overline{CS}$ Rising Edge to Data Transition (t_{DF})	60	75
$\overline{CS}$ Rising Edge to $\overline{QS0}$, $\overline{QS1}$ Rising Edge (t_{AH})	0	0
$\overline{CS}$ Rising Edge to $\overline{RD}$, $\overline{MS}$ Rising Edge (t_{MH})	0	0

OUTPUT LOADS

Readback timing is tested with the output loads shown in Figure 29.

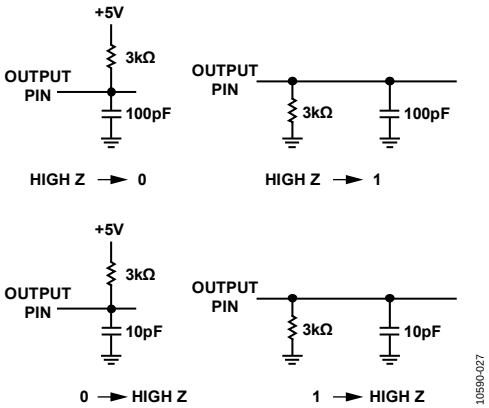


Figure 29. Output Loads

ASYNCHRONOUS RESET OPERATION

The asynchronous reset signal shown in Figure 30 and Table 16 may be asserted at any time. A minimum pulse width (t_{RW}) of 90 ns is required. The reset feature is designed to return all DAC outputs to 0 V, regardless of the mode or range selected. In the 44-lead versions (JLCC and PLCC) and the 44-terminal version (LCC), the modes are reset to UNI 10 V span (gain of 1), and the input codes are rewritten to be zeros. Previous DAC code and mode information is erased.

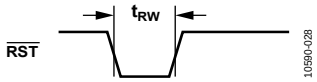


Figure 30. Asynchronous Reset Operation

In the 28-lead versions of the AD664, the mode remains unchanged. The appropriate input code is rewritten to reset the output voltage to 0 V. As in the 44-lead versions (JLCC and PLCC) and the 44-terminal version (LCC), the previous input data is erased.

At power-up, an AD664 may be activated in either the read or write modes. While at the device level this event does not produce any problems, at the system level, it may produce problems. Analog Devices recommends the addition of a simple power-on reset scheme to any system where the possibility of an unknown start-up state is a problem. The simplest version of this scheme is illustrated in Figure 31.

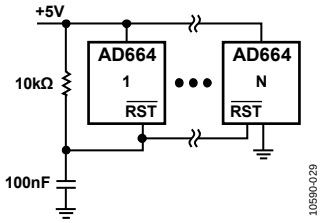


Figure 31. Power-On Reset

Figure 31 shows that the scheme is only appropriate for systems in which the $\overline{RST}$ is otherwise not used. To use the $\overline{RST}$ pin, an additional logic gate may be included to combine the power-on reset with the reset signal.

Table 16. Asynchronous Reset Operation Timing

Parameter	25°C Minimum (ns)	T_{MIN} to T_{MAX} Minimum (ns)
Pulse Width (t_{RW})	80	100

INTERFACING THE AD664 TO MICROPROCESSORS

The AD664 is easy to interface with a wide variety of popular microprocessors. Common architectures include processors with dedicated 8-bit data and address buses, an 8-bit bus over which data and address are multiplexed, an 8-bit data and 16-bit address partially muxed, and separate 16-bit data and address buses.

AD664 addressing is accomplished through either memory mapped or I/O techniques. In memory mapped schemes, the AD664 appears to the host microprocessor as random access memory (RAM). Standard memory addressing techniques are used to select the AD664. In the I/O schemes, the AD664 is treated as an external I/O device by the host. Dedicated I/O pins are used to address the AD664.

MC6801 INTERFACE

Figure 32 to Figure 35 illustrate a few of the various methods that are used to connect the AD664 to the Motorola MC6801 microprocessor. In each of these cases, the MC6801 is intended to be configured in its expanded, nonmultiplexed mode of operation. In this mode, the MC6801 can address 256 bytes of external memory over 8-bit data (Port 3) and 8-bit address (Port 4) buses. Eight general-purpose I/O lines (Port 1) are also available. On-board RAM and read-only memory (ROM) provide program and data storage space.

In Figure 32, the three least significant address bits (P40, P41, and P42) are employed to select the appropriate on-chip addresses for the various input registers of the AD664. Three I/O lines (P17, P16, and P15) are used to select various operating features of the AD664. The SC1 ($\overline{IOS}$) and E pins are combined to produce an appropriate $\overline{CS}$ signal. This addressing scheme leaves the five most significant address bits and five I/O lines free for other tasks in the system.

Figure 33 shows another way to interface an AD664 to the MC6801. Here, the six least significant address lines select AD664 features and registers. This interface configuration is a purely memory mapped scheme while the one illustrated in Figure 32 uses some memory mapping as well as some dedicated I/O pins. In Figure 33, two address lines and all eight I/O lines remain free for other system tasks.

Expansion of the scheme employed in Figure 32 results in that shown in Figure 34. Here, two AD664s are connected to an MC6801, providing a total of eight 12-bit, software programmable DACs. Again, the three LSBs of the address are used to select the on-chip registers of the AD664. The SC1 ($\overline{IOS}$) and E pins, as well as a fourth address bit, are decoded to provide the appropriate $\overline{CS}$ signals. Four address and five I/O lines remain uncommitted.

A slightly more sophisticated approach to system expansion is illustrated in Figure 35. Here, a 74LS138 (1-of-8 decoder) is used to address one of the eight AD664s connected to the MC6801. The three least significant address bits are used to select on-chip register and DAC. The next three address bits are used to select the appropriate AD664. The SC1 ($\overline{IOS}$) and E pins gate the 74LS138 output.

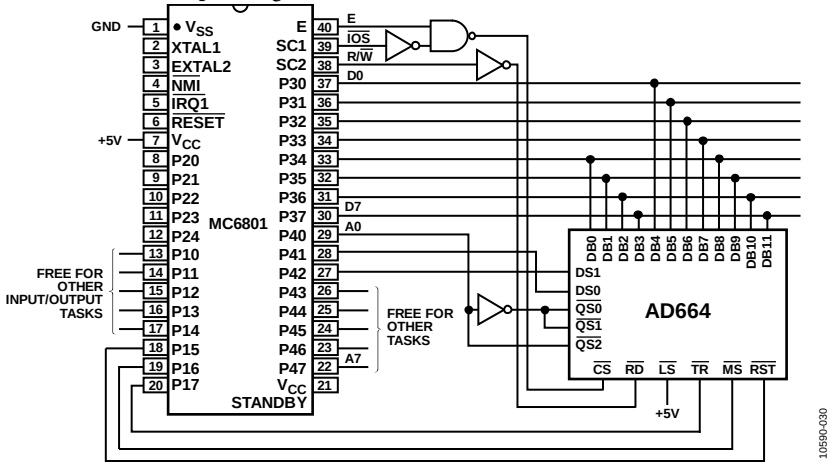


Figure 32. Simple AD664 to MC6801 Interface

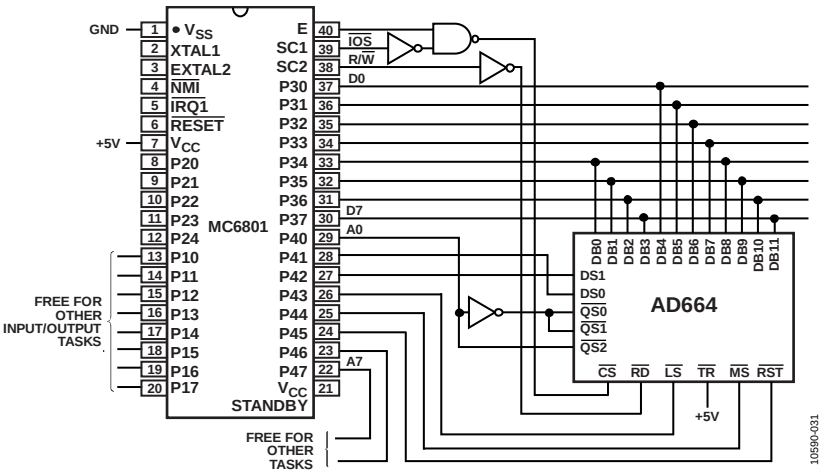


Figure 33. Alternate AD664 to MC6801 Interface

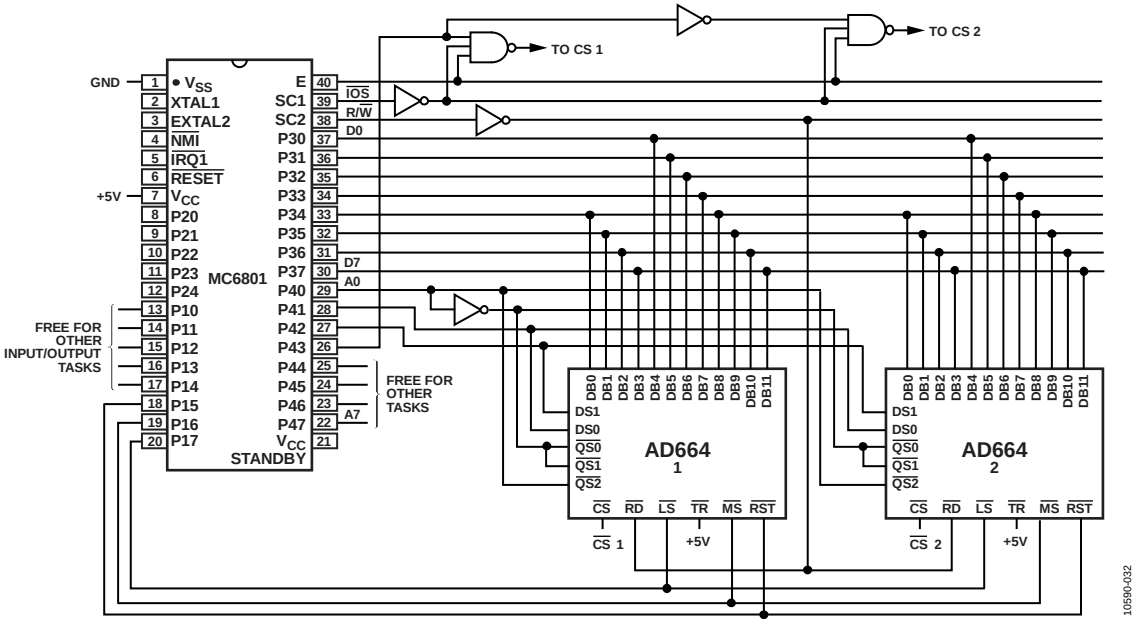


Figure 34. Interfacing Two AD664s to an MC6801

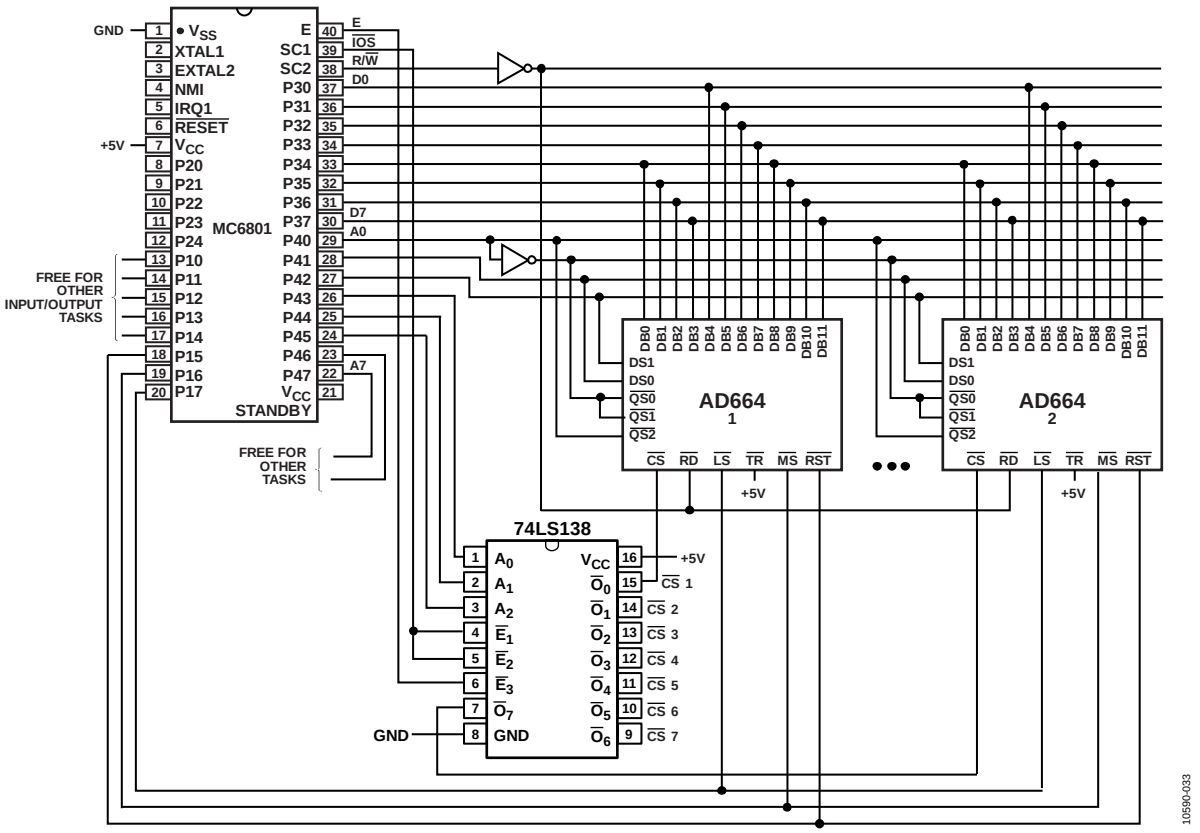


Figure 35. Interfacing Eight AD664s to an MC6801 and a Motorola 74LS138

The schemes in Figure 32 to Figure 35 illustrate some of the trade-offs that a designer may make when configuring a system. For example, the designer may use I/O lines instead of address bits or vice versa. This decision may be influenced by other I/O tasks or system expansion requirements. The designer can also choose to implement only a subset of the features available. Perhaps the $\overline{RST}$ pin is not really needed. Tying that input pin to V_{LL} (+5V) frees up another I/O or address bit. The same consideration applies to mode select. In all of these cases, $\overline{TR}$ is shown tied to V_{LL} (+5V), because the MC6801 cannot provide the 12-bit wide input word required for the transparent mode. In situations where transparent operation is not required, and mode select is also not needed, the designer may consider specifying the dual in-line package (DIP) version of the device (either the UNI or the BIP version).

Each of the schemes illustrated in Figure 32 to Figure 35 operates with an MC6801 at clock rates up to and including 1.5 MHz. Similar schemes are derived for other 8-bit microprocessors and microcontrollers such as the 8051/8086/8088/6502. One such scheme developed for the 8051 and AD664 is illustrated in Figure 36.

8051 INTERFACE

Figure 36 shows the AD664 combined with an 8051 microcontroller chip. Three LSB addresses provide the quad and DAC select signals. Control signals from Port 1 select various operating modes such as readback, mode select, and reset as well as providing the $\overline{LS}$ signal. Read and write signals from the 8051 are decoded to provide the $\overline{CS}$ signal.

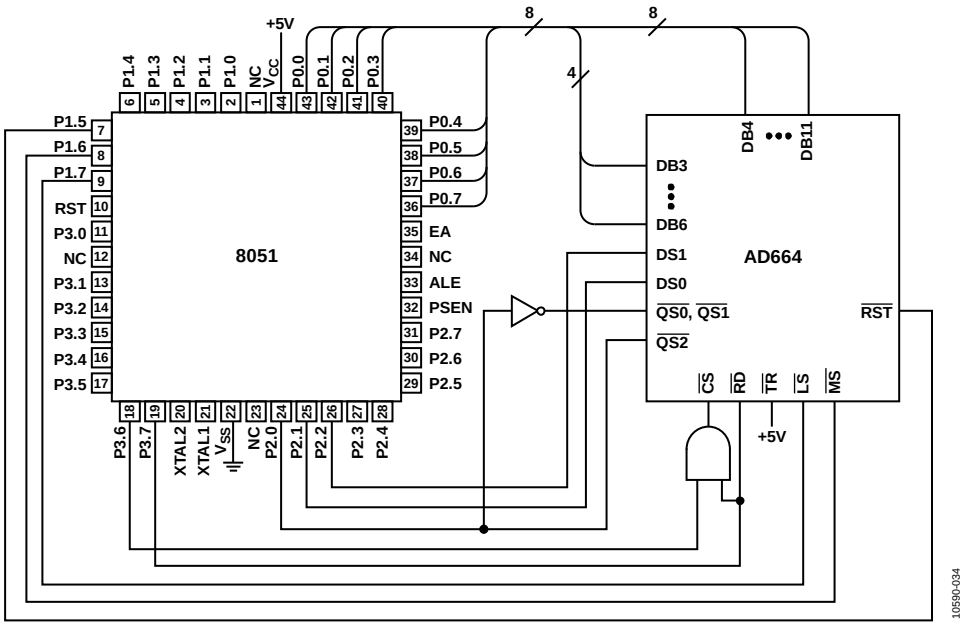


Figure 36. AD664 to 8051 Interface

IBM PC INTERFACE

Figure 37 illustrates a simple interface between an IBM® PC and an AD664. The three least significant address bits are used to select the quad and DAC. The next two address bits are used for $\overline{LS}$ and $\overline{MS}$. In this scheme, a 12-bit input word requires two load cycles, an 8-bit word, and a 4-bit word. Another write is required to transfer the word or words previously written to the second rank. A 12-bit wide word again requires at least two read cycles, namely, one for the eight MSBs and four for the LSBs. The page select signal produces a $\overline{CS}$ strobe for any address from 300 hexadecimal to 31F hexadecimal.

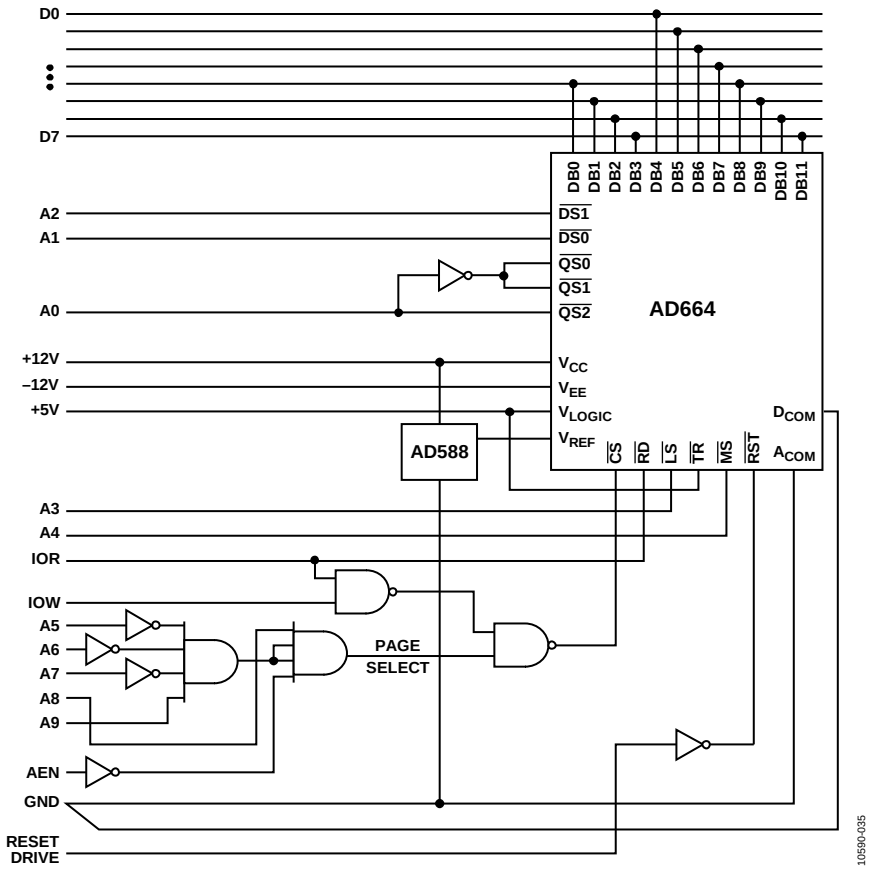


Figure 37. AD664 to IBM PC Interface

Table 17 details the memory locations and addresses used by this interface.

Table 17. IBM PC Memory Map

Hexadecimal	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Register Selected
300	1	1	0	0	0	0	0	0	0	0	Illegal address
301	1	1	0	0	0	0	0	0	0	1	Mode select, first rank
302	1	1	0	0	0	0	0	0	1	0	Illegal address
303	1	1	0	0	0	0	0	0	1	1	Mode select, first rank
304	1	1	0	0	0	0	0	1	0	0	Illegal address
305	1	1	0	0	0	0	0	1	0	1	Mode select, first rank
306	1	1	0	0	0	0	0	1	1	0	Illegal address
307	1	1	0	0	0	0	0	1	1	1	Mode select, first rank
308	1	1	0	0	0	0	1	0	0	0	Mode select, second rank
309[1]	1	1	0	0	0	0	1	0	0	1	Mode select, second rank
30A	1	1	0	0	0	0	1	0	1	0	Mode select, second rank
30B[1]	1	1	0	0	0	0	1	0	1	1	Mode select, second rank
30C	1	1	0	0	0	0	1	1	0	0	Mode select, second rank
30D[1]	1	1	0	0	0	0	1	1	0	1	Mode select, second rank
30E	1	1	0	0	0	0	1	1	1	0	Mode select, second rank
30F[1]	1	1	0	0	0	0	1	1	1	1	Mode select, second rank
310	1	1	0	0	0	1	0	0	0	0	DAC A, 4 LSBs, first rank
311	1	1	0	0	0	1	0	0	0	1	DAC A, 8 MSBs, first rank
312	1	1	0	0	0	1	0	0	1	0	DAC B, 4 LSBs, first rank
313	1	1	0	0	0	1	0	0	1	1	DAC B, 8 MSBs, first rank
314	1	1	0	0	0	1	0	1	0	0	DAC C, 4 LSBs, first rank
315	1	1	0	0	0	1	0	1	0	1	DAC C, 8 MSBs, first rank

Hexadecimal	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Register Selected
316	1	1	0	0	0	1	0	1	1	0	DAC D, 4 LSBs, first rank
317	1	1	0	0	0	1	0	1	1	1	DAC D, 8 MSBs, first rank
318[1]	1	1	0	0	0	1	1	0	0	0	Second rank
319[1]	1	1	0	0	0	1	1	0	0	1	Second rank
31A[1]	1	1	0	0	0	1	1	0	1	0	Second rank
31B[1]	1	1	0	0	0	1	1	0	1	1	Second rank
31C[1]	1	1	0	0	0	1	1	1	0	0	Second rank
31D[1]	1	1	0	0	0	1	1	1	0	1	Second rank
31E[1]	1	1	0	0	0	1	1	1	1	0	Second rank
31F[1]	1	1	0	0	0	1	1	1	1	1	Second rank

[1] Registers are readable.

The following IBM PC basic routine produces four output voltage ramps from one AD664. Line numbers 10 through 70 define the hardware addresses for the first and second ranks of DAC registers as well as the first and second ranks of the mode select register. Program variables are initialized in line numbers 110 through 130. Line number 170 writes 0s out to the first rank and, then, the second rank of the mode select register.

Line numbers 200 through 320 calculate output voltages. Finally, line numbers 410 through 450 update the first, then the second ranks of the DAC input registers. Hardware registers may be read with the INP instruction. For example, the contents of the DAC A register may be accessed with the following command: Line#A = INP(DACA).

```
5     REM----AD664 LISSAJOUS PATTERNS----
10    REM ---ASSIGN HARDWARE ADDRESSES---
20    DACA = 785
30    DACB = 787
40    DACC = 789
50    DACD = 791
60    DAC2ND = 792
70    MODE1 = 769: MODE2 = 776
80    REM
90    REM
100   REM ---INITIALIZE VARIABLES---
110   X = 0: Y1 = 128: Y2 = 64: Y3 = 32
120   CX = 1: CY1 = 1: CY2 = -1: CY3= 1
130   FX = 9: FY1 = 5: FY2 = 13: FY3 = 15
140   REM
150   REM
160   REM ---INITIALIZE MODES AND GAINS---
170   OUT MODE1,0: OUT MODE2,0
180   REM
190   REM
200   REM ---CALCULATE VARIABLES---
210   X = X + FX*CX
220   Y1 = Y1 + FY1*CY1
230   Y2 = Y2 + FY2*CY2
240   Y3 = Y3 + FY3*CY3
250   IF X > 255 THEN X = 255: CX = -1:
GOTO 270
260   IF X < 0 THEN X = 0: CX = 1
270   IF Y1 > 255 THEN Y1 = 255: CY1 = -1:
GOTO 290
280   IF Y1 < 0 THEN Y1 = 0: CY1 = 1
290   IF Y2 > 255 THEN Y2 = 255: CY2 = -1
GOTO 310
300   IF Y2 < 0 THEN Y2 = 0: CY2 = -1
310   IF Y3 > 255 THEN Y3 = 255: CY3 = -1:
GOTO 400
320   IF Y3 < 0 THEN Y3 = 0: CY3 = 1
330   REM
340   REM
400   REM ---SEND DAC DATA---
410   OUT DACA,X
420   OUT DACB,Y1
430   OUT DACC,Y2
440   OUT DACD,Y3
450   OUT DAC2ND,0
500   REM
510   REM
520   REM ---LOOP BACK---
530   GOTO 210
```

SIMPLE AD664 TO MC68000 INTERFACE

Figure 38 shows an AD664 connected to the NXP MC68000. In this memory mapped I/O scheme, the left justified data is written in one 12-bit input word. Four address bits are used to perform the on-chip DAC selection as well as the various operating features. The R/$\overline{W}$ signal controls the $\overline{RD}$ function and system reset controls $\overline{RST}$.

This scheme is converted to write right justified data by connecting the data inputs to data bits DB0 through DB11. Other options include controlling the $\overline{QS0}$, $\overline{QS1}$, and $\overline{QS2}$ pins with $\overline{UDS}$ and $\overline{LDS}$ to provide a way to write 8-bit input and read 8-bit output words.

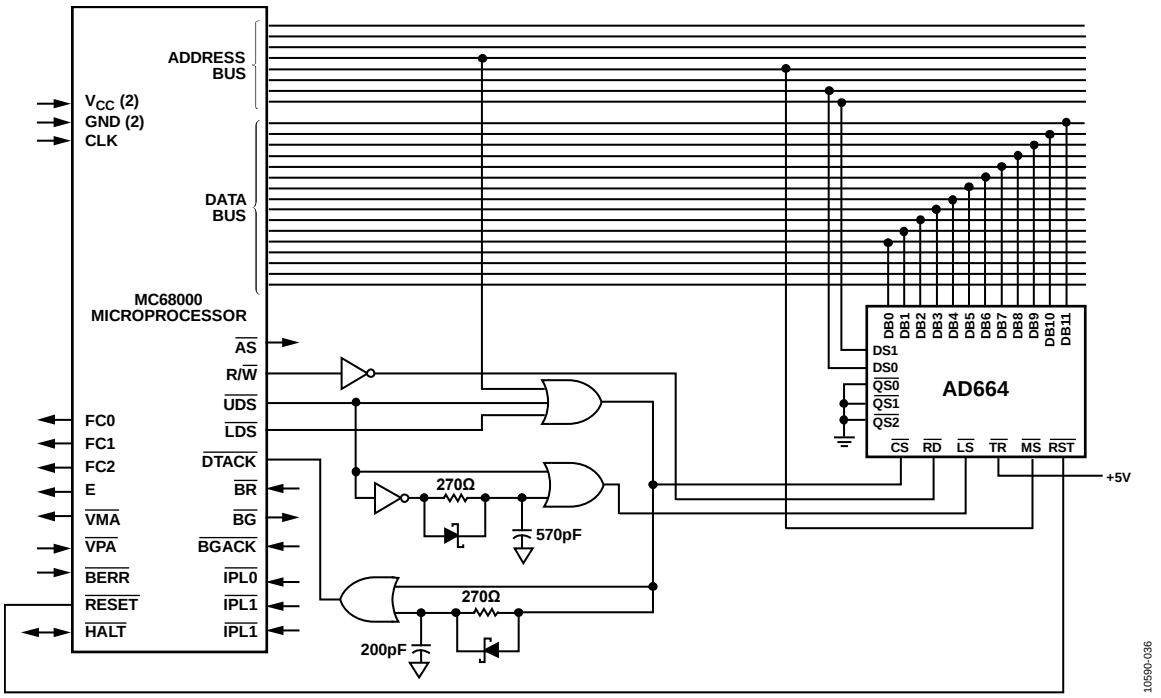


Figure 38. AD664 to MC68000 Interface

APPLICATIONS INFORMATION

TESTER PER PIN AUTOMATIC TEST EQUIPMENT (ATE) ARCHITECTURE

Figure 39 shows the AD664 used in a single channel of a digital test system. In this scheme, the AD664 supplies four individual output voltages. Two output voltages are provided to the V_{HIGH} and V_{LOW} inputs of the pin driver IC to set the digital output levels. Two others are routed to the inputs of the AD96687 dual comparator to supply reference levels of the readback features. This approach is replicated to give as many channels of stimulus or readback as the tester has pins. The AD664 is a particularly appropriate choice for a large scale system because the low power requirements (under 500 mW) ease power supply and cooling requirements. Analog ground currents of 600 µA or less make the ground current management task simpler. All DACs are driven from the same system reference and tracks over time and temperature. Finally, the small board area required by the AD664 (and AD96687) allows a high functional density.

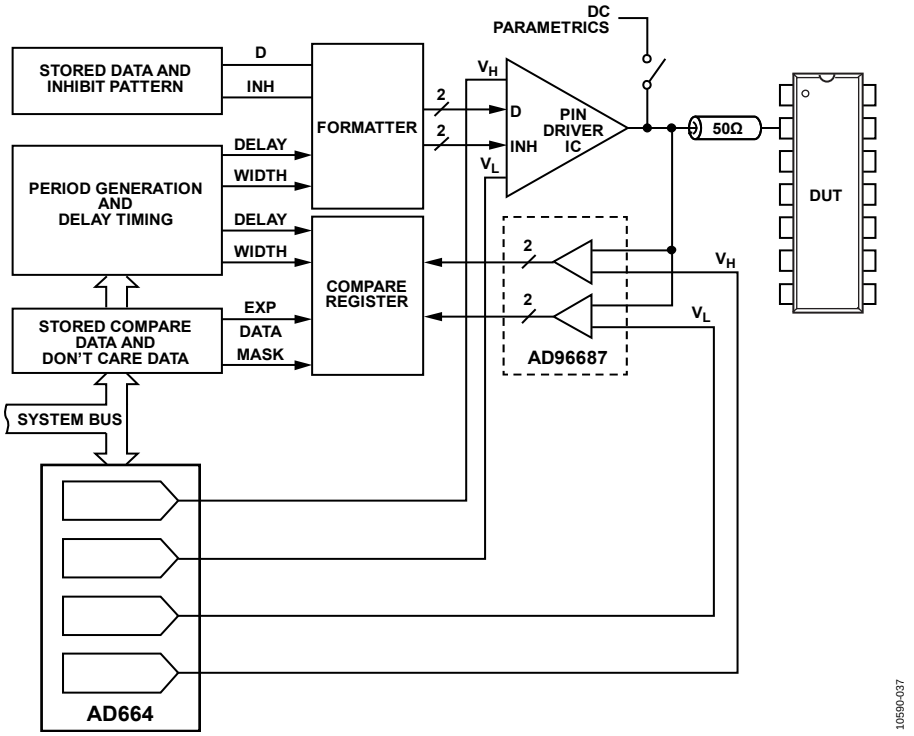


Figure 39. AD664 in Tester per Pin Architecture

X-AXIS AND Y-AXIS PLOTTERS

Figure 40 is a block diagram of the control section of a microprocessor controlled x-axis and y-axis pen plotter. In this conceptual exercise, two of the DACs are used for the X-channel drive and two are used for the Y-channel drive. Each DAC channel provides either the coarse or fine movement control for its respective channel. This approach offers increased resolution over some other approaches.

A designer can take advantage of the reset feature of the AD664 in the following manner. If the system is designed such that the home position of the pen (or galvanometer, beam, head, or similar mechanism) results when the outputs of all of the DACs are at zero, no system software is required to home the pen. A simple reset signal is sufficient.

Similarly, the transparent feature is used to the same end. One code is sent to all DACs at the same time to send the pen to the home position. Of course, this requires some software in which the previous example requires only a single reset strobe signal.

Drawing scaling is achieved by taking advantage of the software programmable gain settings of the AD664. If, for example, an A size drawing is created with gain settings of 1, a C size drawing is created by simply resetting all DAC gains to 2 and redrawing the object. Conversely, a C size drawing created with gains of 2 is reduced to an A size simply by changing the gains to 1 and redrawing. The same principal applies for conversion from B size to D size or D size to B size. The multiplying capability of the AD664 provides another scaling option. Changing the reference voltage provides a proportional change in drawing size. Inverting the reference voltage inverts the drawing.

Swapping digital input data from the X-channel to the Y-channel rotates the drawing 90°.

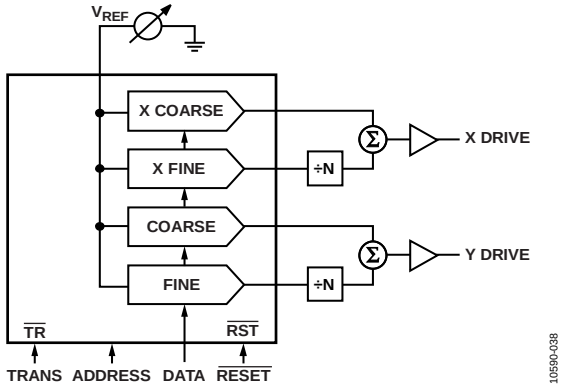


Figure 40. X-Axis and Y-Axis Plotter Block Diagram

DIE INFORMATION

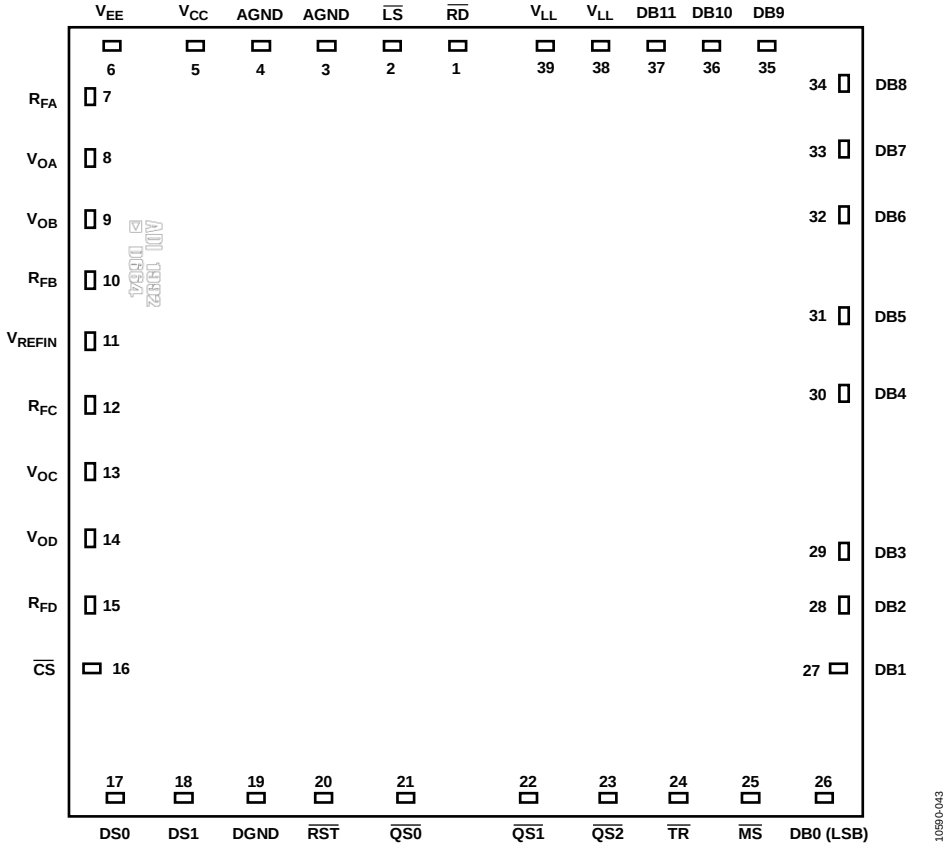


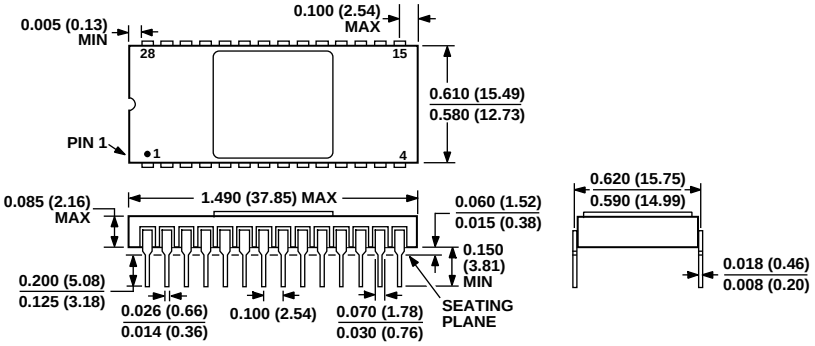
Figure 41. Bond Pad Diagram

Table 18. Bond Pad Coordinates

Pad No.	Mnemonic	Pad Coordinates		Description
		X (µm)	Y (µm)	
1	$\overline{RD}$	−98	+3403	Readback Pin (Active Low).
2	$\overline{LS}$	−896	+3403	Latch Select Pin (Active Low).
3	AGND	−1869	+3448	Analog Ground Pin.
4	AGND	−2384	+3448	Analog Ground Pin.
5	V_{CC}	−2998	+3448	Positive Analog Supply Connection.
6	V_{EE}	−3452	+2990	Negative Analog Supply Connection.
7	R_{FA}	−3452	+2396	Feedback Connection for DAC A.
8	V_{OA}	−3452	+1809	Analog Output Voltage from DAC A.
9	V_{OB}	−3452	+1208	Analog Output Voltage from DAC B.
10	R_{FB}	−3452	+611	Feedback Connection for DAC B.
11	V_{REFIN}	−3452	−1	Reference Input Voltage Pin.
12	R_{FC}	−3452	−596	Feedback Connection for DAC C.
13	V_{OC}	−3452	−1190	Analog Output Voltage from DAC C.
14	V_{OD}	−3452	−1808	Analog Output Voltage from DAC D.
15	R_{FD}	−3452	−2385	Feedback Connection for DAC D.
16	$\overline{CS}$	−3405	−2988	Chip Select Pin (Active Low).
17	DS0	−3015	−3403	DAC Address Data 0.
18	DS1	−2421	−3403	DAC Address Data 1.
19	DGND	−1825	−3456	Digital Ground.
20	$\overline{RST}$	−1222	−3403	Reset Pin (Active Low).
21	$\overline{QS0}$	−617	−3403	4-Bit Nibble Data.

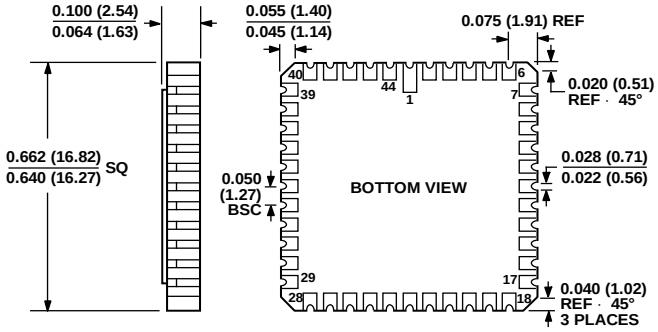
Pad No.	Mnemonic	Pad Coordinates		Description
		X (µm)	Y (µm)	
22	$\overline{QS1}$	−23	−3403	8-Bit Nibble Data.
23	$\overline{QS2}$	+574	−3403	12-Bit Nibble Data.
24	$\overline{TR}$	+1181	−3403	Transfer Register Pin (Active Low).
25	$\overline{MS}$	+1775	−3403	Mode Select Pin (Active Low).
26	DB0 (LSB)	+2294	−3321	Data Input/Output.
27	DB1	+3463	−3321	Data Input/Output.
28	DB2	+3463	−2633	Data Input/Output.
29	DB3	+3463	−1922	Data Input/Output.
30	DB4	+3463	−1195	Data Input/Output.
31	DB5	+3463	−474	Data Input/Output.
32	DB6	3463	488	Data Input/Output.
33	DB7	3463	1202	Data Input/Output.
34	DB8	3463	1925	Data Input/Output.
35	DB9	3463	2636	Data Input/Output.
36	DB10	3463	3324	Data Input/Output.
37	DB11	2301	3324	Data Input/Outputs. DB11 is MSB.
38	V_{LL}	1780	3448	Digital Supply.
39	V_{LL}	1330	3448	Digital Supply.

OUTLINE DIMENSIONS



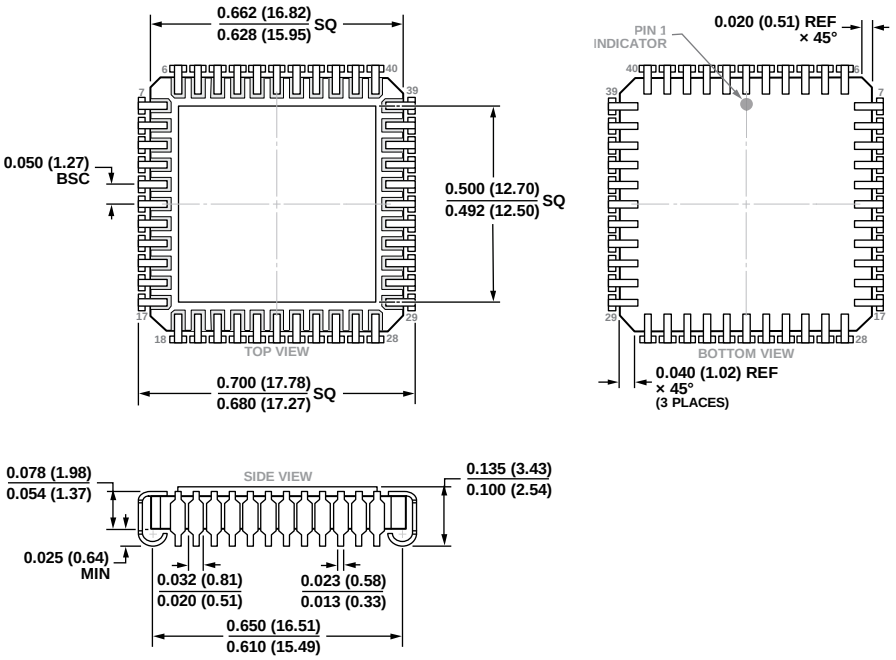
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 42. 28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]
(D-28-2)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

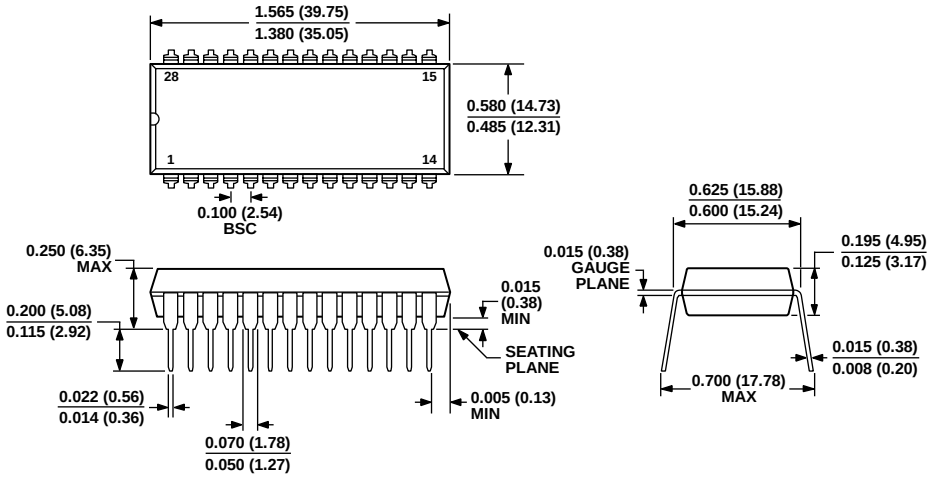
Figure 43. 44-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-44-1)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

11-16-2018-B

Figure 44. 44-Lead Ceramic Leaded Chip Carrier, J-Formed Leads [JLCC]
(J-44)
Dimensions shown in inches and (millimeters)

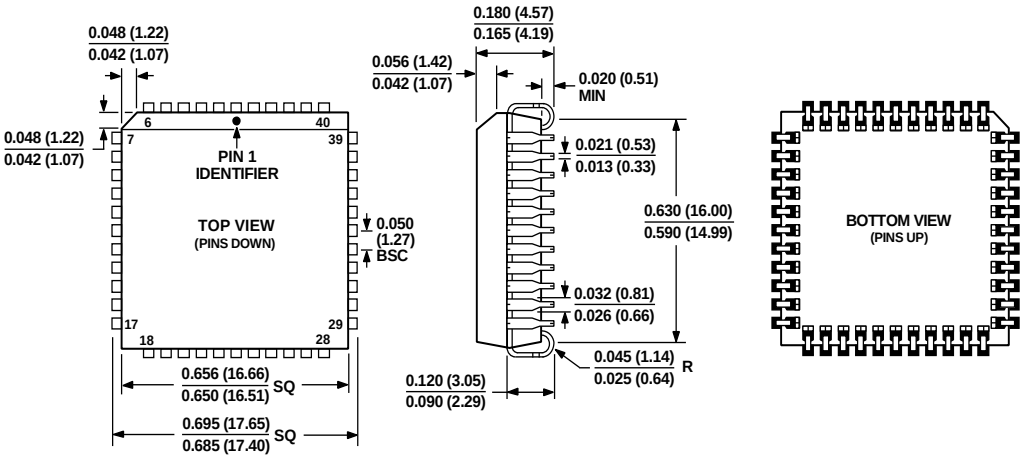


COMPLIANT TO JEDEC STANDARDS MS-011

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

Figure 45. 28-Lead Plastic Dual In-Line Package [PDIP]
Wide Body
(N-28-2)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 46. 44-Lead Plastic Leaded Chip Carrier [PLCC]
(P-44)
Dimensions shown in inches and (millimeters)

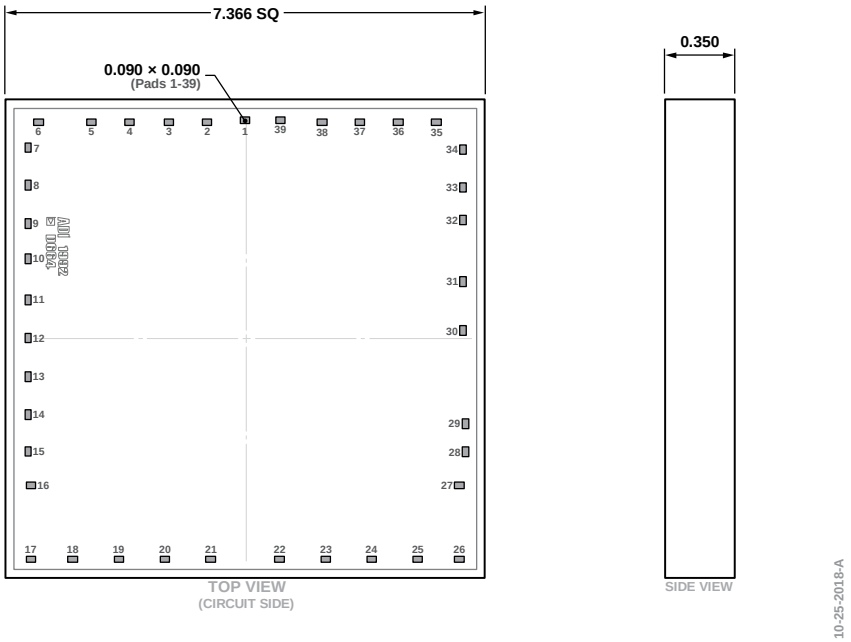


Figure 47. 39-Pad Bare Die [Chip]
(C-39-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
5962-8871901MXA	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
5962-8871902MXA	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
5962-8871903MYA	−55°C to +125°C	44-Terminal Ceramic Leadless Chip Carrier [LCC]	E-44-1
AD664AD-BIP	−40°C to +85°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664AD-UNI	−40°C to +85°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664AJ	−40°C to +85°C	44-Lead Ceramic Leaded Chip Carrier, J-Formed Leads [JLCC]	J-44
AD664BD-BIP	−40°C to +85°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664BD-UNI	−40°C to +85°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2

Model[1, 2]	Temperature Range	Package Description	Package Option
AD664BE	−40°C to +85°C	44-Terminal Ceramic Leadless Chip Carrier [LCC]	E-44-1
AD664BJ	−40°C to +85°C	44-Lead Ceramic Leaded Chip Carrier, J-Formed Leads [JLCC]	J-44
AD664JNZ-BIP	0°C to +70°C	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD664JNZ-UNI	0°C to +70°C	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD664JPZ	0°C to +70°C	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD664KNZ-BIP	0°C to +70°C	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD664KNZ-UNI	0°C to +70°C	28-Lead Plastic Dual In-Line Package [PDIP]	N-28-2
AD664KPZ	0°C to +70°C	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD664SD-BIP	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664SD-BIP/883B	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664SD-UNI/883B	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664TD-BIP	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664TD-BIP/883B	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664TD-UNI/883B	−55°C to +125°C	28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-28-2
AD664TE/883B	−55°C to +125°C	44-Terminal Ceramic Leadless Chip Carrier [LCC]	E-44-1
AD664TJ/883B	−55°C to +125°C	44-Lead Ceramic Leaded Chip Carrier, J-Formed Leads [JLCC]	J-44
AD664CHIPS	−55°C to +125°C	39-Pad Bare Die [CHIP]	C-39-2

[1] Z = RoHS Compliant Part.
[2] The AD664AJ and AD664BE are also RoHS compliant parts.

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