THE DATASHEET OF

AFT26HW050GSR3

Document Number: AFT26HW050S
Rev. 2, 7/2013

RoHS

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

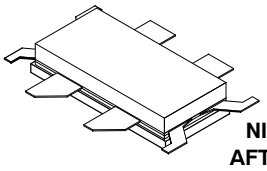
AFT26HW050SR3
AFT26HW050GSR3
AFT26H050W26SR3

2496–2690 MHz, 9 W AVG., 28 V

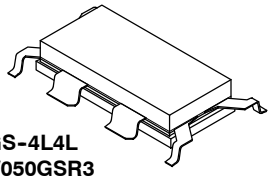
These 9 watt asymmetrical Doherty RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2496 to 2690 MHz.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 100 mA, V_{GSB} = 1.4 Vdc, P_{out} = 9 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2620 MHz	14.9	48.6	7.9	-28.4
2655 MHz	14.6	48.3	7.9	-32.6
2690 MHz	14.2	47.1	7.8	-37.3



NI-780S-4L4S
AFT26HW050SR3



NI-780GS-4L4L
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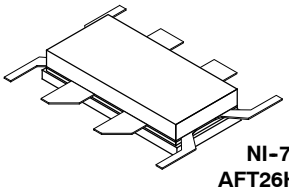


NI-780S-4L4L
AFT26H050W26SR3

Features

- Advanced High Performance In-Package Doherty
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel.

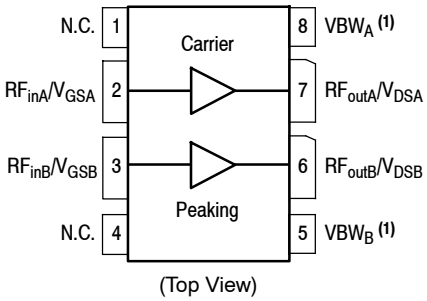


Figure 1. Pin Connections

1. Device can operate with the V_{DD} current supplied through pin 5 and pin 8.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 72°C, 9 W W-CDMA, 28 Vdc, I_{DQA} = 100 mA, V_{GSB} = 2.8 Vdc, 2655 MHz	$R_{\theta JC}$	0.75	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 18 μAdc)	$V_{GS(th)}$	1.5	2.1	2.5	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DA} = 100 mA)	$V_{GSA(Q)}$	—	2.85	—	Vdc
Gate Quiescent Voltage (5) (V_{DD} = 28 Vdc, I_{DA} = 100 mA, Measured in Functional Test)	$V_{GGA(Q)}$	5.0	5.7	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.18 Adc)	$V_{DS(on)}$	0.1	0.21	0.3	Vdc
On Characteristics - Side B (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 36 μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc)	$V_{GSB(Q)}$	—	1.4	—	Vdc
Gate Quiescent Voltage (5) (V_{DD} = 28 Vdc, Measured in Functional Test)	$V_{GGB(Q)}$	—	2.8	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.36 Adc)	$V_{DS(on)}$	0.1	0.22	0.3	Vdc

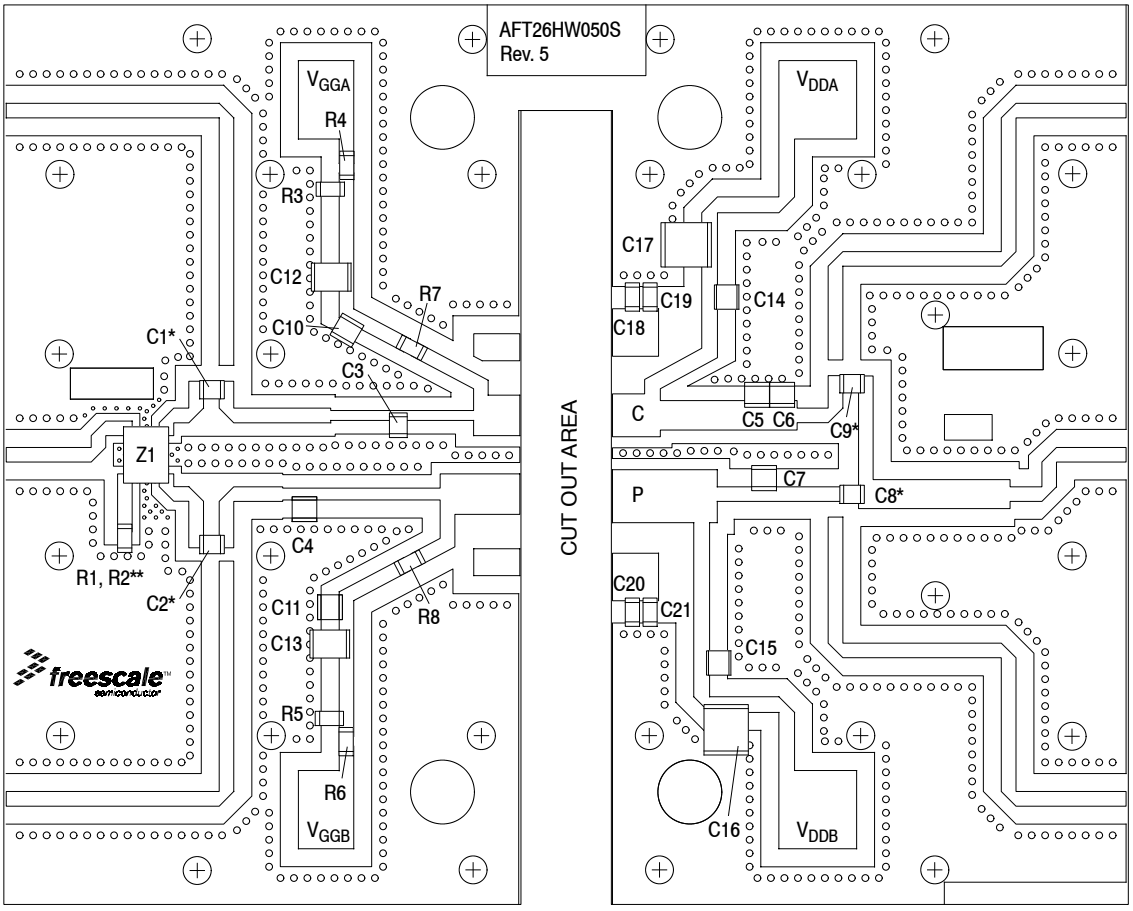
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.
5. V_{GG} = 2 × $V_{GS(Q)}$. Parameter measured on Freescale test fixture, due to resistor divider network on the board. Refer to test fixture layout.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 100 mA, V_{GSB} = 1.4 Vdc, P_{out} = 9 W Avg., f = 2690 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	13.5	14.2	16.5	dB
Drain Efficiency	η_D	44.0	47.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	7.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.3	-32.5	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 100 mA, f = 2655 MHz					
VSWR 10:1 at 32 Vdc, 35 W CW Output Power (3 dB Input Overdrive from 70 W CW Rated Power)	No Device Degradation				
Typical Performances (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 100 mA, V_{GSB} = 1.4 Vdc, 2620-2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	42	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	54	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2620-2690 MHz frequency range)	Φ	—	35	—	°
VBW Resonance Point (5) (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	130	—	MHz
Gain Flatness in 70 MHz Bandwidth @ P_{out} = 9 W Avg.	G_F	—	0.7	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.014	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.007	—	dB/°C

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Measured using gull wing formed part in AFT26HW050GS characterization test fixture. See Appendix, p. 17.



*C1, C2, C8 and C9 are mounted vertically.
**R1 and R2 are stacked.

Figure 2. AFT26HW050SR3 Test Circuit Component Layout

Table 5. AFT26HW050SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C8, C9, C10, C11, C14, C15	3.9 pF Chip Capacitors	ATC100B3R9BT500XT	ATC
C3	0.4 pF Chip Capacitor	ATC100B0R4BT500XT	ATC
C4	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C5, C6	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C7	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
C12, C13	4.7 μF Chip Capacitors	C4532X7S2A475M230KB	TDK
C16, C17	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C18, C19, C20, C21	1.0 μF Chip Capacitors	12065G105ZAT2A	AVX
R1, R2	100 Ω, 1/4 W Chip Resistors	WCR1206-100RFI	Welwyn
R3, R4, R5, R6	10 kΩ, 1/4 W Chip Resistors	WCR1206-10K0FI	Welwyn
R7, R8	4.7 Ω, 1/4 W Chip Resistors	WCR1206-4R70FI	Welwyn
Z1	2300–2700 MHz Band, 90°, 5 dB Hybrid Coupler	X3C25P1-05S	Anaren
PCB	0.030″, ε_r = 3.5	RF35A2	Taconic

TYPICAL CHARACTERISTICS

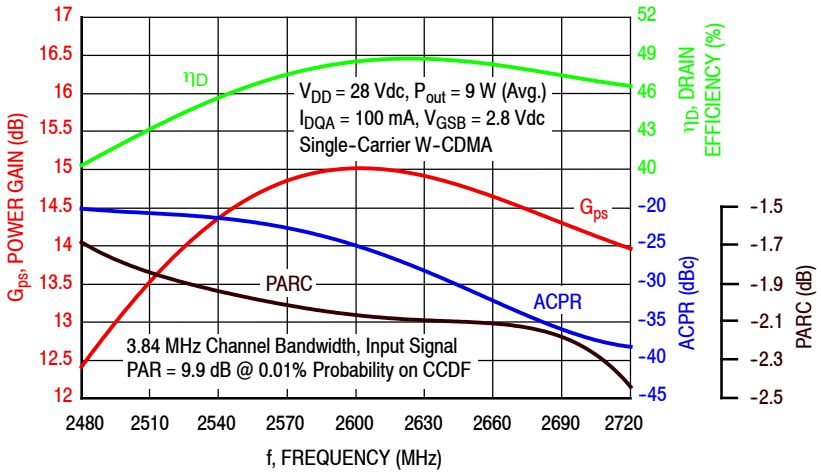
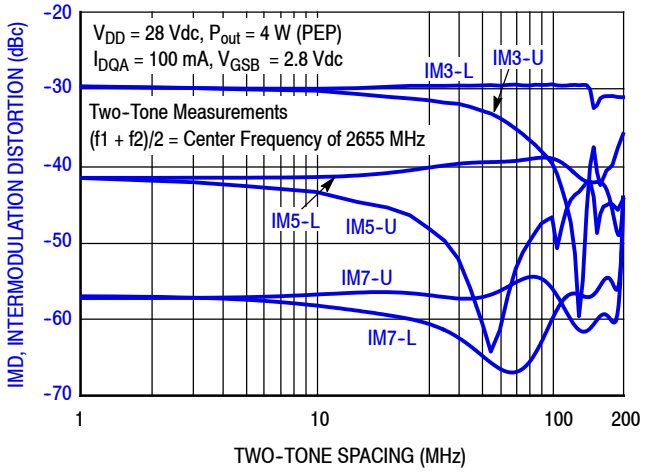


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 9 Watts Avg.



Note: Measured using gull wing formed part in AFT26HW050GS characterization test fixture. See Appendix, p. 17.

Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

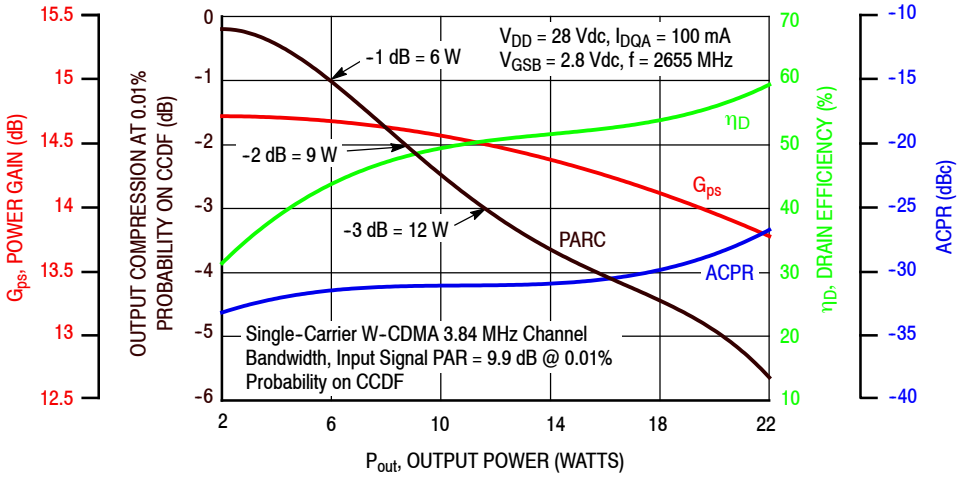


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

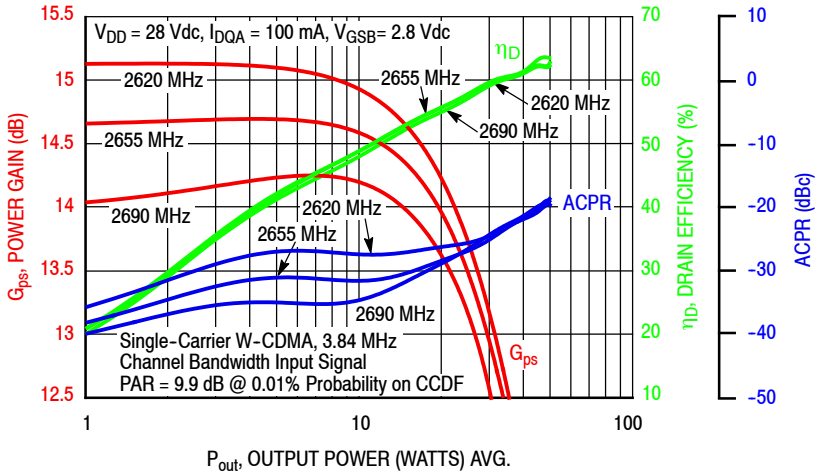


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

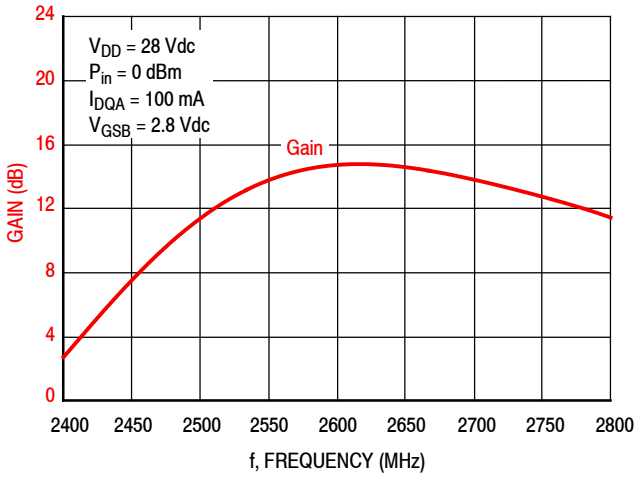


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 87 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	28.0 - j23.1	23.9 + j22.9	27.8 - j12.4	17.2	42.9	19	54.9	-17
2655	36.9 - j21.1	33.1 + j21.2	29.1 - j11.6	17.3	42.9	19	56.0	-16
2690	48.4 - j13.5	42.1 + j16.0	30.9 - j14.3	17.0	42.8	19	53.5	-17

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	28.0 - j23.1	27.1 + j23.9	29.8 - j16.4	14.8	43.6	23	54.6	-21
2655	36.9 - j21.1	37.9 + j20.4	31.0 - j16.1	14.9	43.6	23	55.1	-21
2690	48.4 - j13.5	47.7 + j12.5	32.1 - j14.9	14.9	43.6	23	54.9	-22

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

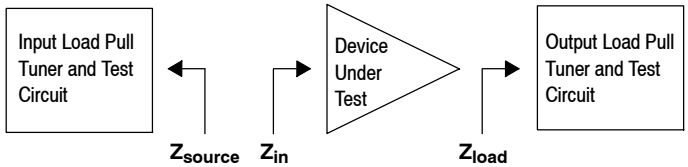
V_{DD} = 28 Vdc, I_{DQA} = 87 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	28.0 - j23.1	25.7 + j23.9	24.3 + j8.63	19.5	41.2	13	62.2	-22
2655	36.9 - j21.1	35.7 + j21.2	22.2 + j8.93	19.7	41.0	13	62.8	-22
2690	48.4 - j13.5	44.6 + j15.4	21.1 + j7.02	19.6	41.1	13	62.5	-22

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	28.0 - j23.1	28.0 + j24.6	26.6 + j5.46	17.2	42.3	17	63.1	-27
2655	36.9 - j21.1	39.6 + j20.7	23.4 + j5.31	17.3	42.2	17	63.6	-29
2690	48.4 - j13.5	49.3 + j11.6	21.5 + j5.46	17.4	42.0	16	63.0	-30

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	27.1 – j17.7	22.9 + j19.6	8.62 – j15.3	12.8	46.1	40	58.3	–32
2655	36.7 – j12.5	32.0 + j15.6	8.78 – j15.7	12.8	46.1	40	58.4	–33
2690	39.5 – j2.23	37.9 + j7.03	8.71 – j17.3	12.4	45.9	39	54.9	–33

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	27.1 – j17.7	26.5 + j18.9	8.56 – j16.9	10.5	46.7	47	57.3	–37
2655	36.7 – j12.5	35.9 + j11.8	8.57 – j17.0	10.5	46.8	47	57.2	–38
2690	39.5 – j2.23	39.4 + j1.33	9.02 – j18.1	10.4	46.6	46	55.6	–38

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

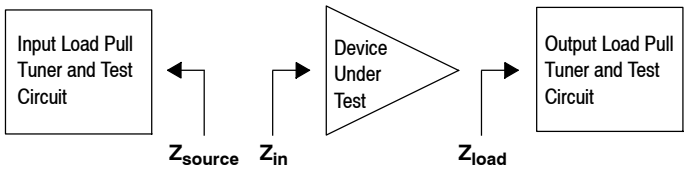
V_{DD} = 28 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	27.1 – j17.7	21.4 + j21.6	13.6 – j7.07	14.1	44.4	28	68.7	–38
2655	36.7 – j12.5	31.4 + j19.0	13.5 – j5.38	14.0	44.0	25	68.6	–40
2690	39.5 – j2.23	39.1 + j10.8	13.5 – j7.10	13.9	44.2	26	67.7	–39

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2620	27.1 – j17.7	25.3 + j21.2	13.9 – j7.07	12.1	44.9	31	68.0	–48
2655	36.7 – j12.5	36.2 + j15.4	12.5 – j7.10	12.1	45.0	31	68.1	–49
2690	39.5 – j2.23	41.9 + j4.53	12.5 – j6.42	12.0	44.6	29	66.9	–50

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2655 MHz

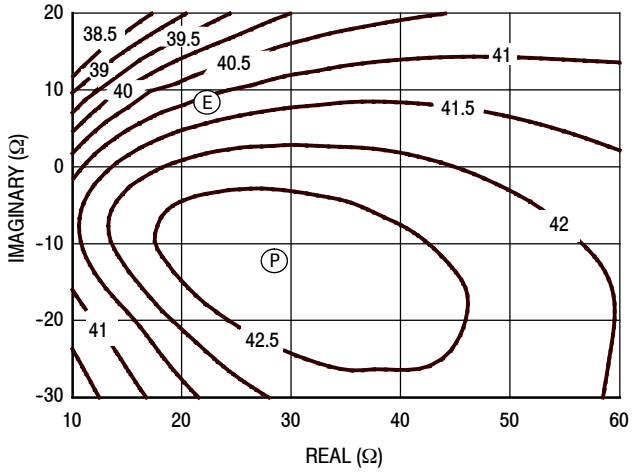


Figure 12. P1dB Load Pull Output Power Contours (dBm)

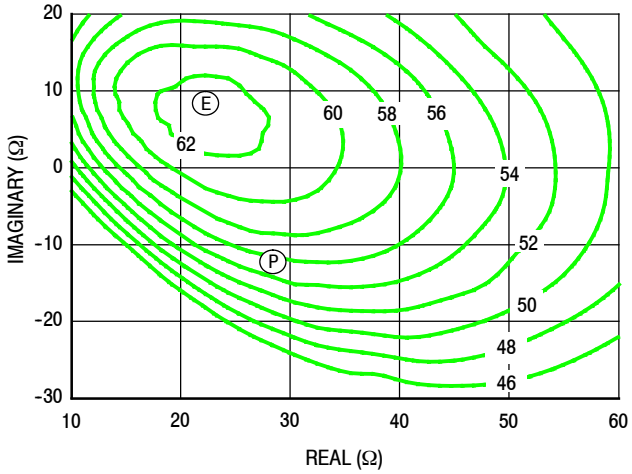


Figure 13. P1dB Load Pull Efficiency Contours (%)

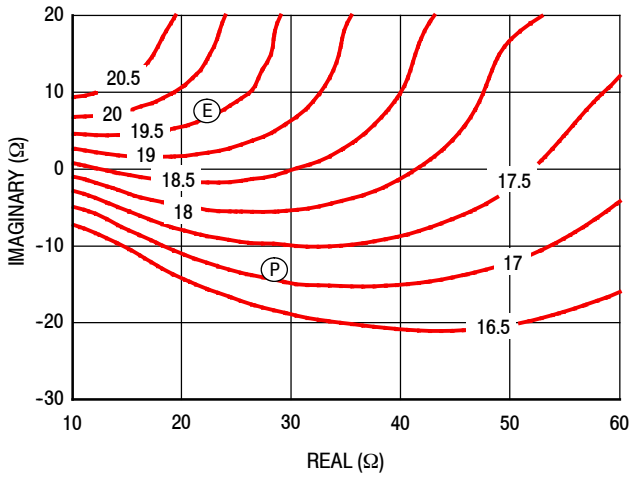


Figure 14. P1dB Load Pull Gain Contours (dB)

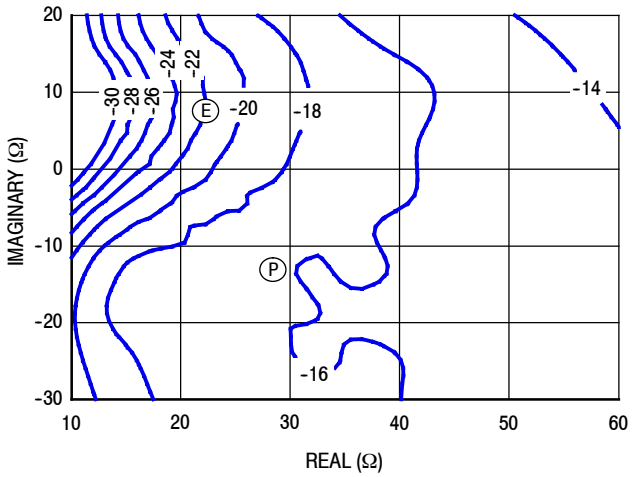


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2655 MHz

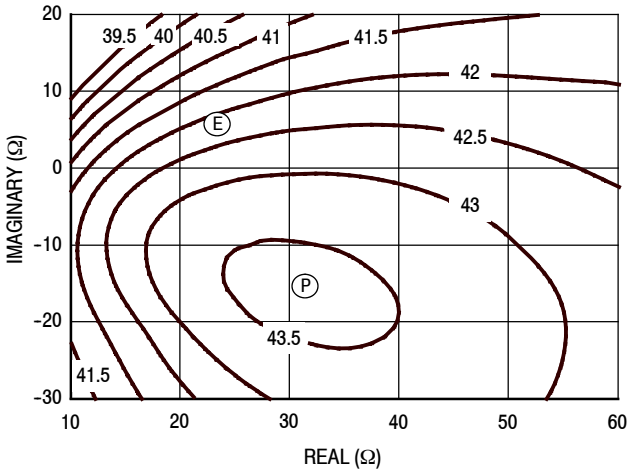


Figure 16. P3dB Load Pull Output Power Contours (dBm)

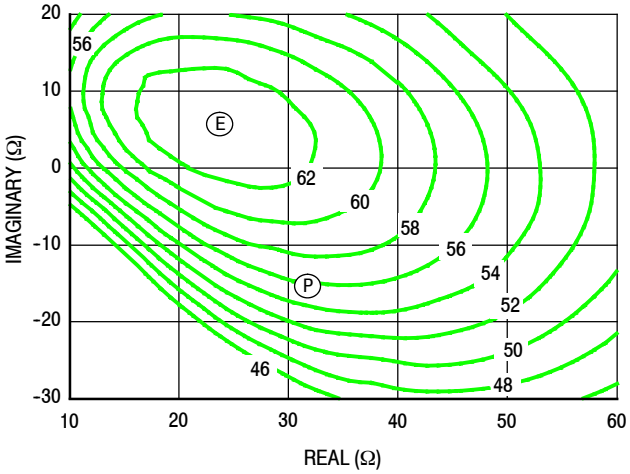


Figure 17. P3dB Load Pull Efficiency Contours (%)

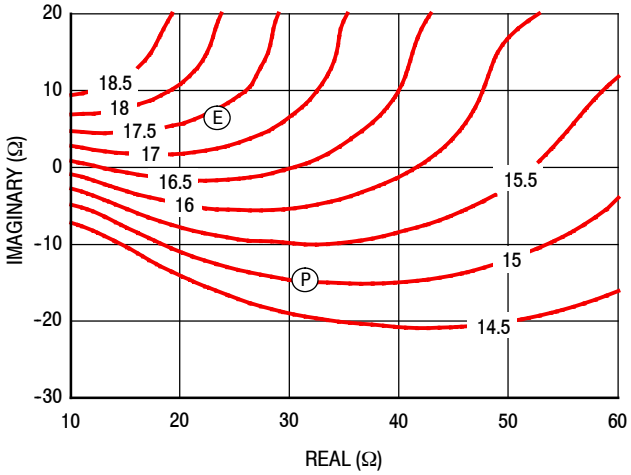


Figure 18. P3dB Load Pull Gain Contours (dB)

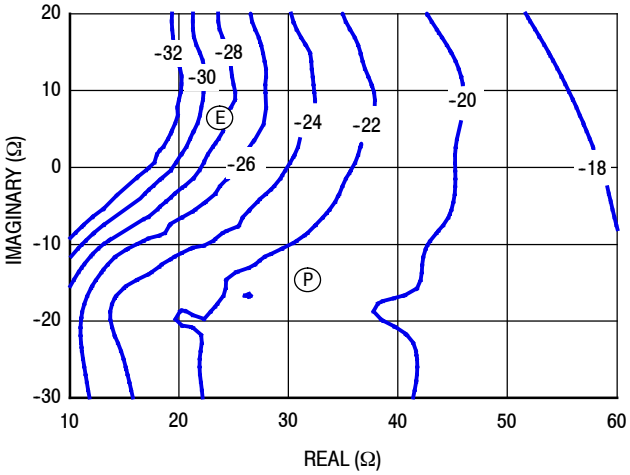


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2655 MHz

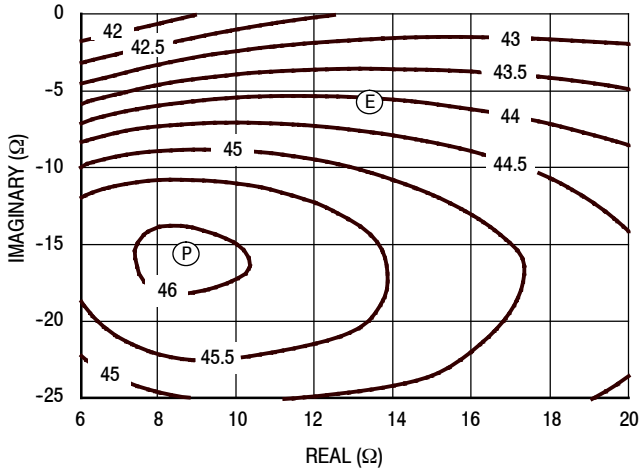


Figure 20. P1dB Load Pull Output Power Contours (dBm)

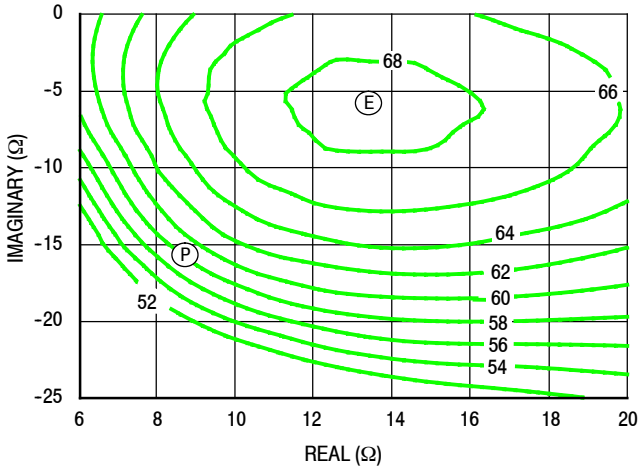


Figure 21. P1dB Load Pull Efficiency Contours (%)

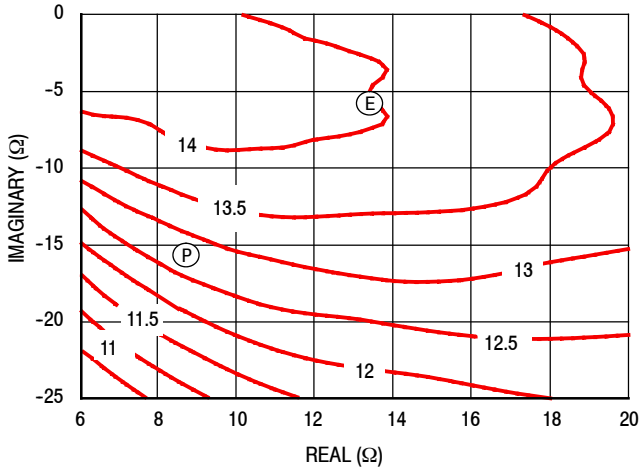


Figure 22. P1dB Load Pull Gain Contours (dB)

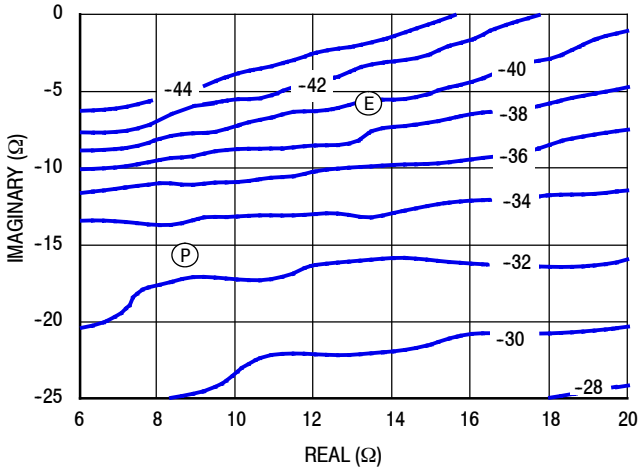


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2655 MHz

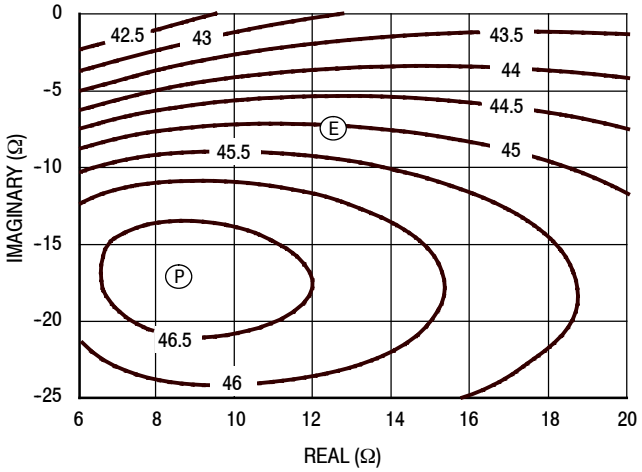


Figure 24. P3dB Load Pull Output Power Contours (dBm)

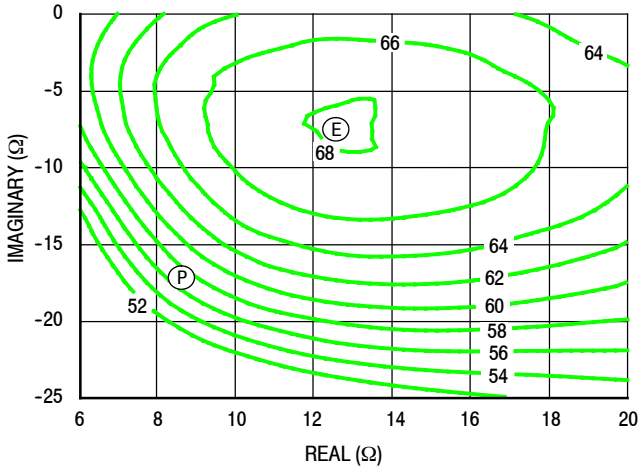


Figure 25. P3dB Load Pull Efficiency Contours (%)

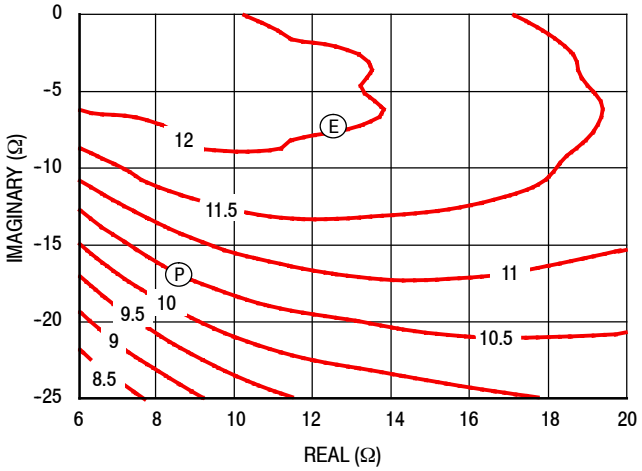


Figure 26. P3dB Load Pull Gain Contours (dB)

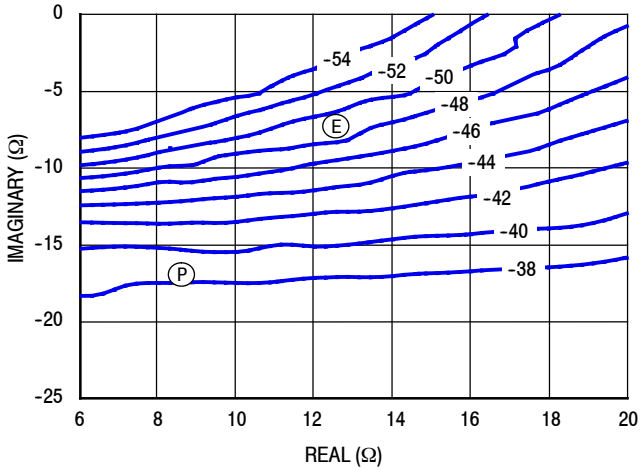


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

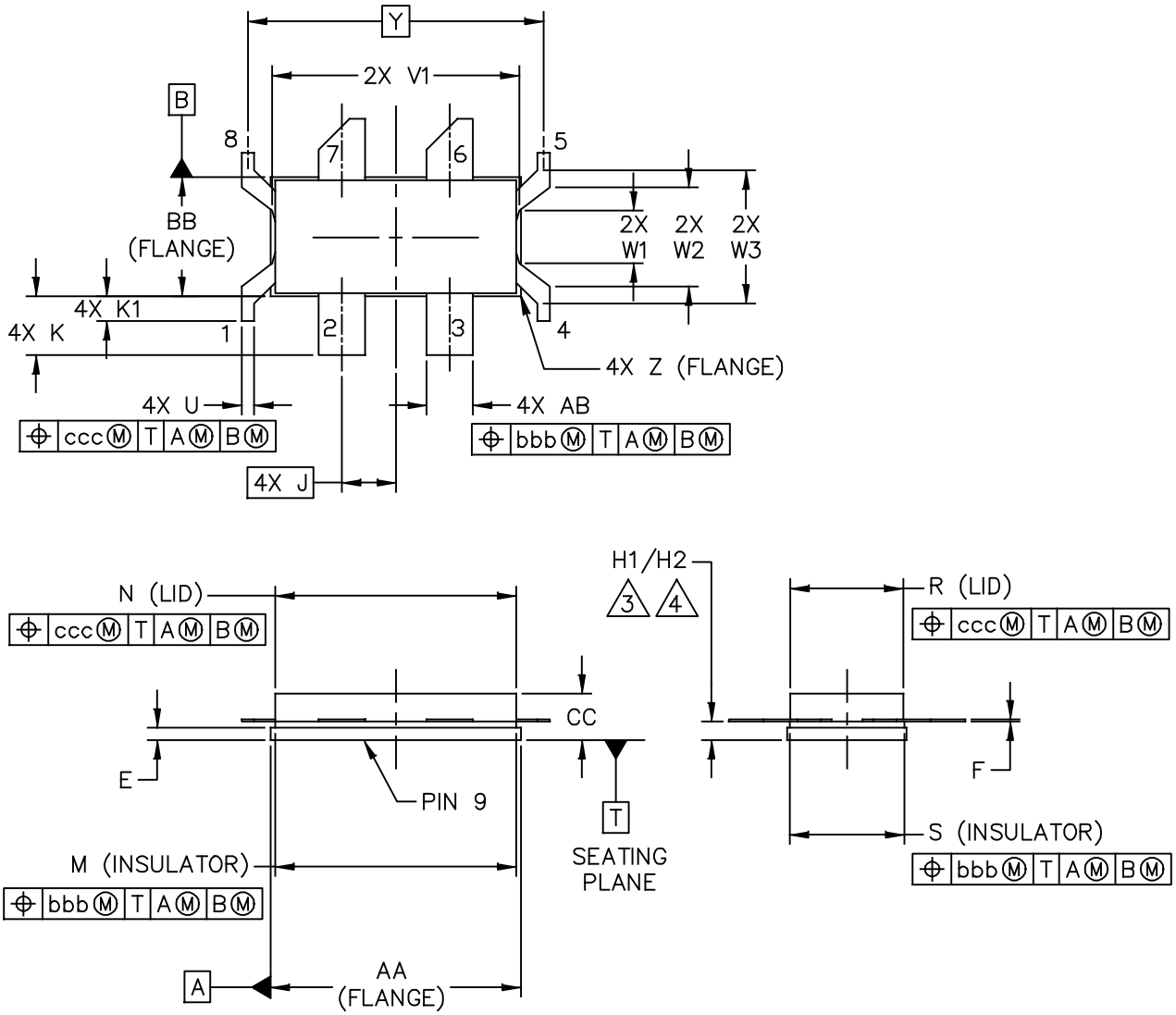
Power Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2, 3, 6 & 7. H2 APPLIES TO PINS 1, 4, 5 & 8.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.165	.175	4.19	4.45
H1	.057	.067	1.45	1.70	W2	.315	.325	8.00	8.26
H2	.054	.070	1.37	1.78	W3	.425	.435	10.80	11.05
J	.175 BSC		4.45 BSC		Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
K1	.070	.090	1.78	2.29	AB	.145	.155	3.68	3.94
M	.774	.786	19.66	19.96	aaa	–	.005	–	0.13
N	.772	.788	19.61	20.02	bbb	–	.010	–	0.25
					ccc	–	.015	–	0.38

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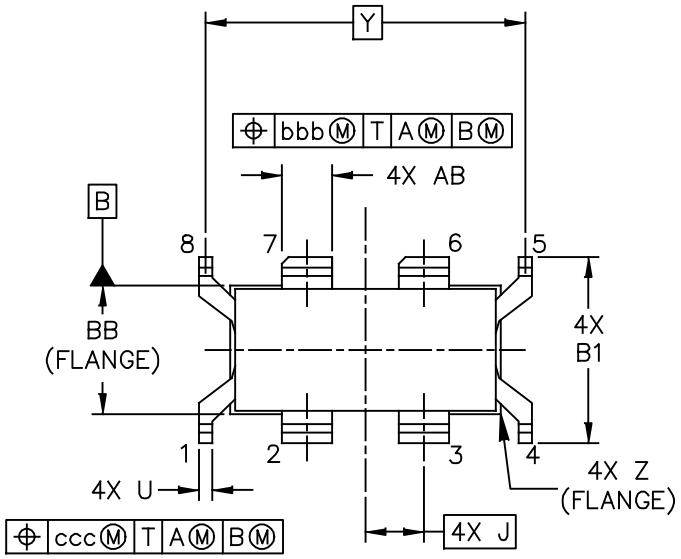
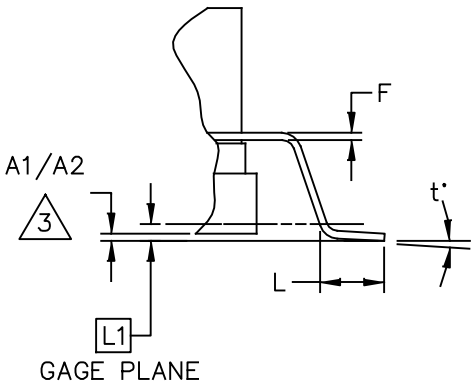
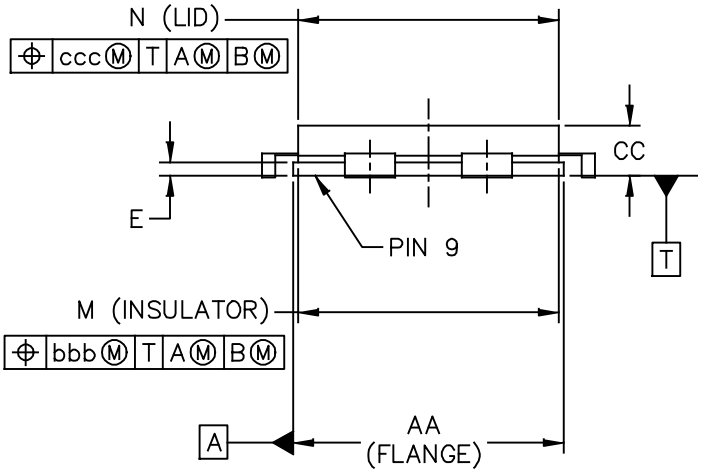
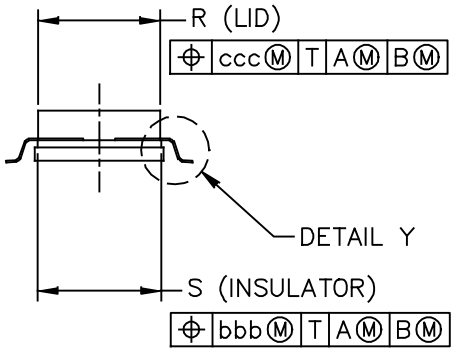




DETAIL "Y"





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NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSION A1/A2 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM. A1 APPLIES TO PINS 2, 3, 6 & 7. A2 APPLIES TO PINS 1, 4, 5 & 8

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
A1	.000	.010	0.00	0.25	S	.365	.375	9.27	9.53
A2	−.003	.013	−0.08	0.33	U	.035	.045	0.89	1.14
BB	.380	.390	9.65	9.91	Y	.956 BSC		24.28 BSC	
B1	.549	.559	13.94	14.20	Z	R.000	R.040	R0.00	R1.02
CC	.125	.170	3.18	4.32	AB	.145	.155	3.68	3.94
E	.035	.045	0.89	1.14	t°	0°	8°	0°	8°
F	.004	.007	0.10	0.18	aaa	–	.005	–	0.13
J	.175 BSC		4.45 BSC		bbb	–	.010	–	0.25
L	.038	.046	0.97	1.17	ccc	–	.015	–	0.38
L1	.01 BSC		0.25 BSC						
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					

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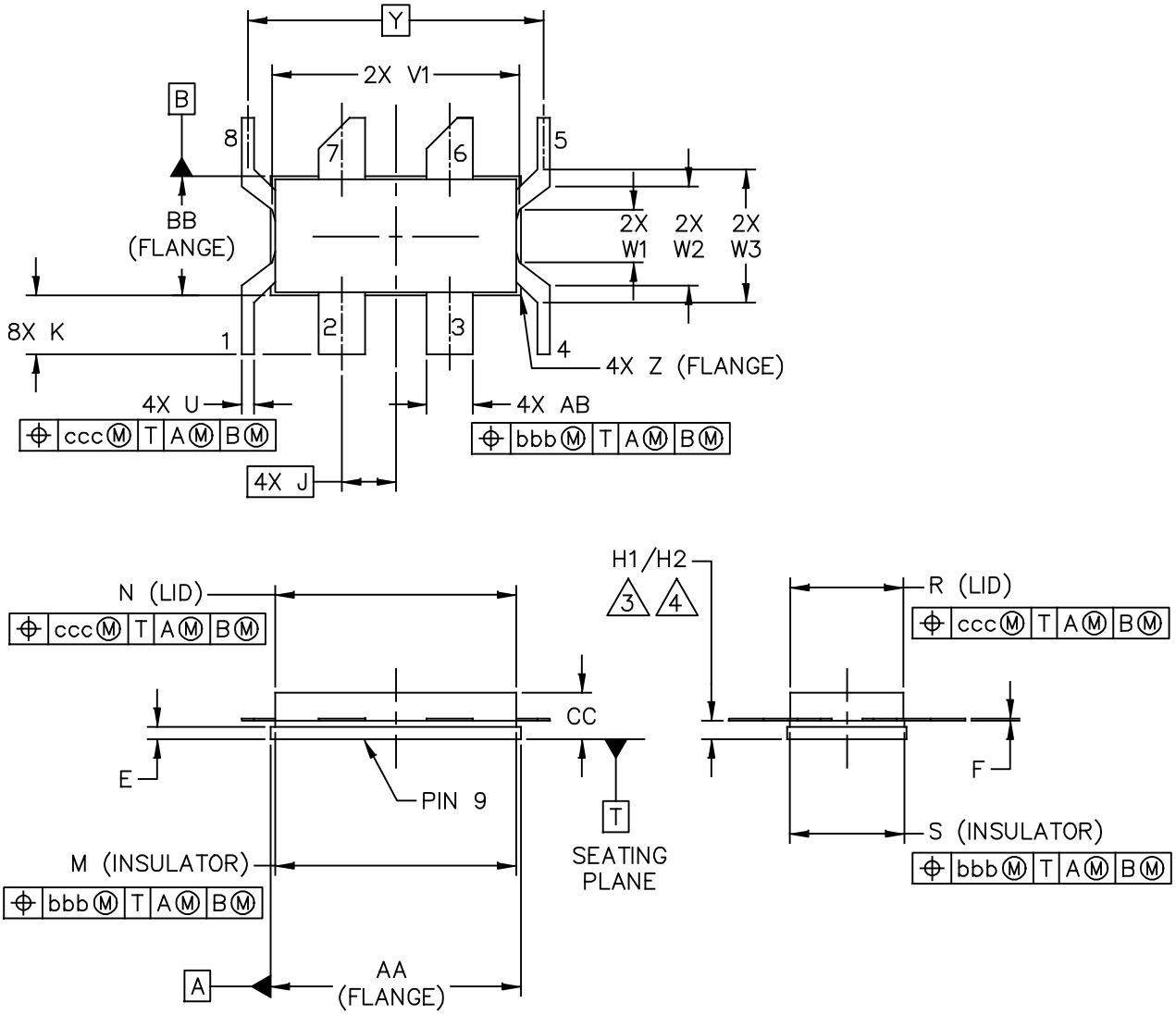

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NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2, 3, 6 & 7. H2 APPLIES TO PINS 1, 4, 5 & 8.

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DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.165	.175	4.19	4.45
H1	.057	.067	1.45	1.70	W2	.315	.325	8.00	8.26
H2	.054	.070	1.37	1.78	W3	.425	.435	10.80	11.05
J	.175 BSC		4.45 BSC		Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	AB	.145	.155	3.68	3.94
N	.772	.788	19.61	20.02	aaa	.005		0.13	
					bbb	.010		0.25	
					ccc	.015		0.38	

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APPENDIX

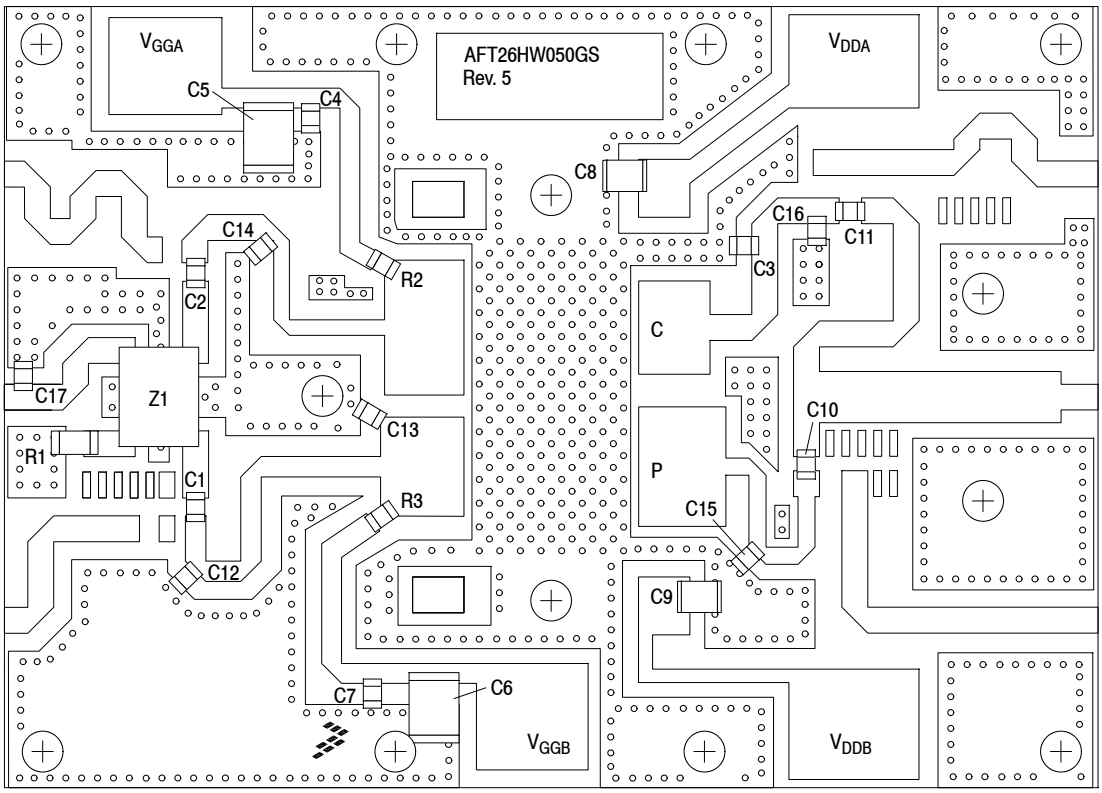

Figure A-1. AFT26HW050GSR3 Characterization Test Circuit Component Layout

Table A-1. AFT26HW050GSR3 Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	3.3 pF Chip Capacitor	08051J3R3CBTTR	AVX
C2, C4, C7, C10, C11	4.7 pF Chip Capacitors	08051J4R7CBTTR	AVX
C3, C12, C13, C15	0.5 pF Chip Capacitors	08051J0R5BBTTR	AVX
C5, C6	4.7 μF Chip Capacitors	C4532X7S2A475M230KB	TDK
C8, C9	3.3 μF Chip Capacitors	C3225X7S2A335M200AB	TDK
C14, C17	0.2 pF Chip Capacitors	08051J0R2ABTTR	AVX
C16	0.1 pF Chip Capacitor	08051J0R1ABTTR	AVX
R1	51 Ω, 1/4 W Chip Resistor	WCR1206-51FI	Welwyn
R2, R3	4.7 Ω, 1/8 W Chip Resistors	WCR0805-4R7FI	Welwyn
Z1	2300-2700 MHz Band, 90°, 5 dB Hybrid Coupler	X3C25P1-05S	Anaren
PCB	0.030″, ε_r = 3.5	RF35A2	Taconic

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial Release of Data Sheet
1	June 2013	• Added part number AFT26H050W26SR3, p. 1 • Added NI-780S-4L4L package isometric, p. 1, and Mechanical Outline, p. 17, 18
2	July 2013	• AFT26HW050S data sheet frequency changed from 2620 MHz to 2496 MHz to show part performance capability in the 2496-2690 MHz frequency range, p. 1 • Fig. 3, Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 9 Watts Avg., updated to reflect part performance in the 2496-2690 MHz frequency range, p. 5

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