THE DATASHEET OF

LTC1147LCS8-3.3#PBF

High Efficiency Step-Down Switching Regulator Controllers

FEATURES

- **Very High Efficiency: Over 95% Possible**
- **Wide V_{IN} Range: 3.5V* to 16V**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Three Decades of Output Current
- Low 160µA Standby Current at Light Loads
- Logic Controlled Micropower Shutdown: I_Q < 20µA
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- High Efficiency in a Small Amount of Board Space
- Output Can Be Externally Held High in Shutdown
- Available in 8-Pin SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Cellular Telephones
- DC Power Distribution Systems
- GPS Systems

DESCRIPTION

The LTC®1147 series are step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive an external P-channel power MOSFET at switching frequencies exceeding 400kHz using a constant off-time current mode architecture providing constant ripple current in the inductor.

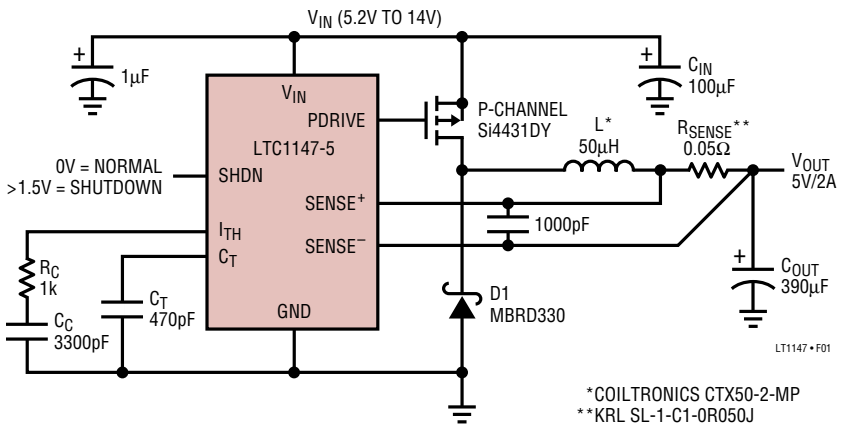
The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V* to 14V (16V maximum). Constant off-time architecture provides low dropout regulation limited by only the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1147 series incorporates automatic power saving Burst Mode operation to reduce switching losses when load currents drop below the level required for continuous operation. Standby power is reduced to only 2mW at V_{IN} = 10V (at I_{OUT} = 0). Load currents in Burst Mode operation are typically 0mA to 300mA.

For applications where even higher efficiency is required, refer to the LTC1148 data sheet and Application Note 54.

*LTC1147L and LTC1147L-3.3 only.

TYPICAL APPLICATION



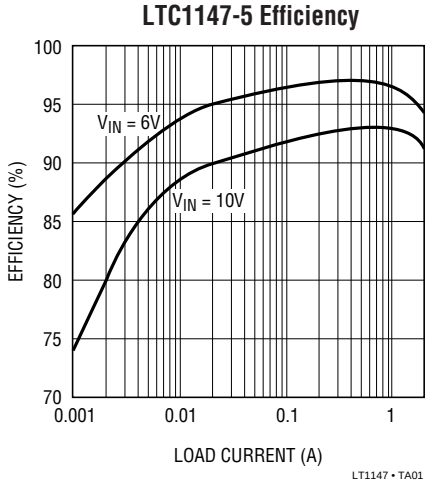


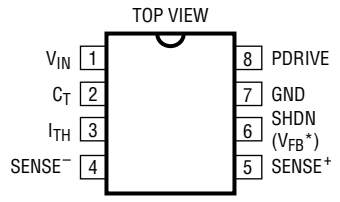
Figure 1. High Efficiency Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 1) ..... 16V to –0.3V
Continuous Output Current (Pin 8) 50mA
Sense Voltages (Pins 4, 5)
$V_{IN} \geq 12.7V$ ..... 13V to –0.3V
$V_{IN} < 12.7V$ ..... (V_{IN} + 0.3V) to –0.3V

Operating Ambient Temperature Range
LTC1147C ..... 0°C to 70°C
LTC1147I ..... –40°C to 85°C
Extended Commercial
Temperature Range (Note 4) ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SO

* ADJUSTABLE OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 110°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER		S8 PART MARKING
LTC1147CN8-3.3	LTC1147IS8-5	11473
LTC1147CN8-5	LTC1147LCS8	11475
LTC1147CS8-3.3	LTC1147LCS8-3.3	1147I3
LTC1147CS8-5	LTC1147LIS8	1147I5
LTC1147IS8-3.3		1147L
		1147L3
		1147LI

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, V_{SHDN} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_6	Feedback Voltage (LTC1147L)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_6	Feedback Current (LTC1147L)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage V_{IN} = 9V						
	LTC1147-3.3, LTC1147L-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1147-5	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1147-3.3, LTC1147L-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1147-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_Q	Input DC Supply Current (Note 2) LTC1147 Series	(Note 5)					
	Normal Mode	4V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	4V < V_{IN} < 12V			160	230	µA
	Sleep Mode (LTC1147-5)	5V < V_{IN} < 12V			160	230	µA
	Shutdown	V_{SHDN} = 2.1V, 4V < V_{IN} < 12V			10	20	µA
	LTC1147L Series						
	Normal Mode	3.5V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	3.5V < V_{IN} < 12V			160	230	µA
	Shutdown (LTC1147L-3.3)	V_{SHDN} = 2.1V, 3.5V < V_{IN} < 12V			10	20	µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, V_{SHDN} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_5 - V_4$	Current Sense Threshold Voltage (Note 6)						
	LTC1147-3.3, LTC1147L-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)		130	150	170	mV
	LTC1147–5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)		130	150	170	mV
	LTC1147L	V_{SENSE}^- = 5V, V6 = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 5V, V6 = V_{OUT}/4 – 25mV (Forced)		130	150	170	mV
V_6	SHDN Pin Threshold						
	LTC1147-3.3/LTC1147-5/LTC1147L-3.3			0.5	0.8	2	V
I_6	SHDN Pin Input Current						
	LTC1147-3.3/LTC1147-5/LTC1147L-3.3	0V < V_{SHDN} < 8V, V_{IN} = 16V			1.2	5	µA
I_2	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pin 8), V_{IN} = 6V			100	200	ns

–40°C ≤ T_A ≤ 85°C (Note 4), V_{IN} = 10V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_6	Feedback Voltage (LTC1147L)	V_{IN} = 9V	●	1.20	1.25	1.30	V
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	LTC1147-3.3/LTC1147L-3.3	I_{LOAD} = 700mA	●	3.17	3.33	3.43	V
	LTC1147-5	I_{LOAD} = 700mA	●	4.85	5.05	5.20	V
I_Q	Input DC Supply Current (Note 2)	(Note 5)					
	LTC1147 Series						
	Normal Mode	4V < V_{IN} < 12V			1.6	2.4	mA
	Sleep Mode	4V < V_{IN} < 12V			160	260	µA
	Sleep Mode (LTC1147-5)	5V < V_{IN} < 12V			160	260	µA
	Shutdown	V_{SHDN} = 2.1V, 4V < V_{IN} < 12V			10	22	µA
	LTC1147L Series						
	Normal Mode	3.5V < V_{IN} < 12V			1.6	2.4	mA
	Sleep Mode	3.5V < V_{IN} < 12V			160	260	µA
	Shutdown (LTC1147L-3.3)	V_{SHDN} = 2.1V, 3.5V < V_{IN} < 12V			10	22	µA
$V_5 - V_4$	Current Sense Threshold Voltage (Note 6)						
	LTC1147-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	125	150	185	mV
	LTC1147-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	125	150	185	mV
	LTC1147L	V_{SENSE}^- = 5V, 6V = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 5V, 6V = V_{OUT}/4 – 25mV (Forced)		125	150	185	mV
V_6	SHDN Pin Threshold						
	LTC1147-3.3/LTC1147-5/LTC1147L-3.3	0V < V_{SHDN} < 8V, V_{IN} = 16V		0.5	0.8	2	V
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA		3.8	5	6.5	µs

The ● denotes specifications which apply over the full specified temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1147CN8-3.3/LTC1147CN8-5: $T_J = T_A + (P_D)(110°C/W)$
LTC1147LIS/LTC1147IS8/LTC1147LCS/
LTC1147CS8-3.3/LTC1147CS8-5: $T_J = T_A + (P_D)(150°C/W)$

Note 2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

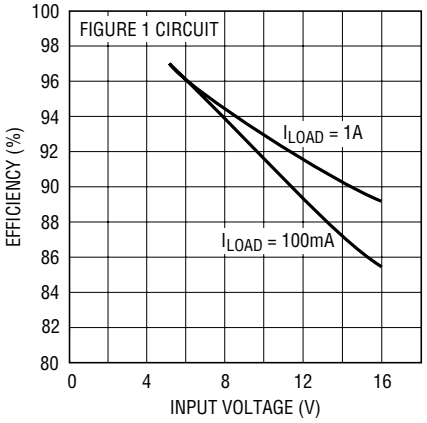
Note 4: The LTC1147C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. The LTC1147I is guaranteed to meet the extended temperature limits.

Note 5: The LTC1147L/LTC1147L-3.3 allow operation to V_{IN} = 3.5V.

Note 6: The LTC1147L is tested with external feedback resistors resulting in a nominal output voltage of 2.5V.

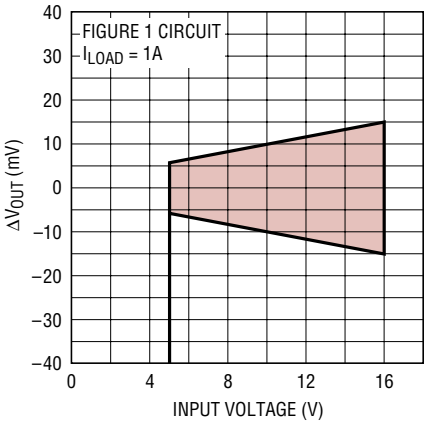
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



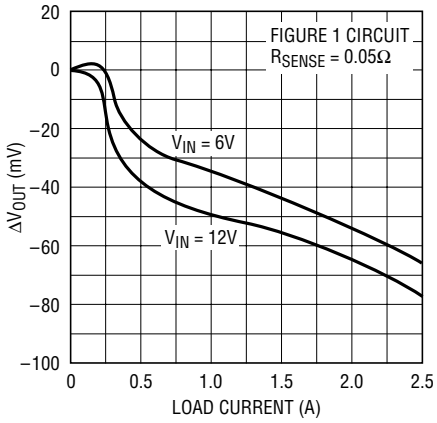
LTC1147 • G01

Line Regulation



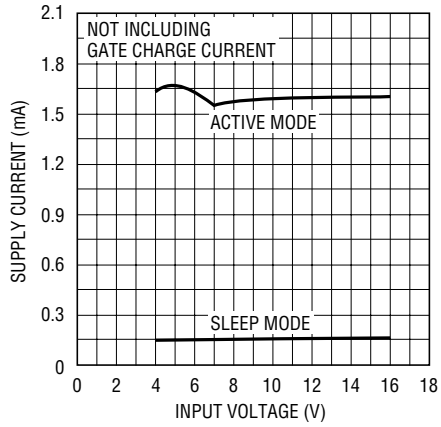
LTC1147 • G02

Load Regulation



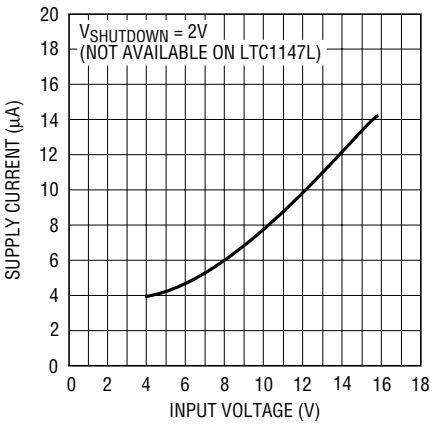
LTC1147 • G03

DC Supply Current



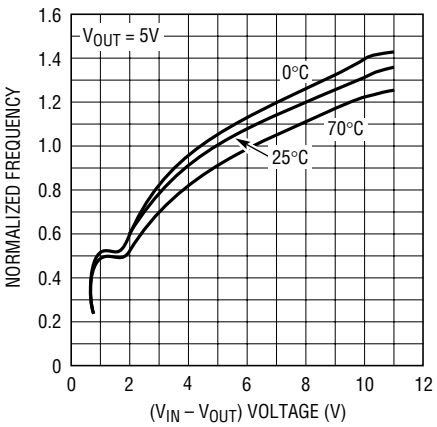
LTC1147 • G04

Supply Current in Shutdown



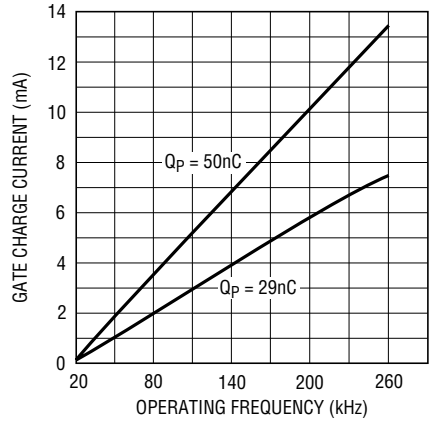
LTC1147 • G05

Operating Frequency vs (V_{IN} – V_{OUT})



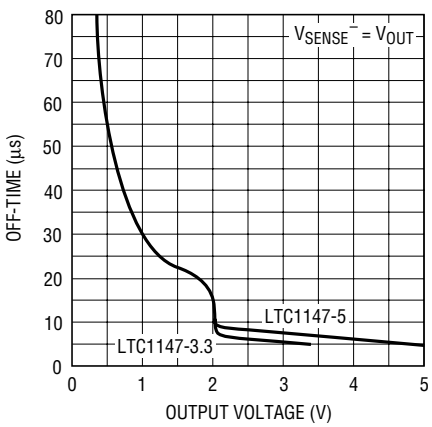
LTC1148 • G06

Gate Charge Supply Current



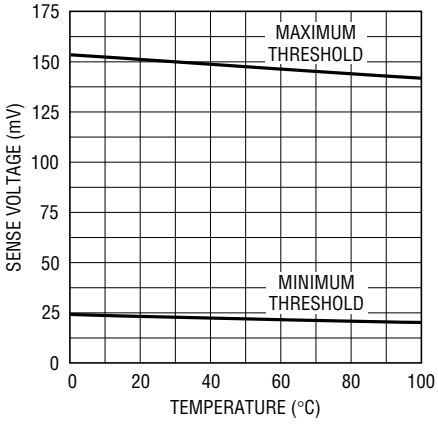
LTC1147 • G07

Off-Time vs V_{OUT}



LTC1147 • G08

Current Sense Threshold Voltage



LTC1147 • G09

PIN FUNCTIONS

V_{IN} (Pin 1): Main Supply Pin. Must be closely decoupled to ground Pin 7.

C_T (Pin 2): External capacitor C_T from Pin 2 to ground sets the operating frequency. The actual frequency is also dependent upon the input voltage.

I_{TH} (Pin 3): Gain Amplifier Decoupling Point. The current comparator threshold increases with the Pin 3 voltage.

SENSE$^-$ (Pin 4): Connects to internal resistive divider which sets the output voltage. Pin 4 is also the (–) input for the current comparator.

SENSE$^+$ (Pin 5): The (+) input to the current comparator. A built-in offset between Pins 4 and 5 in conjunction with R_{SENSE} sets the current trip threshold.

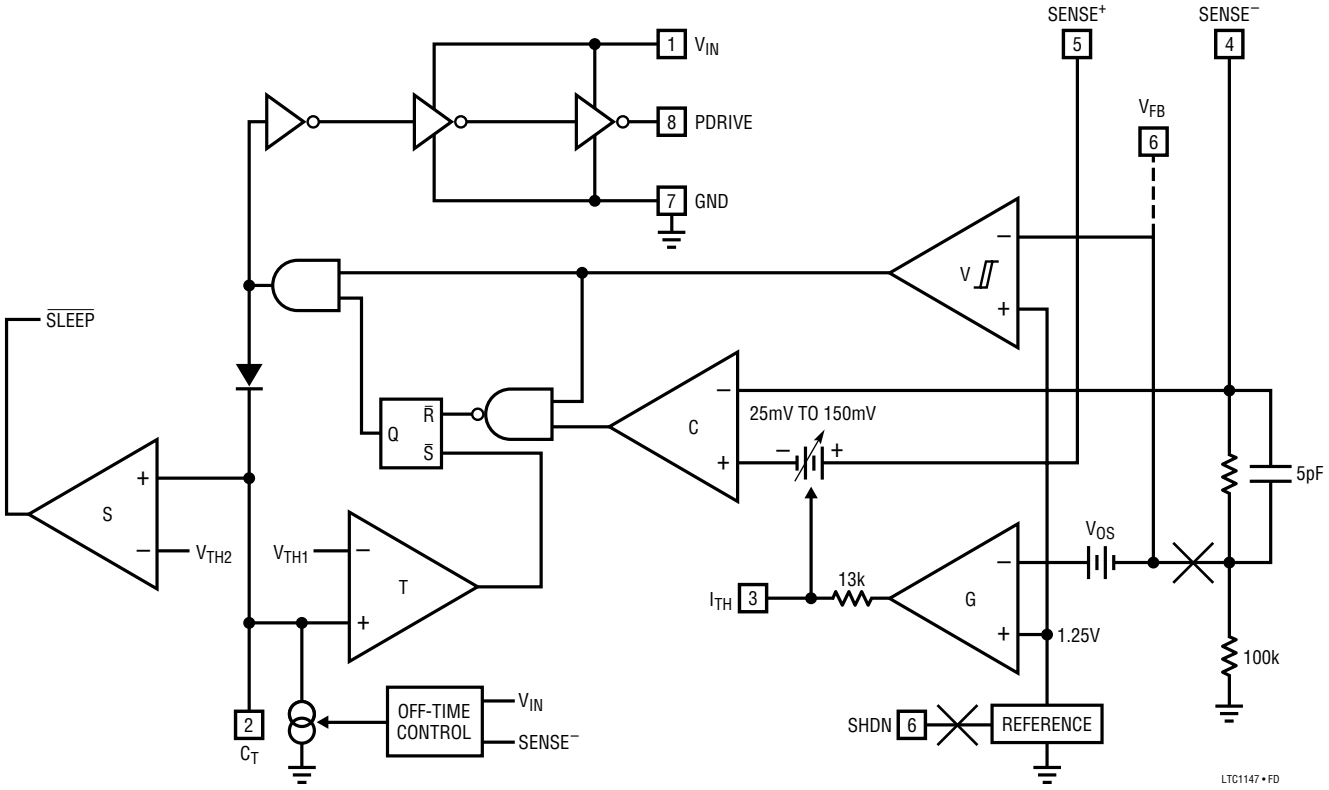
SHDN/V_{FB} (Pin 6): When grounded, the fixed output versions of the LTC1147 family operate normally. Pulling Pin 6 high holds the P-channel MOSFET off and puts the LTC1147 in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not leave this pin floating. On the LTC1147L this pin serves as the feedback pin from an external resistive divider used to set the output voltage.

GND (Pin 7): Two independent ground lines must be routed separately to: 1) the (–) terminal of C_{OUT}, and 2) the cathode of the Schottky diode and (–) terminal of C_{IN}.

PDRIVE (Pin 8): High current drive for the P-channel MOSFET. Voltage swing at this pin is from V_{IN} to ground.

FUNCTIONAL DIAGRAM

Pin 6 Connection Shown For LTC1147-3.3 and LTC1147-5; Changes Create LTC1147L.



OPERATION (Refer to Functional Diagram)

The LTC1147 series uses a current mode, constant off-time architecture to switch an external P-channel power MOSFET. Operating frequency is set by an external capacitor at C_T (Pin 2).

The output voltage is sensed by an internal voltage divider connected to $SENSE^-$ (Pin 4). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1147 series automatically switchs between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "on" cycle in continuous mode, current comparator C monitors the voltage between Pins 4 and 5 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the PDRIVE output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to Pin 2 is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by Pin 4) to model the inductor current, which decays at a rate which is also proportional to the output voltage.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the PDRIVE output to go low turning the P-channel MOSFET back on. The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (Pin 3) to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{sleep}$ line to go low.

The circuit now enters $\overline{sleep}$ mode with the power MOSFET turned off. In $\overline{sleep}$ mode, a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160μA. The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing low dropout operation with $V_{OUT} \approx V_{IN}$.

APPLICATIONS INFORMATION

LTC1147L Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1147L adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} (Pin 6) (see Figure 7). The regulated voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1147L.

For Figure 1 applications with V_{OUT} below 2V, or when R_{SENSE} is moved to ground, the current sense comparator inputs operate near ground. When the current comparator is operated at less than 2V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

APPLICATIONS INFORMATION

The basic LTC1147 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFET and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 16V. If the application requires higher input voltage, then the synchronous switched LTC1149 should be used. Consult factory for lower minimum input voltage version.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1147 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1147 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

The load current below in which Burst Mode operation commences, I_{BURST} and the peak short-circuit current $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

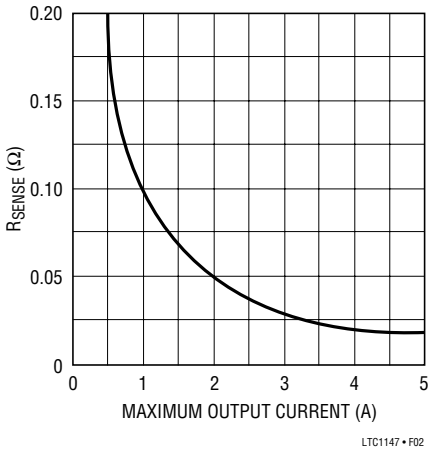


Figure 2. Selecting R_{SENSE}

The LTC1147 series automatically extend t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1147 series use a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{(1.3)(10^4)(f)}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)$$

Where V_D is the drop across the Schottky diode.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will reduce efficiency (see Efficiency Considerations). The complete expression for operating frequency

APPLICATIONS INFORMATION

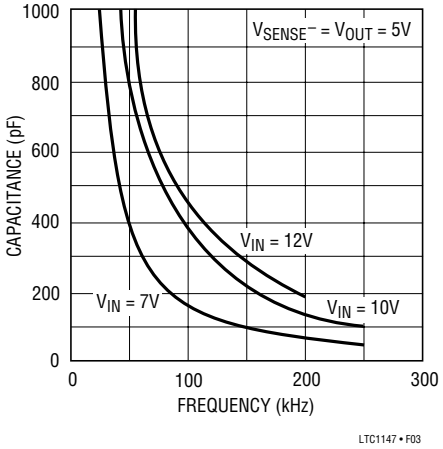


Figure 3. Timing Capacitor Value

is given by:

$$f \approx \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = (1.3)(10^4)(C_T)\left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus V_{REG}/V_{OUT} = 1 in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1147 reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = (5.1)(10^5)(R_{SENSE})(C_T)(V_{REG})$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will become discontinuous before the LTC1147 series enters Burst Mode operation. A consequence of this is that the LTC1147 series will delay entering Burst Mode operation and efficiency will be degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. Highest efficiency will be obtained using ferrite, Kool Mμ® (from Magnetics, Inc.) or molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance but cut efficiency by 3% to 5%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered in the LTC1147. Do not allow the core to saturate!

Kool Mμ is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics, Sumida and Beckman Industrial Corp. which do not increase the height significantly.

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC1147 series. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and "on" resistance $R_{DS(ON)}$.

The minimum input voltage determines whether a standard threshold or logic-level threshold MOSFET must be

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used. For V_{IN} > 8V, a standard threshold MOSFET ($V_{GS(TH)}$ < 4V) may be used. If V_{IN} is expected to drop below 8V, a logic-level threshold MOSFET ($V_{GS(TH)}$ < 2.5V) is strongly recommended. When a logic-level MOSFET is used, the LTC1147 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFET.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the power MOSFET. When the LTC1147 series is operating in continuous mode, the simplifying assumption can be made that either the MOSFET or Schottky diode is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Schottky Diode Duty Cycle} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}}$$

From the duty cycle the required $R_{DS(ON)}$ for the MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{(V_{IN})(P_P)}{(V_{OUT})(I_{MAX}^2)(1 + \delta_P)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependency of $R_{DS(ON)}$. P_P will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.007/°C can be used as an approximation for low voltage MOSFETs.

Output Diode Selection (D1)

The Schottky diode D1 shown in Figure 1 only conducts during the off-time. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

The most stressful condition for the output diode is under short circuit (V_{OUT} = 0V). Under this condition the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions the average current conducted by the diode is:

$$I_{D1} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}} (I_{LOAD})$$

Remember to keep lead lengths short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

The forward voltage drop allowable in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(PK)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements (see Efficiency Considerations).

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic decoupling capacitor is also required on V_{IN} (Pin 1) for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1147:*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

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Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1147 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

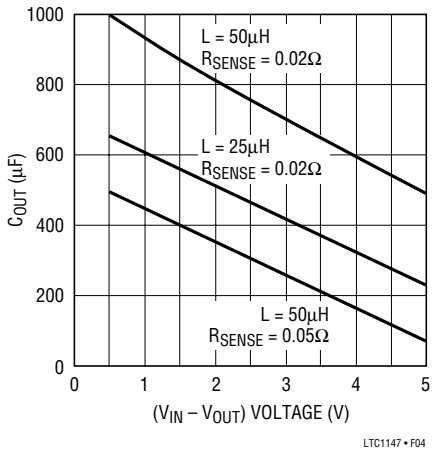

Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD}(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

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where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1147 circuits: 1) LTC1147 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, and 4) voltage drop of the Schottky diode.

1. The DC supply current is the current which flows into V_{IN} (Pin 1) less the gate charge current. For V_{IN} = 10V the LTC1147 series DC supply current is 160μA for no load, and increases proportionally with load up to a constant 1.6mA after the LTC1147 series has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_P)$. The typical gate charge for a 0.135Ω P-channel power MOSFET is 40nC. This results in $I_{GATECHG}$ = 4mA in 100kHz continuous operation for a 2% to 3% typical midcurrent loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and Schottky diode. The MOSFET $R_{DS(ON)}$ multiplied by the P-channel duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω at $V_{IN} \approx 2V_{OUT}$. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4. The Schottky diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage drop times the Schottky diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A.

   Figure 5 shows how the efficiency losses in a typical LTC1147 series regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the midcurrent region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses and Schottky diode loss dominate at high load currents.

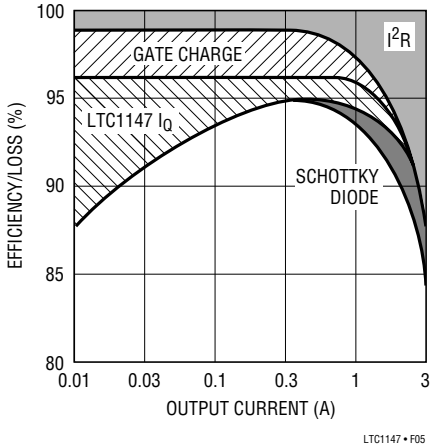

Figure 5. Efficiency Loss

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Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 5V (nominal), V_{OUT} = 3.3V, I_{MAX} = 1A, and f = 130kHz; R_{SENSE}, C_T and L can immediately be calculated:

$R_{SENSE} = 100mV/1A = 0.1\Omega$

$t_{OFF} = (1/130kHz)[1 – (3.3/5)] = 2.61\mu s$

$C_T = 2.61\mu s/(1.3)(10^4) = 220pF$

$L = (5.1)(10^5)(0.1\Omega)(220pF)(3.3V) = 33\mu H$

Assume that the MOSFET dissipation is to be limited to P_P = 250mW.

If T_A = 50°C and the thermal resistance of the MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = 0.007(63 – 25) = 0.27$. The required $R_{DS(ON)}$ for the MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{5(0.25)}{3.3(1)^2\,(1.27)} = 0.3\Omega$$

The P-channel requirement can be met by a Si9430DY. Note that the most stringent requirement for the Schottky diode is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst-case Schottky diode dissipation rises to:

$$P_D = I_{SC(AVG)}(V_D)$$

With the 0.1Ω sense resistor $I_{SC(AVG)}$ = 1A will result, increasing the 0.4V Schottky diode dissipation to 0.4W.

C_{IN} will require an RMS current rating of at least 0.5A at temperature, and C_{OUT} will require an ESR of 0.1Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time, causing the power dissipation to increase. At $V_{IN(MIN)}$ = 4.5V, the frequency will decrease and the P-channel will be conducting most of the time causing its power dissipation to increase. At $V_{IN(MIN)}$ = 4.5V:

$$f_{MIN} = \frac{1}{2.61\mu s}\left(1 - \frac{3.3}{4.5}\right) = 102kHz$$

$$P_P = \frac{3.3(0.125\Omega)(1A)^2(1.27)}{4.5} = 116mW$$

This last step is necessary to assure that the power dissipation and junction temperature of the P-channel are not exceeded.

Troubleshooting Hints

Since efficiency is critical to LTC1147 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor Pin 2.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 6a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 6b. During this time the LTC1147 series are in sleep mode with the quiescent current reduced to 160μA.

The inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Burst Mode operation.

Figure 6a. Continuous Mode Operation C_T Waveform

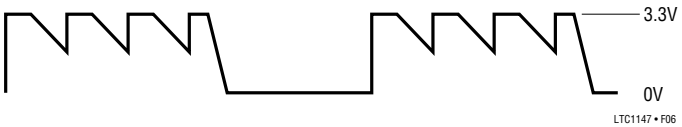

Figure 6b. Burst Mode Operation C_T Waveform

If Pin 2 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

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Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1147 series. These items are also illustrated graphically in the layout diagram of Figure 7. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1147 ground (Pin 7) must return separately to a) the power and b) signal grounds. The power ground (a) returns to the source anode of the Schottky diode and (–) plate of C_{IN}, which should have lead lengths as short as possible. The signal ground (b) connects to the (–) plate of C_{OUT}.
2. Does the LTC1147 SENSE$^-$ (Pin 4) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?
3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 4 and 5 should be as close as possible to the LTC1147.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.
5. Is the input decoupling capacitor (0.1µF/1µF) connected closely between V_{IN} (Pin 1) and ground (Pin 7)? This capacitor carries the MOSFET driver peak currents.
6. On fixed output versions, is the SHDN (Pin 6) actively pulled to ground during normal operation? The SHDN pin is high impedance and must not be allowed to float.

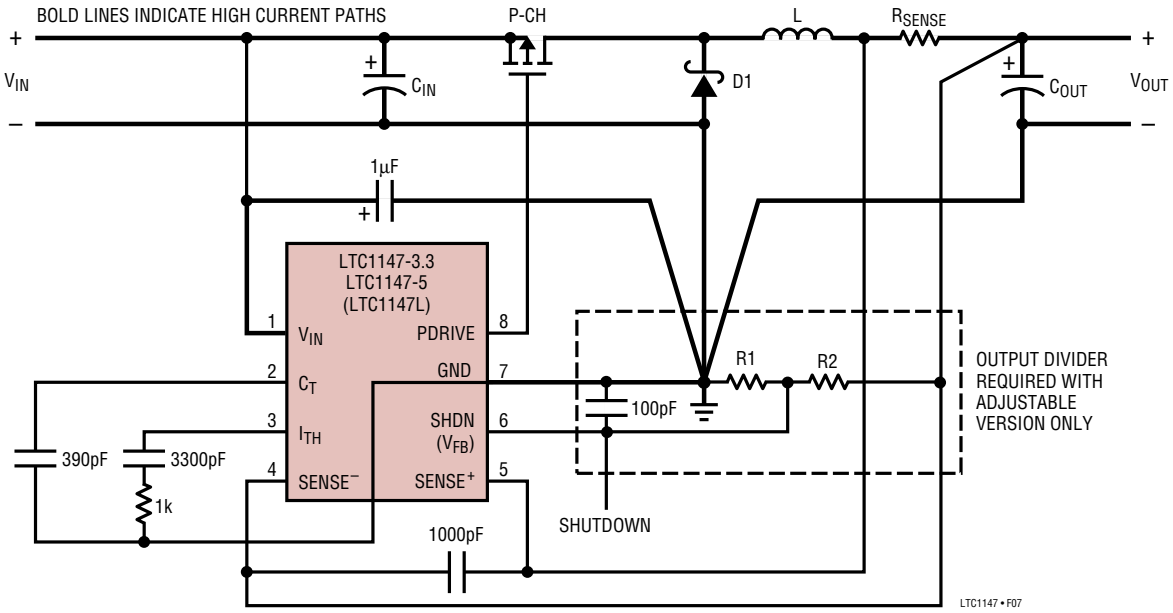
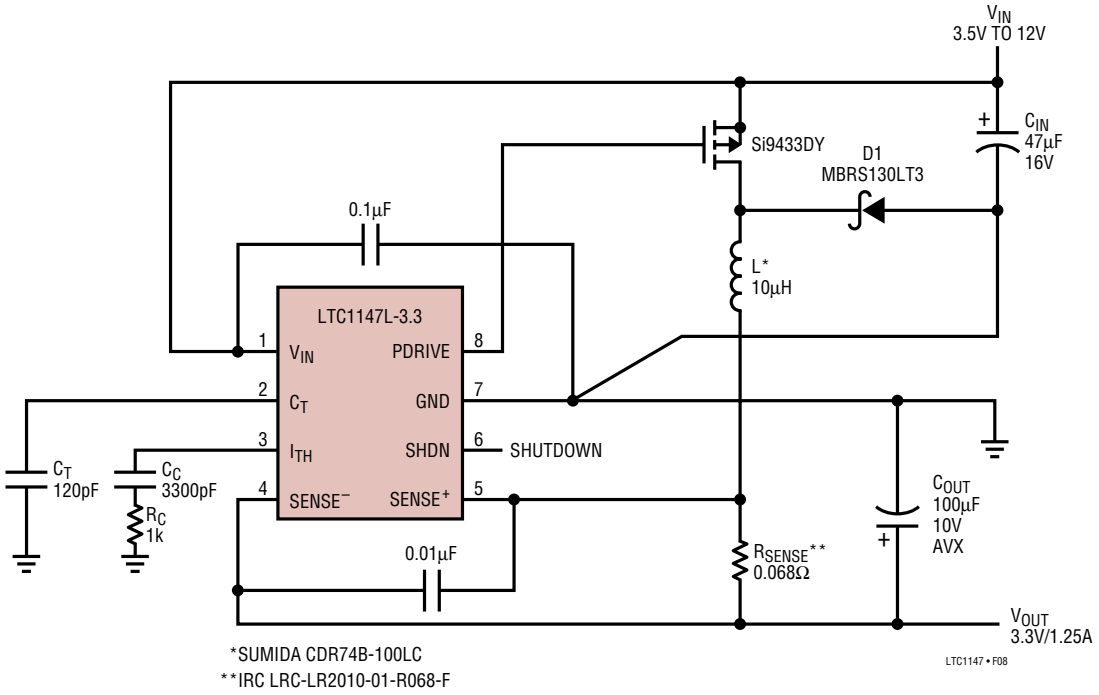


Figure 7. LTC1147 Layout Diagram (See Board Layout Checklist)

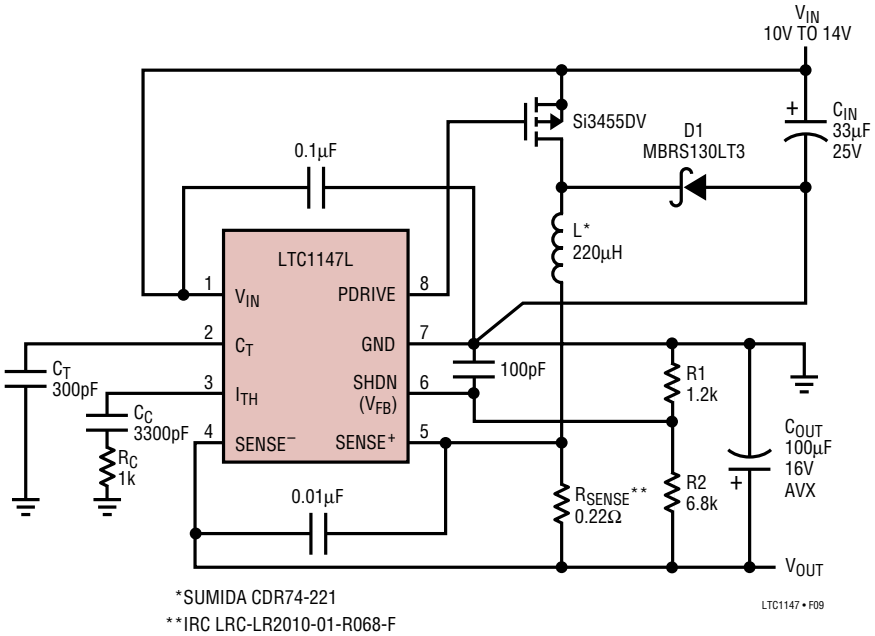
For additional High Efficiency application circuits see Application Note 54.

TYPICAL APPLICATIONS

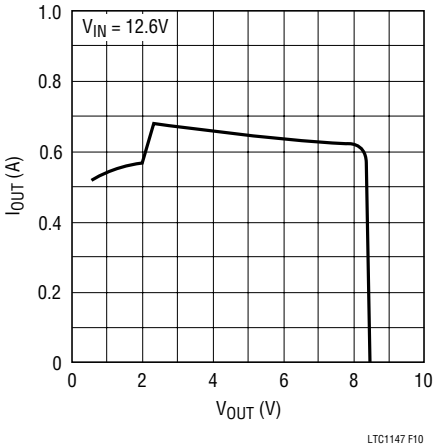
3.3V Low Dropout High Efficiency Regulator



Precision Constant Current Source

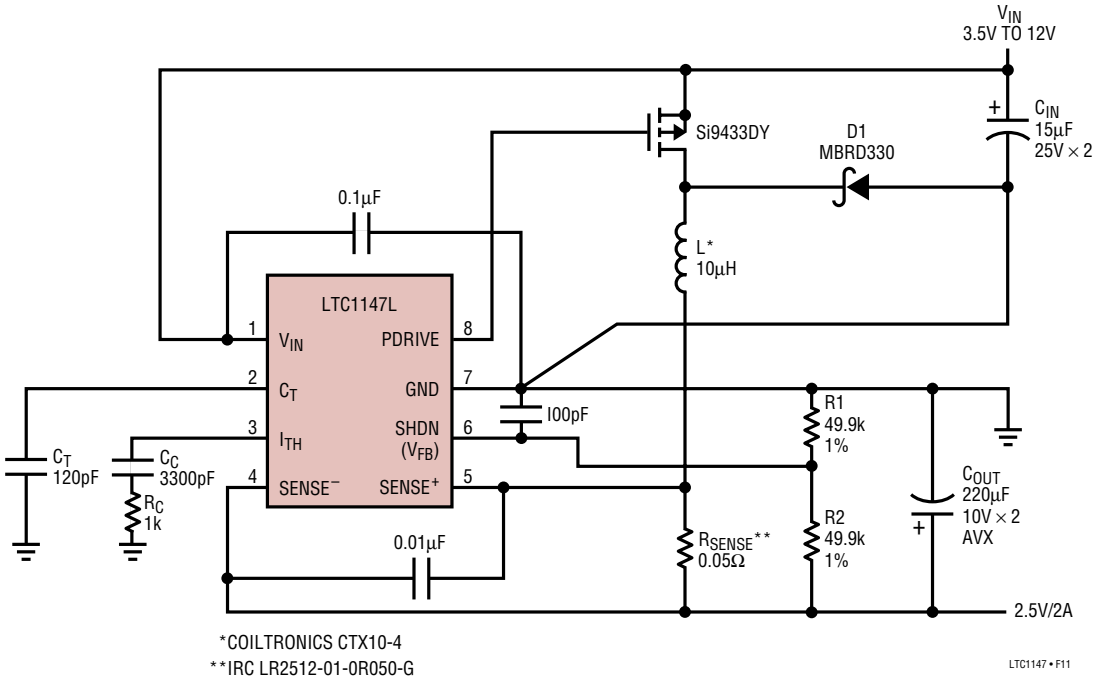


IOUT vs VOUT For Figure 9



TYPICAL APPLICATIONS

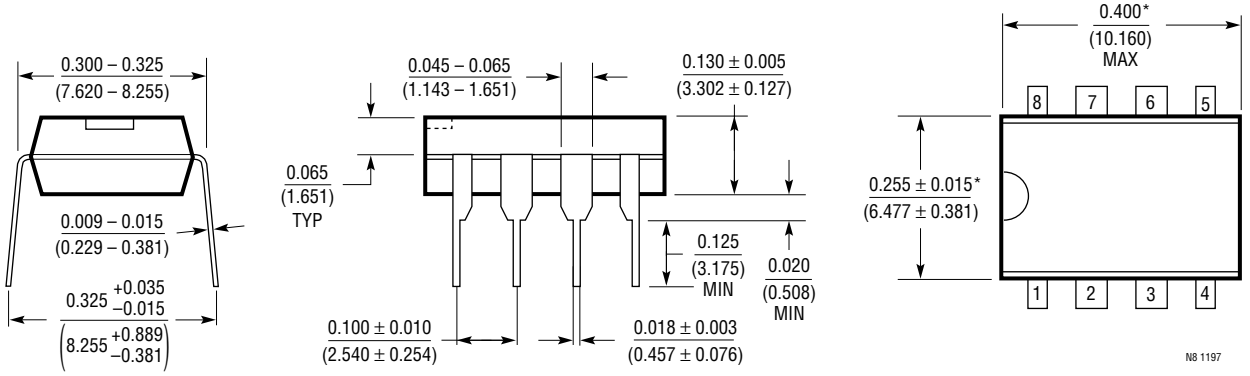
2.5V/2A Regulator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

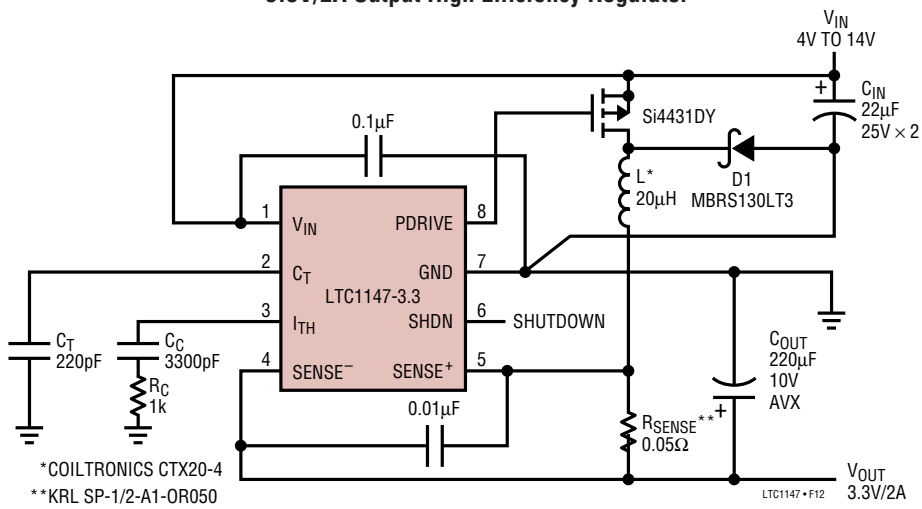
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

TYPICAL APPLICATION

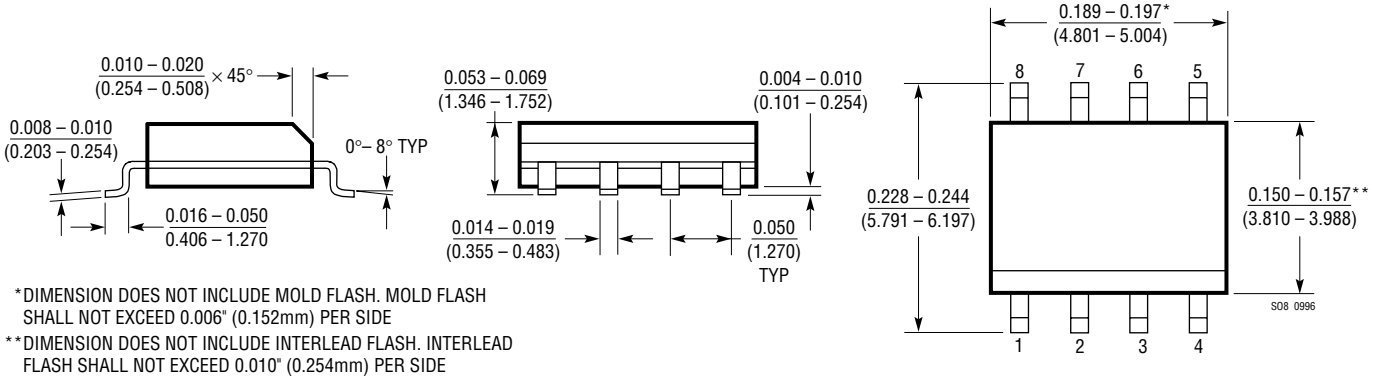
3.3V/2A Output High Efficiency Regulator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulator	Dual Version of LTC1148
LTC1143	Dual High Efficiency Step-Down Switching Regulator Controller	Dual Version of LTC1147
LTC1147	High Efficiency Step-Down Switching Regulator Controller	Nonsynchronous, 8-Lead, $V_{IN} \leq 16V$
LTC1148	High Efficiency Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	High Efficiency Step-Down Switching Regulator	Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs
LTC1159	High Efficiency Step-Down Switching Regulator	Synchronous, $V_{IN} \leq 40V$ for Logic Level MOSFETS
LTC1174	High Efficiency Step-Down and Inverting DC/DC Converter	0.5A Switch, $V_{IN} \leq 18.5V$, Comparator
LTC1265	High Efficiency Step-Down DC/DC Converter	1.2A Switch, $V_{IN} \leq 13V$, Comparator
LTC1267	Dual High Efficiency Synchronous Step-Down Switching Regulators	Dual Version of LTC1159
LTC1435	High Efficiency Low Noise Synchronous Step-Down Switching Regulator	16-Pin Narrow SO/SSOP; Constant Frequency

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