THE DATASHEET OF

LMX2324TMX/NOPB

LMX2324 PLLatinum™ 2.0 GHz Frequency Synthesizer for RF Personal Communications

Check for Samples: LMX2324

FEATURES

- **RF Operation up to 2.0 GHz**
- **2.7V to 5.5V Operation**
- **Low Current Consumption: I_{CC} = 3.5 mA (typ) at V_{CC} = 3.0V**
- **Dual Modulus Prescaler: 32/33**
- **Internal Balanced, Low Leakage Charge Pump**

APPLICATIONS

- **Cellular Telephone Systems (GSM, NADC, CDMA, PDC)**
- **Personal Wireless Communications (DCS-1800, DECT, CT-1+)**
- **Wireless Local Area Networks (WLANs)**
- **Other Wireless Communication Systems**

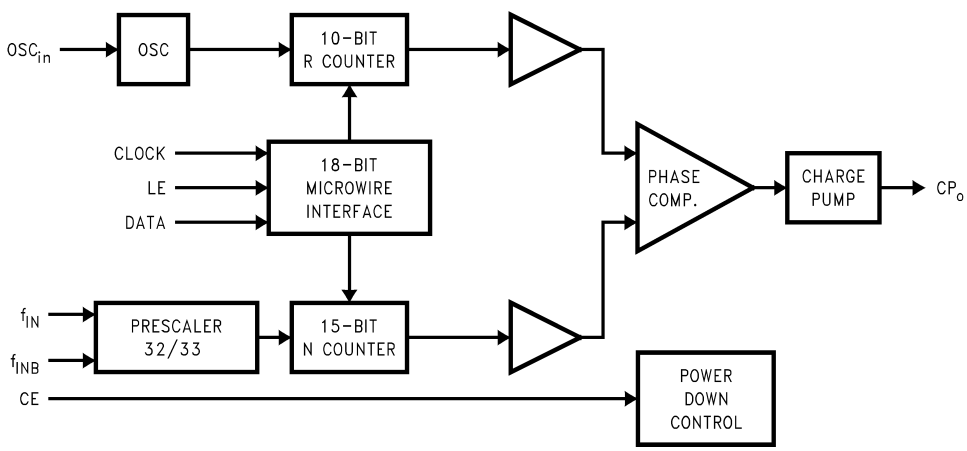
DESCRIPTION

The LMX2324 is a high performance frequency synthesizer with integrated 32/33 dual modulus prescaler designed for RF operation up to 2.0 GHz. Using a proprietary digital phase locked loop technique, the LMX2324's linear phase detector characteristics can generate very stable, low noise control signals for UHF and VHF voltage controlled oscillators.

Serial data is transferred into the LMX2324 via a three-line MICROWIRE interface (Data, LE, Clock). Supply voltage range is from 2.7V to 5.5V. The LMX2324 features very low current consumption, typically 3.5 mA at 3V. The charge pump provides 4 mA output current.

The LMX2324 is manufactured using TI's ABiC V BiCMOS process and is packaged in a 16-pin TSSOP and a 16-pin PLGA package.

Functional Block Diagram



Connection Diagram

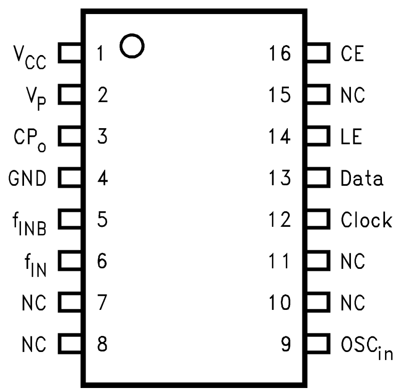


Figure 1. TSSOP 16-Pin Package
See Package Number PW0016A

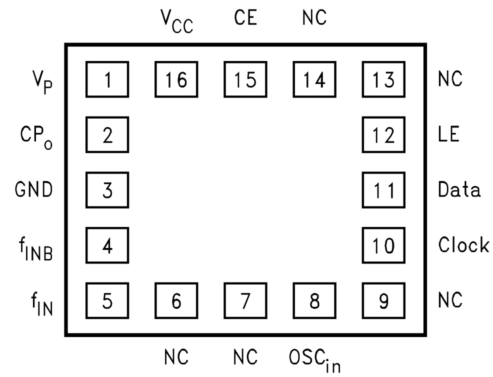


Figure 2. PLGA 16-Pin Package
See Package Number NPG0016A

PIN DESCRIPTIONS

Pin No.		Pin Name	I/O	Description
TSSOP16	PLGA16			
2	1	V_P	—	Power supply for charge pump. Must be ≥ V_{CC}
3	2	CP_o	O	Internal charge pump output. For connection to a loop filter for driving the voltage control input of an external oscillator.
4	3	GND	—	Ground.
5	4	f_{INB}	I	RF prescaler complimentary input. In single-ended mode, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The LMX2324 can be driven differentially when the bypass capacitor is omitted.
6	5	f_{IN}	I	RF prescaler input. Small signal input from the voltage controlled oscillator.
7	6	NC		No Connect
8	7	NC		No Connect
9	8	OSC_{in}	I	Oscillator input. A CMOS inverting gate input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
10	9	NC		No Connect
12	10	Clock	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, for the various counters and registers.
13	11	Data	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
14	12	LE	I	Load Enable input. When Load Enable transitions HIGH, data is loaded into either the N or R register (control bit dependent). See Serial Data Input Timing.
15	13	NC		No Connect
11	14	NC		No Connect
16	15	CE	I	CHIP Enable. A LOW on CE powers down the device asynchronously and will TRI-STATE the charge pump output.
1	16	V_{CC}	I	Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Power Supply Voltage (V_{CC})	−0.3V to 6.5V
Power Supply for Charge Pump (V_P)	V_{CC} to 6.5V
Voltage on Any Pin with	
GND = 0V (V_I)	−0.3V to V_{CC} + 0.3V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (solder, 4 sec.) (T_L)	+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) This device is a high performance RF integrated circuit with an ESD rating < 2kV. and is ESD sensitive. Handling and assembly of this device should on be done on ESD protected workstations.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions [1]

Power Supply Voltage (V_{CC})	2.7V to 5.5V
Power Supply for Charge Pump (V_P)	V_{CC} to 5.5V
Operating Temperature (T_A)	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

(V_{CC} = 3V, V_P = 3V; −40°C < T_A < 85°C except as specified).
All min/max specifications are ensured by design, or test, or statistical methods.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GENERAL						
I_{CC}	Power Supply Current	V_{CC} = 2.7V to 5.5V		3.5		mA
I_{CC}-PWDN	Power Down Current			10		µA
f_{IN}	f_{IN} Operating Frequency		0.1		2.0	GHz
OSC_{in}	Oscillator Operating Frequency		5		40	MHz
f_{PD}	Phase Detector Frequency				10	MHz
Pf_{IN}	Input Sensitivity f_{INB} grounded through a 10 pF capacitor	V_{CC} = 3.0V	−15		0	dBm
		V_{CC} = 5.0V	−10		0	
V_{OSC}	Oscillator Sensitivity		0.4	1.0	V_{CC}−0.3	V_{PP}
CHARGE PUMP						
$ICP_{o\text{-}source}$	Charge Pump Output Current	$VCP_o = V_P/2$		−4.0		mA
$ICP_{o\text{-}sink}$				4.0		mA
$ICP_{o\text{-}Tri}$	Charge Pump TRI-STATE Current	$0.5 \le VCP_o \le V_P - 0.5$ T = 25°C		0.1		nA
ICP_o vs. VCP_o	Charge Pump Output Current Variation vs. Voltage [1]	$0.5 \le VCP_o \le V_P - 0.5$ T = 25°C		10		%
$ICP_{o\text{-}sink}$ vs. $ICP_{o\text{-}source}$	Charge Pump Output Current Sink vs. Source Mismatch [1]	$VCP_o = V_P/2$ T = 25°C		5		%
ICP_o vs. T	Charge Pump Output Current Magnitude Variation vs. Temperature [1]	$VCP_o = V_P/2$ −40°C ≤ T ≤ +85°C		10		%

(1) See related equations in Charge Pump Current Specification Definitions

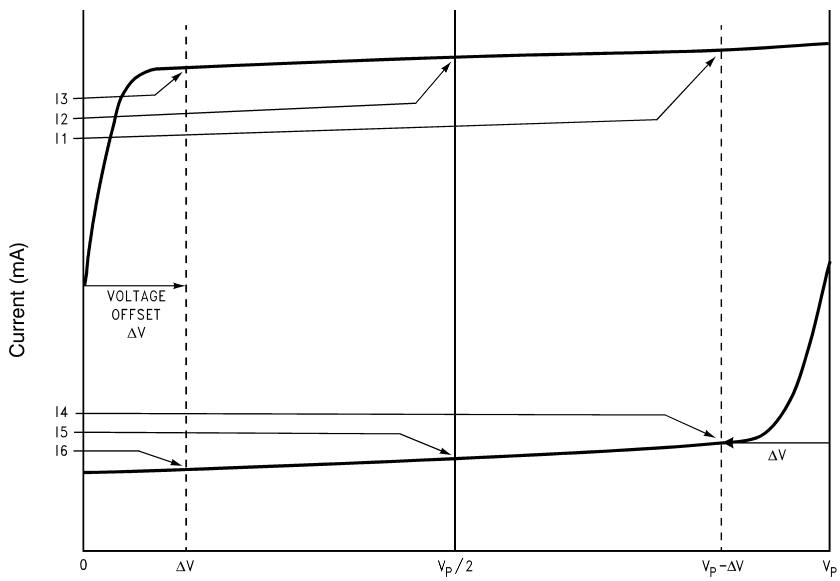
Electrical Characteristics (continued)

(V_{CC} = 3V, V_P = 3V; −40°C < T_A < 85°C except as specified).
All min/max specifications are ensured by design, or test, or statistical methods.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE (DATA, CLK, LE, CE)						
V_{IH}	High-Level Input Voltage	(2)	0.8 V_{CC}			V
V_{IL}	Low-Level Input Voltage	(2)			0.2 V_{CC}	V
I_{IH}	High-Level Input Current	$V_{IH} = V_{CC}$ = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0, V_{CC} = 5.5V	−1.0		1.0	µA
I_{IH}	Oscillator Input Current	$V_{IH} = V_{CC}$ = 5.5V			100	µA
I_{IL}		V_{IL} = 0, V_{CC} = 5.5V	−100			µA
MICROWIRE TIMING						
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

(2) Except f_{IN} and OSC_{in}

Charge Pump Current Specification Definitions



I1 = CP sink current at $VCP_o = V_P - \Delta V$
I2 = CP sink current at $VCP_o = V_P/2$
I3 = CP sink current at $VCP_o = \Delta V$
I4 = CP source current at $VCP_o = V_P - \Delta V$
I5 = CP source current at $VCP_o = V_P/2$
I6 = CP source current at $VCP_o = \Delta V$
ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_P and ground. Typical values are between 0.5V and 1.0V.

1. ICP_o vs. VCP_o = Charge Pump Output Current magnitude variation vs. Voltage =
   [½ * {|I1| − |I3|}]/[½ * {|I1| + |I3|}] * 100% and [½ * {|I4| − |I6|}]/[½ * {|I4| + |I6|}] * 100%
2. $ICP_{o\text{-sink}}$ vs. $ICP_{o\text{-source}}$ = Charge Pump Output Current Sink vs. Source Mismatch =
   [|I2| − |I5|]/[½ * {|I2| + |I5|}] * 100%
3. ICP_o vs. T = Charge Pump Output Current magnitude variation vs. Temperature =
   [|I2 @ temp| − |I2 @ 25°C|]/|I2 @ 25°C| * 100% and [|I5 @ temp| − |I5 @ 25°C|]/|I5 @ 25°C| * 100%

FUNCTIONAL DESCRIPTION

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the Texas Instruments LMX2324, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency that sets the comparison frequency. This reference signal, f_r, is then presented to the input of a phase/frequency detector and compared with another signal, f_p, the feedback signal, which was obtained by dividing the VCO frequency down by way of the N counter. The phase/frequency detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The phase/frequency comparator's function is to adjust the voltage presented to the VCO until the feedback signal's frequency (and phase) match that of the reference signal. When this “phase-locked” condition exists, the RF VCO's frequency will be N times that of the comparison frequency, where N is the divider ratio.

OSCILLATOR

The reference oscillator frequency for the PLL is provided by an external reference TCXO through the OSC_{in} pin. OSC_{in} block can operate to 40 MHz with a minimum input sensitivity of $0.4V_{PP}$. The inputs have a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.

REFERENCE DIVIDERS (R COUNTER)

The R Counter is clocked through the oscillator block. The maximum frequency is 40 MHz. The R Counter is a 10 bit CMOS binary counter with a divide range from 2 to 1,023. See 10-Bit Programmable Reference Divider Ratio (R Counter).

PROGRAMMABLE DIVIDERS (N COUNTER)

The N counter is clocked by the small signal f_{IN} and f_{INB} input pins. The LMX2324 RF N counter is 15 bit integer divider. The N counter is configured as a 5 bit A Counter and a 10 bit B Counter, offering a continuous integer divide range from 992 to 32,767. The LMX2324 is capable of operating from 100 MHz to 2.0 GHz with a 32/33 prescaler.

Prescaler

The RF inputs to the prescaler consist of the f_{IN} and f_{INB} pins which are the complimentary inputs of a differential pair amplifier. The differential f_{IN} configuration can operate to 2 GHz with an input sensitivity of −15 dBm. The input buffer drives the N counter's ECL D-type flip flops in a dual modulus configuration. A 32/33 prescale ratio is provided for the LMX2324. The prescaler clocks the subsequent CMOS flip-flop chain comprising the fully programmable A and B counters.

PHASE/FREQUENCY DETECTOR

The phase(/frequency) detector is driven from the N and R counter outputs. The maximum frequency at the phase detector inputs is 10 MHz. The phase detector outputs control the charge pumps. The polarity of the pump-up or pump-down control is programmed using PD_POL, depending on whether RF VCO characteristics are positive or negative (see R Register Truth Table). The phase detector also receives a feedback signal from the charge pump, in order to eliminate dead zone.

CHARGE PUMP

The phase detector's current source output pumps charge into an external loop filter, which then converts the charge into the VCO's control voltage. The charge pumps steer the charge pump output, CP_o, to V_P (pump-up) or Ground (pump-down). When locked, CP_o is primarily in a TRI-STATE mode with small corrections. The RF charge pump output current magnitude is set to 4.0 mA. The charge pump output can also be used to output divider signals as detailed in Test Mode Truth Table (R[13] = 1).

MICROWIRE SERIAL INTERFACE

The programmable functions are accessed through the MICROWIRE serial interface. The interface is made of three functions: clock, data and latch enable (LE). Serial data for the various counters is clocked in from data on the rising edge of clock, into the 18-bit shift register. Data is entered MSB first. The last bit decodes the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the two appropriate latches (selected by address bits). A complete programming description is included in the following sections.

POWER CONTROL

The PLL can be power controlled in two ways. The first method is by setting the CE pin LOW. This asynchronously powers down the PLL and TRI-STATE the charge pump output, regardless of the PWDN bit status. The second method is by programming through MICROWIRE, while keeping the CE HIGH. Programming the PWDN bit in the N register HIGH (CE=HIGH) will disable the N counter and de-bias the f_{IN} input (to a high impedance state). The R counter functionality also becomes disabled. The reference oscillator block powers down when the power down bit is asserted. The OSC_{in} pin reverts to a high impedance state when this condition exists. Power down forces the charge pump and phase comparator logic to a TRI-STATE condition. A power down counter reset function resets both N and R counters. Upon powering up the N counter resumes counting in “close” alignment with the R counter (The maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

Programming Description

MICROWIRE INTERFACE

The LMX2324 register set can be accessed through the MICROWIRE interface. A 18-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a 17-bit DATA[16:0] field and a 1-bit address (ADDR) field as shown below. The address field is used to decode the internal register address. Data is clocked into the shift register in the direction from MSB to LSB, when the CLOCK signal goes high. On the rising edge of Load Enable (LE) signal, data stored in the shift register is loaded into the addressed latch.

MSB					LSB
DATA[16:0]			ADDR		
17		1		0	

Registers' Address Map

When Load Enable (LE) is transitioned high, data is transferred from the 18-bit shift register into the appropriate latch depending on the state of the ADDRESS bit. A multiplexing circuit decodes the address bit and writes the data field to the corresponding internal register.

REGISTER ADDRESSED	**ADDRESS BIT ADDR**
R Register	1
N Register	0

Register Content Truth Table

	MSB				**SHIFT REGISTER BIT LOCATION**												**LSB**
	17	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register	*Data Field*																	ADDR Field
N	NB_CNTR[9:0]										NA_CNTR[4:0]					CTL_WORD[1:0]		0
	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	
R	X	X	X	TEST	RS	PD_POL	CP_TRI	R_CNTR[9:0]										1
	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	

R REGISTER

If the Address Bit (ADDR) is 1, when LE is transitioned high data is transferred from the 18-bit shift register into the 14-bit R register. The R register contains a latch which sets the PLL 10-bit R counter divide ratio. The divide ratio is programmed using the bits R_CNTR as shown in 10-Bit Programmable Reference Divider Ratio (R Counter). The ratio must be ≥ 2. The PD_POL, CP_TRI and TEST bits control the phase detector polarity, charge pump TRI-STATE, and test mode respectively, as shown in R Register Truth Table. The RS bit is reserved and should always be set to zero. X denotes a don't care condition. Data is clocked into the shift register MSB first.

	MSB				**SHIFT REGISTER BIT LOCATION**											**LSB**	
	17	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register	*Data Field*																	ADDR Field
R	X	X	X	TEST	RS	PD_POL	CP_TRI	R_CNTR[9:0]										1
	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	

10-Bit Programmable Reference Divider Ratio (R Counter)(1)

R_CNTR[9:0]										
Divide Ratio	**R9**	**R8**	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•
1,023	1	1	1	1	1	1	1	1	1	1

(1) **Notes:** Divide ratio: 2 to 1,023 (Divide ratios less than 2 are prohibited)
R_CNTR—These bits select the divide ratio of the programmable reference dividers.

R Register Truth Table

Bit	Location	Function	0	1
CP_TRI	R[10]	Charge Pump TRI-STATE	Normal Operation	TRI-STATE
PD_POL	R[11]	Phase Detector Polarity	Negative	Positive
TEST	R[13]	Test Mode Bit	Normal Operation	Test Mode

If the test mode is NOT activated (R[13]=0), the charge pump is active when CP_TRI is set LOW. When CP_TRI is set HIGH, the charge pump output and phase comparator are forced to a TRI-STATE condition. This bit must be set HIGH if the test mode is ACTIVATED (R[13]=1).

If the test mode is NOT activated (R[13]=0), PD_POL sets the VCO characteristics to positive when set HIGH. When PD_POL is set LOW, the VCO exhibits a negative characteristic where the VCO frequency decreases with increasing control voltage.

If the test mode is ACTIVATED (R[13]=1), the outputs of the N and R counters are directed to the CP_o output to allow for testing. The PD_POL bit selects which counter output according to Test Mode Truth Table (R[13] = 1).

Test Mode Truth Table (R[13] = 1)

CP_o Output	CP_TRI R[10]	PD_POL R[11]
R Divider Output	1	0
N Divider Output	1	1

N REGISTER

If the address bit is LOW (ADDR=0) when LE is transitioned high, data is transferred from the 18-bit shift register into the 17-bit N register. The N register consists of the 5-bit swallow counter (A counter), the 10-bit programmable counter (B counter) and the control word. Serial data format is shown below in 5-Bit Swallow Counter Divide Ratio (A Counter) and 10-Bit Programmable Counter Divide Ratio (B Counter). The pulse swallow function which determines the divide ratio is described in Pulse Swallow Function. Data is clocked into the shift register MSB first.

	MSB				SHIFT REGISTER BIT LOCATION											LSB
	17	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register	*Data Field*																	ADDR Field
N	NB_CNTR[9:0]										NA_CNTR[4:0]					CTL_WORD[1:0]		0
	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	

5-Bit Swallow Counter Divide Ratio (A Counter)[(1)]

Swallow Count	NA_CNTR[4:0]				
(A)	**N6**	**N5**	**N4**	**N3**	**N2**
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

(1) **Notes:** Swallow Counter Value: 0 to 31
NB_CNTR ≥ NA_CNTR

10-Bit Programmable Counter Divide Ratio (B Counter)[(1)]

NB_CNTR[10:0]										
Divide Ratio	**N16**	**N15**	**N14**	**N13**	**N12**	**N11**	**N10**	**N9**	**N8**	**N7**
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•
1023	1	1	1	1	1	1	1	1	1	1

(1) **Notes:** Divide ratio: 3 to 1,023 (Divide ratios less than 3 are prohibited)
NB_CNTR ≥ NA_CNTR

Pulse Swallow Function

The N divider counts such that it divides the VCO RF frequency by (P+1) A times, and then divides by P (B - A) times. The B value (NB_CNTR) must be ≥ 3. The continuous divider ratio is from 992 to 32,767. Divider ratios less than 992 are achievable as long as the binary counter value is greater than the swallow counter value (NB_CNTR ≥ NA_CNTR).

$f_{VCO} = N \times (f_{OSC}/R)$

$N = (P \times B) + A$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 10-bit programmable reference counter (2 to 1023)

N: Preset divide ratio of main 15-bit programmable integer N counter (992 to 32,767)

B: Preset divide ratio of binary 10-bit programmable B counter (3 to 1023)

A: Preset value of binary 5-bit swallow A counter (0 ≤ A ≤ 31, A ≤ B)

P: Preset modulus of dual modulus prescaler (P=32)

CTL_WORD

MSB			LSB
N1		N0	
CNT_RST		PWDN	

Control Word Truth Table(1)

CE	CNT_RST	PWDN	Function
1	0	0	Normal Operation
1	0	1	Synchronous Powerdown
1	1	0	Counter Reset
1	1	1	Asynchronous Powerdown
0	X	X	Asynchronous Powerdown

(1) **Notes:** X denotes don't care.

The **Counter Reset** enable bit when activated allows the reset of both N and R counters. Upon powering up the N counter resumes counting in “close” alignment with the R counter. (The maximum error is one prescaler cycle).

Both synchronous and asynchronous **power down** modes are available with the LMX2324 to be able to adapt to different types of applications. The MICROWIRE control register remains active and capable of loading and latching in data during all of the powerdown modes.

Synchronous Power down Mode

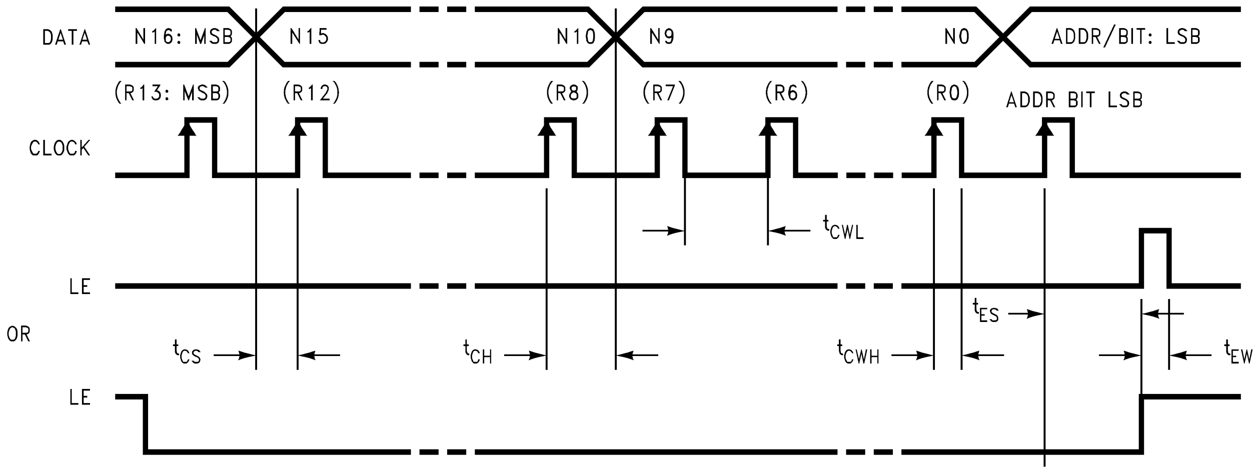
The PLL loops can be synchronously powered down by setting the counter reset mode bit to LOW (N[1] = 0) and its power down mode bit to HIGH (N[0] = 1). The power down function is gated by the charge pump. Once the power down mode and counter reset mode bits are loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power down Mode

The PLL loops can be asynchronously powered down by setting the counter reset mode bit to HIGH (N[1] = 1) and its power down mode bit to HIGH (N[0] = 1), or by setting CE pin LOW. The power down function is NOT gated by the charge pump. Once the power down and counter reset mode bits are loaded, the part will go into power down mode immediately.

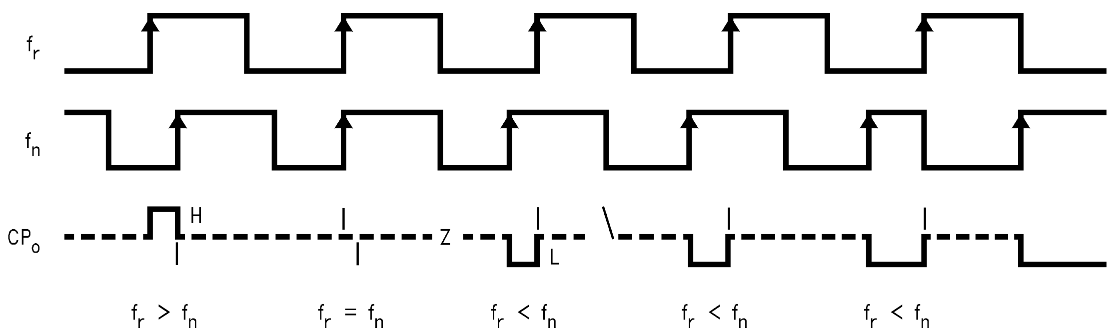
The R and N counters are disabled and held at load point during the synchronous and asynchronous power down modes. This will allow a smooth acquisition of the RF signal when the PLL is programmed to power up. Upon powering up, both R and N counters will start at the ‘zero' state, and the relationship between R and N will not be random.

Serial Data Input Timing



Notes: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.
Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 1.6V @ V_{CC} = 2.7V and 3.3V @ V_{CC} = 5.5V.

Phase Comparator and Internal Charge Pump Characteristics



Notes: Phase difference detection range: −2π to +2π
The minimum width pump up and pump down current pulses occur at the CP_o pin when the loop is locked. PD_POL = 1
f_R: Phase comparator input from the R Divider
f_N: Phase comparator input from the N divider
CP_o: Charge pump output

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	10