



**THE DATASHEET OF  
PMZB290UNE2YL**





# PMZB290UNE2

20 V, N-channel Trench MOSFET

24 March 2015

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Very fast switching
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Ultra thin package profile of 0.37 mm

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

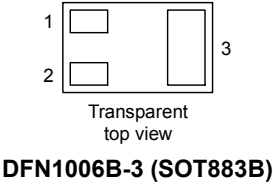
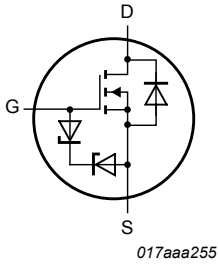
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	1.2	A
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 1.2\text{ A}; T_j = 25\text{ °C}$	-	270	320	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1006B-3 (SOT883B)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

### 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZB290UNE2	DFN1006B-3	DFN1006B-3: leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B

### 7. Marking

Table 4. Marking codes

Type number	Marking code
PMZB290UNE2	0101 0011

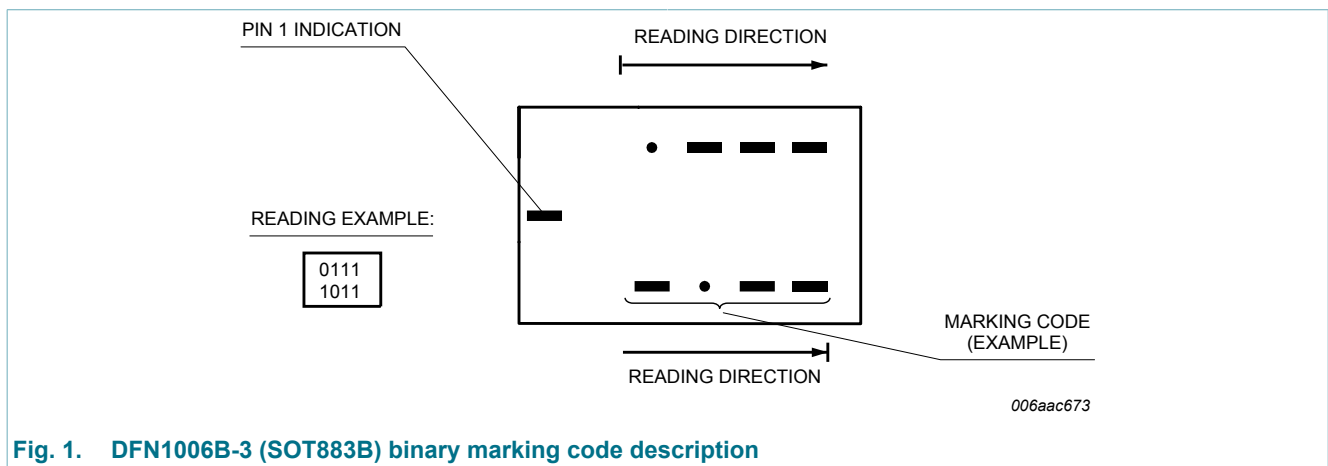


Fig. 1. DFN1006B-3 (SOT883B) binary marking code description

## 8. Limiting values

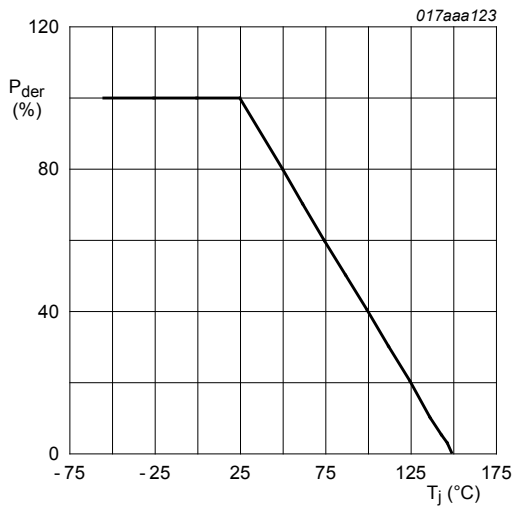
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	20	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	1.2	A
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	0.8	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	4	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	350	mW
			[1]	-	715	mW
		T <sub>sp</sub> = 25 °C		-	5430	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	0.7	A

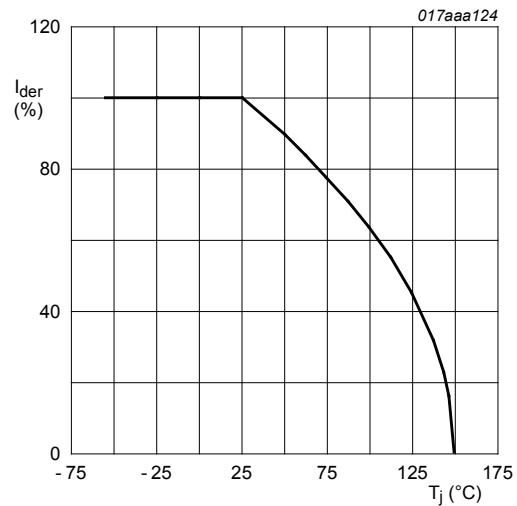
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



**Fig. 2. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$



**Fig. 3. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

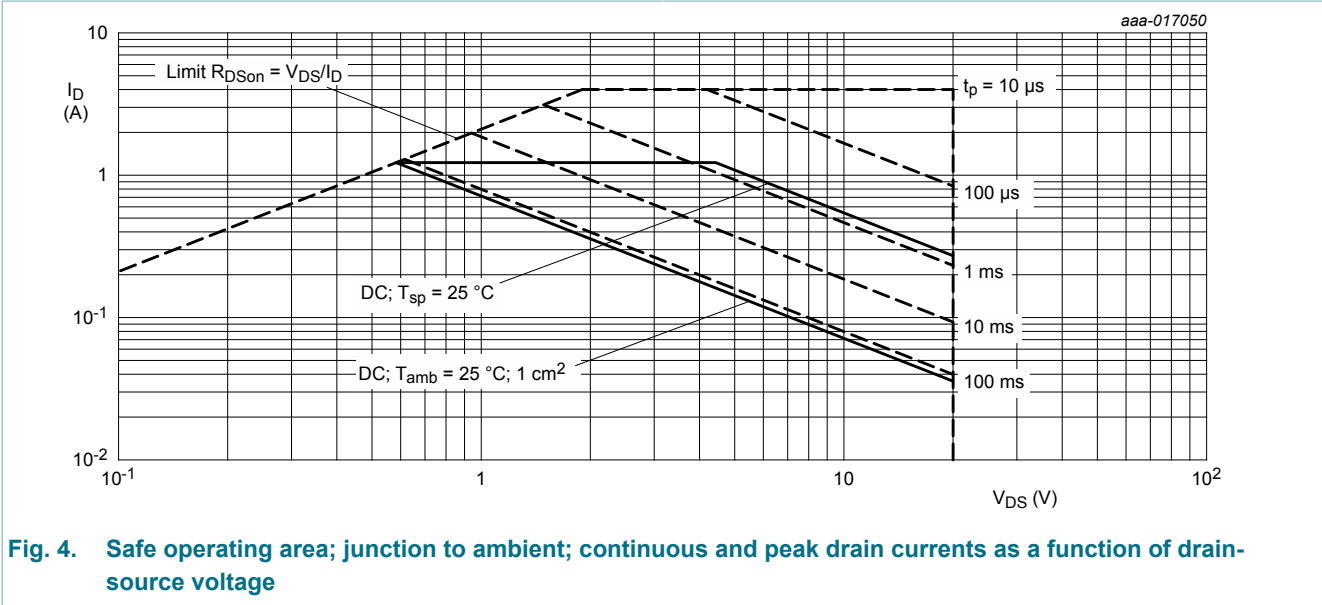


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

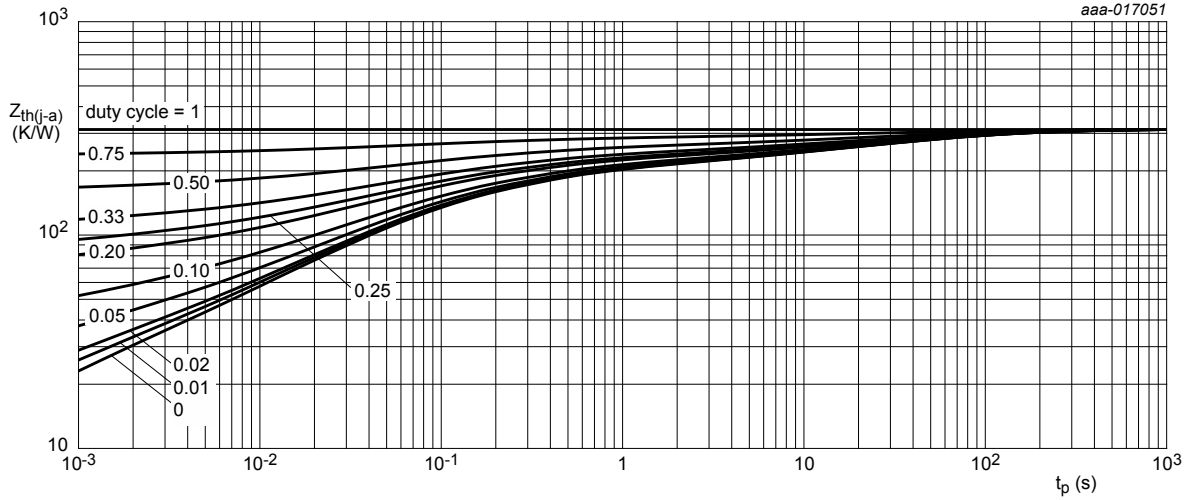
## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	315	360	K/W
			[2]	-	150	175	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	20	23	K/W

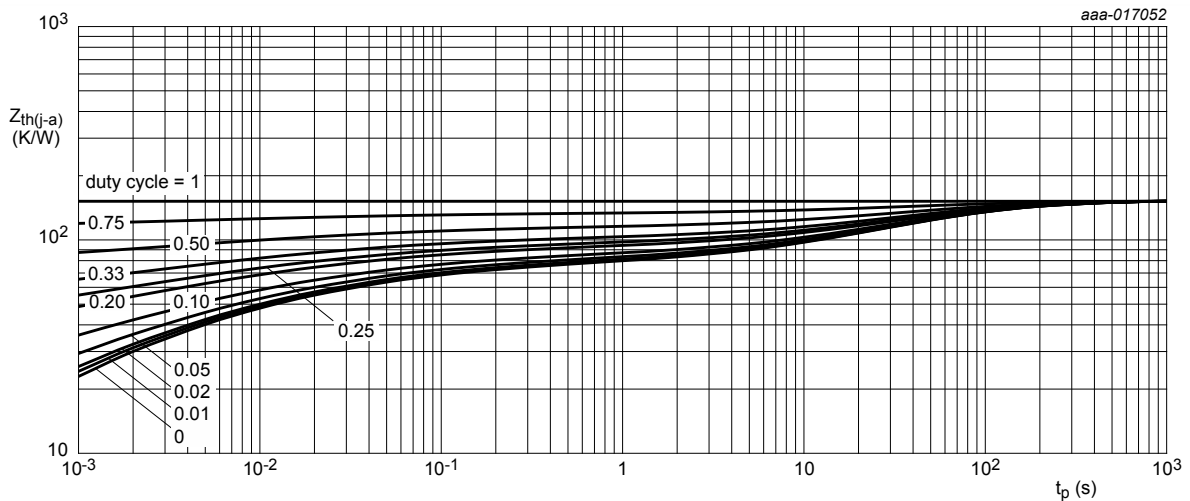
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



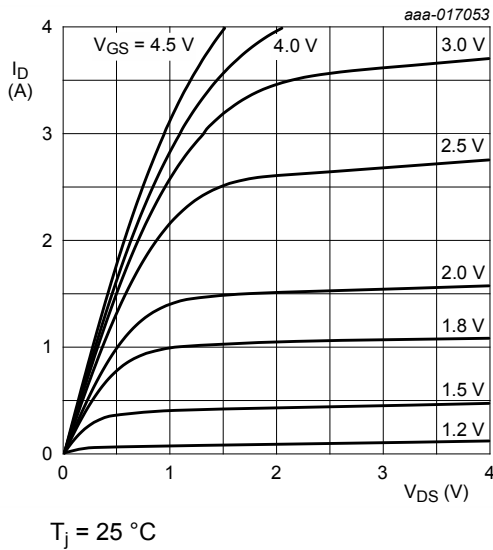
FR4 PCB, mounting pad for drain = 1 cm<sup>2</sup>

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

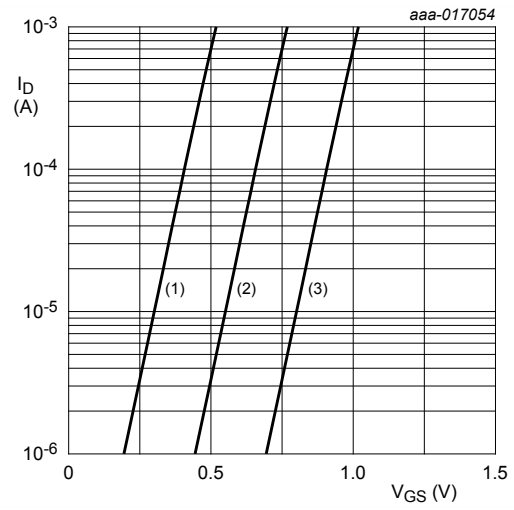
## 10. Characteristics

Table 7. Characteristics

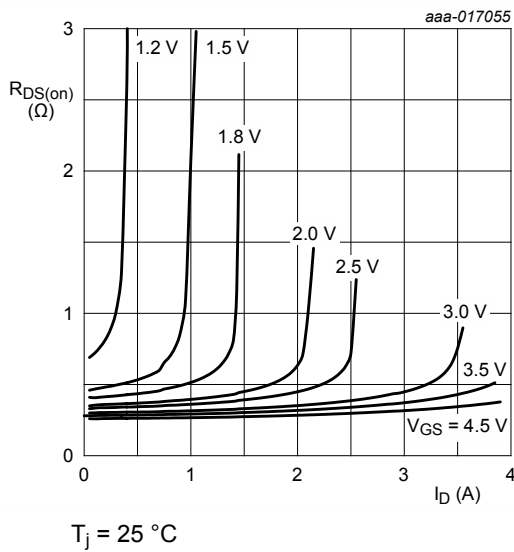
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	0.45	0.7	0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	5	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-5	$\mu A$
		$V_{GS} = 4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{GS} = -4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{GS} = 2.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 V$ ; $I_D = 1.2 A$ ; $T_j = 25 \text{ }^\circ C$	-	270	320	m $\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 1.2 A$ ; $T_j = 150 \text{ }^\circ C$	-	400	475	m $\Omega$
		$V_{GS} = 2.5 V$ ; $I_D = 1.0 A$ ; $T_j = 25 \text{ }^\circ C$	-	360	480	m $\Omega$
		$V_{GS} = 1.8 V$ ; $I_D = 0.12 A$ ; $T_j = 25 \text{ }^\circ C$	-	470	680	m $\Omega$
		$V_{GS} = 1.5 V$ ; $I_D = 0.01 A$ ; $T_j = 25 \text{ }^\circ C$	-	600	1190	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V$ ; $I_D = 1.23 A$ ; $T_j = 25 \text{ }^\circ C$	-	1.9	-	S
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V$ ; $I_D = 1.0 A$ ; $V_{GS} = 4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.8	1.4	nC
$Q_{GS}$	gate-source charge		-	0.1	-	nC
$Q_{GD}$	gate-drain charge		-	0.2	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	46	-	pF
$C_{oss}$	output capacitance		-	9.6	-	pF
$C_{rss}$	reverse transfer capacitance		-	7.7	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V$ ; $I_D = 1.0 A$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	6	-	ns
$t_r$	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	11	-	ns
$t_f$	fall time		-	4	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 0.7 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.9	1.2	V



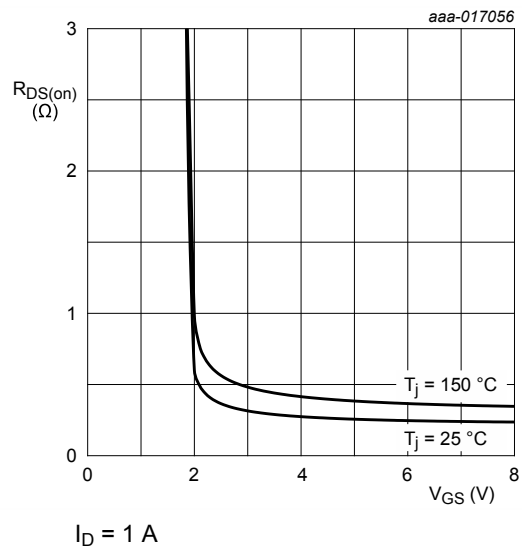
**Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values**



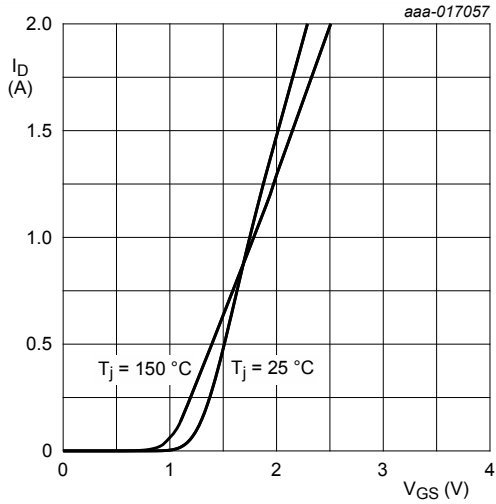
**Fig. 8. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 9. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

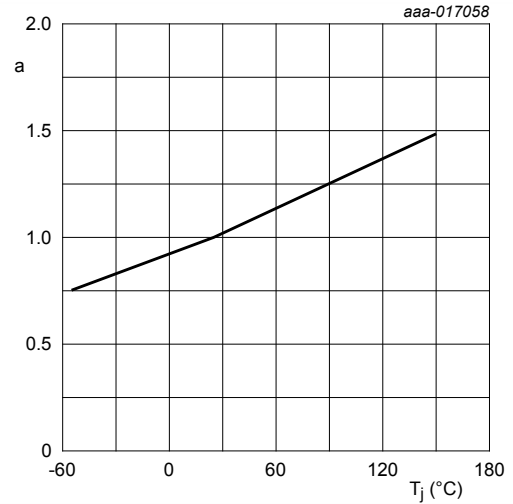
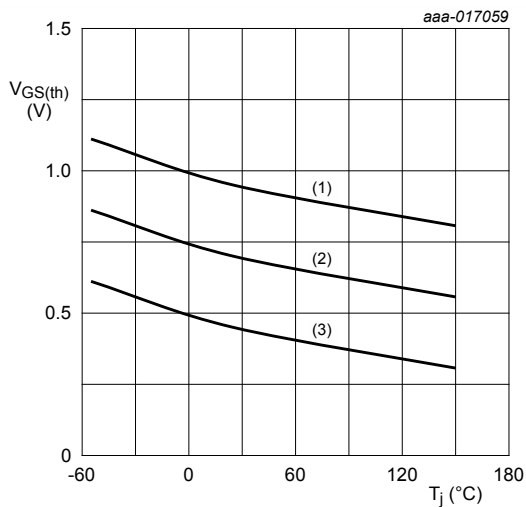


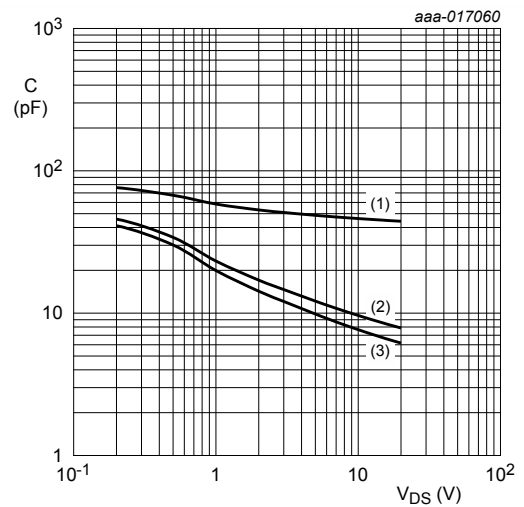
Fig. 12. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



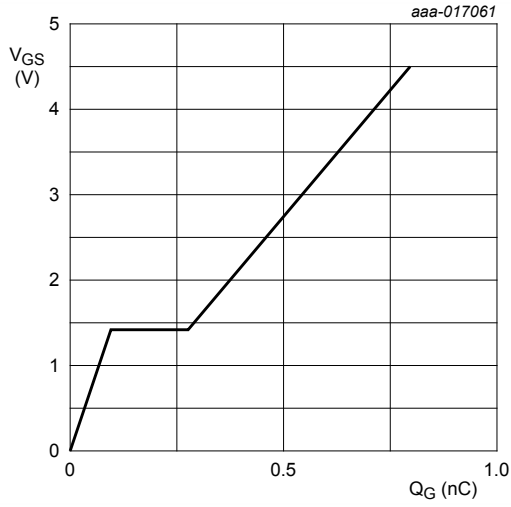
$I_D = 250 \mu A$ ;  $V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

Fig. 13. Gate-source threshold voltage as a function of ambient temperature



$f = 1 \text{ MHz}$ ;  $V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 10 \text{ V}; I_D = 0.5 \text{ A}$   
 $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

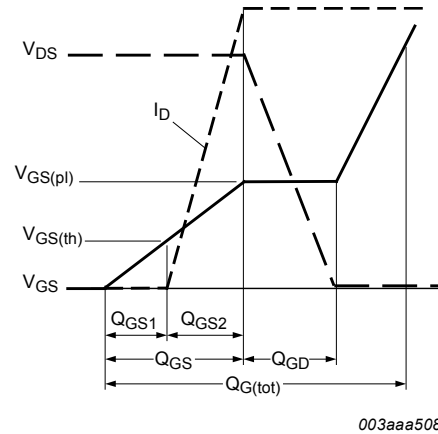
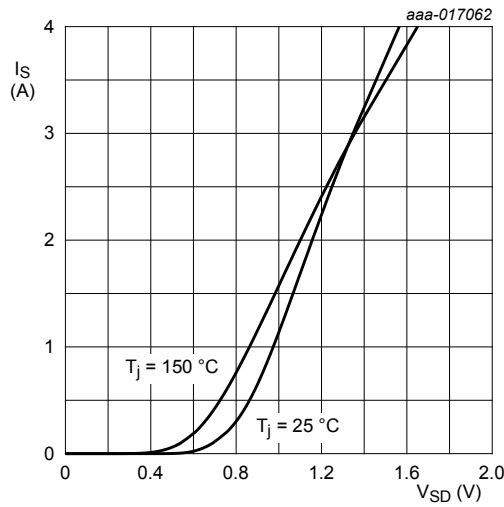


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

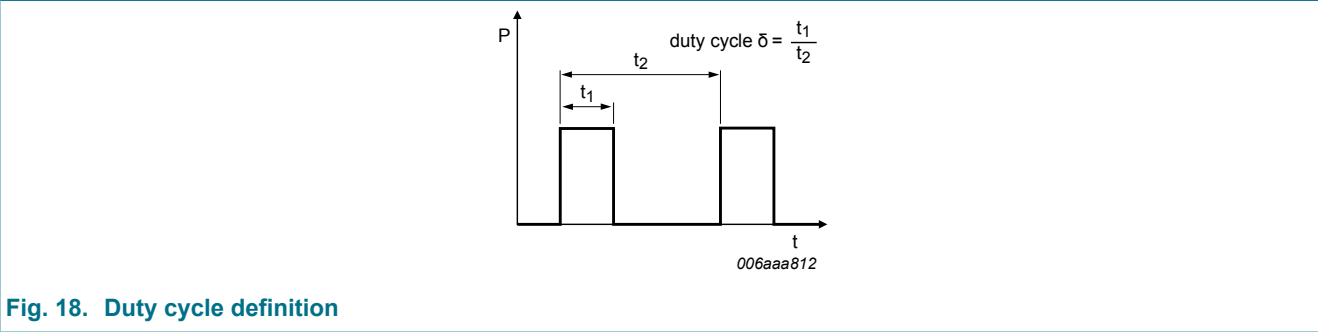
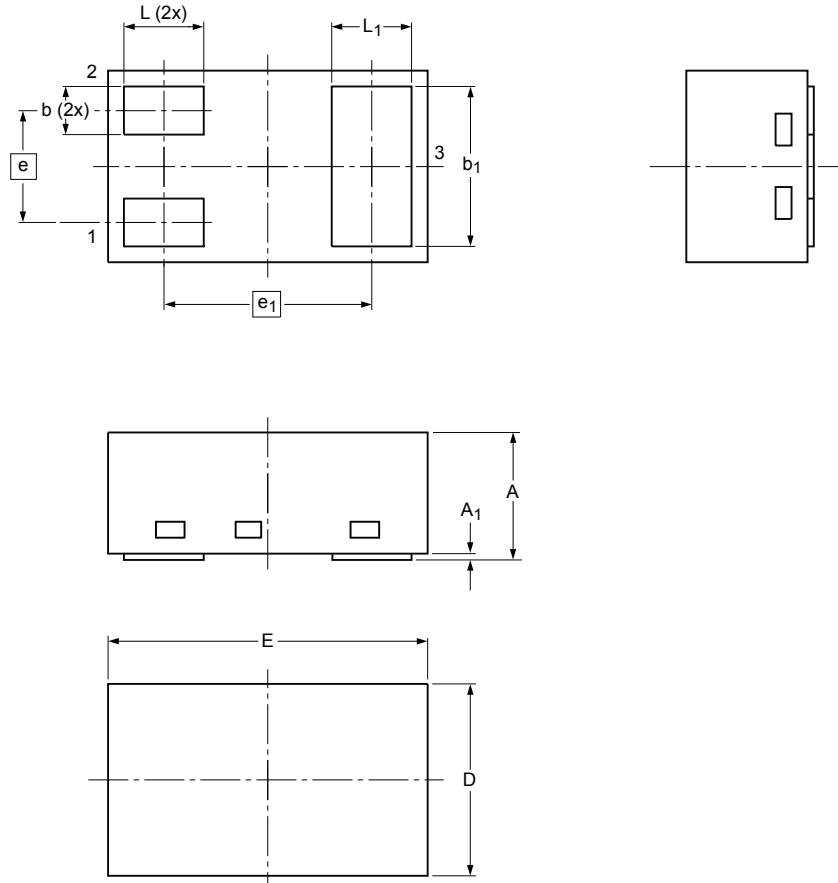


Fig. 18. Duty cycle definition

## 12. Package outline

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm

SOT883B



Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	b <sub>1</sub>	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	max 0.40	0.04	0.20	0.55	0.65	1.05			0.30	0.30
	nom 0.37		0.15	0.50	0.60	1.00	0.35	0.65	0.25	0.25
	min 0.34		0.12	0.47	0.55	0.95			0.22	0.22

Note

1. Including plating thickness

sot883b\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT883B						-11-11-02- 12-01-03

Fig. 19. Package outline DFN1006B-3 (SOT883B)

### 13. Soldering

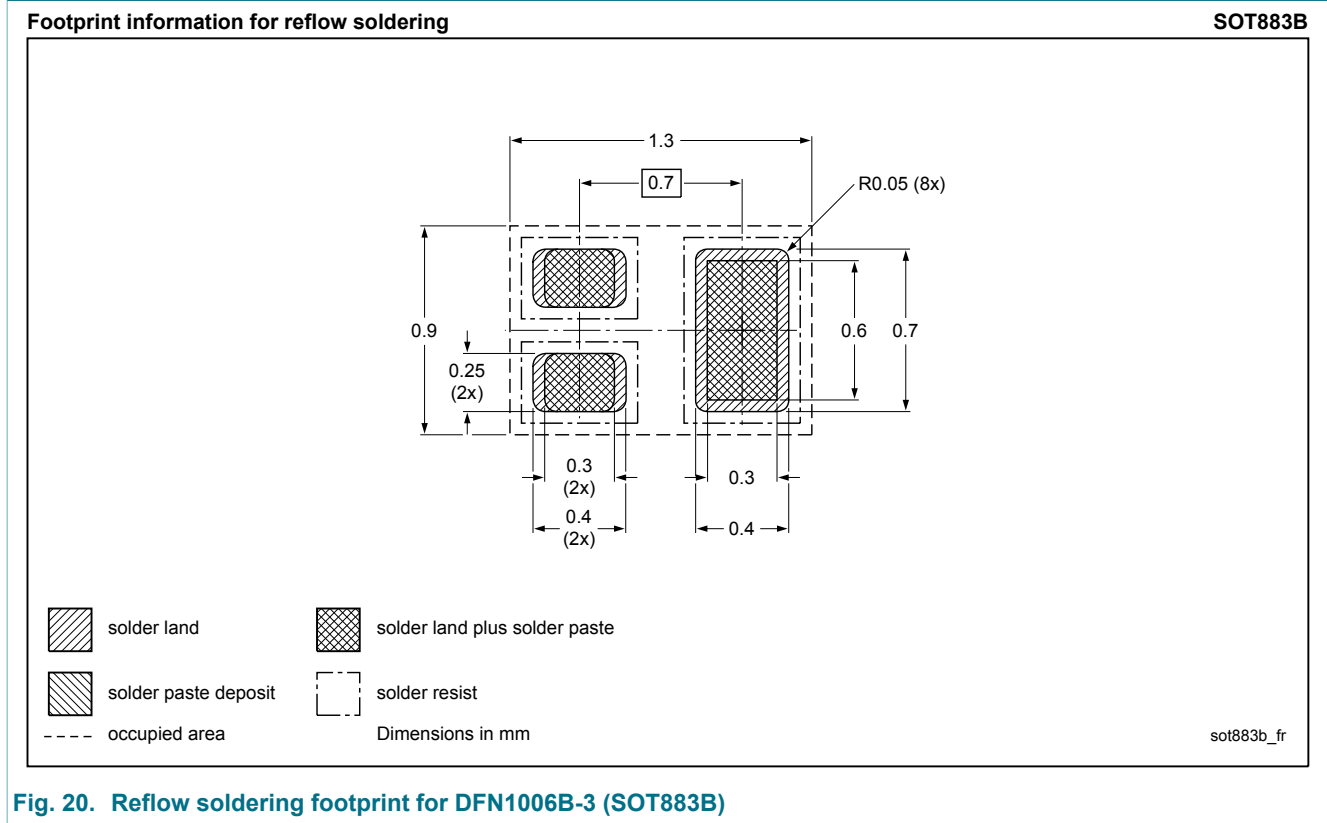


Fig. 20. Reflow soldering footprint for DFN1006B-3 (SOT883B)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZB290UNE2 v.1	20150324	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 16. Contents

1	General description .....	1
2	Features and benefits .....	1
3	Applications .....	1
4	Quick reference data .....	1
5	Pinning information .....	2
6	Ordering information .....	2
7	Marking .....	2
8	Limiting values .....	3
9	Thermal characteristics .....	4
10	Characteristics .....	6
11	Test information .....	10
12	Package outline .....	11
13	Soldering .....	12
14	Revision history .....	13
15	Legal information .....	14
15.1	Data sheet status .....	14
15.2	Definitions .....	14
15.3	Disclaimers .....	14
15.4	Trademarks .....	15

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Date of release: 24 March 2015

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