



**THE DATASHEET OF
MAX3238IDBRQ1**

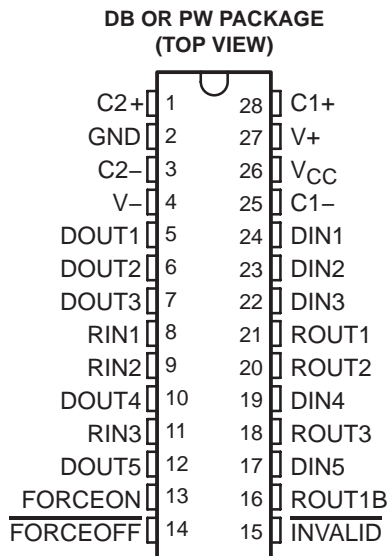


MAX3238-Q1

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ± 15 -kV ESD (HBM) PROTECTION

SLLS569B – MAY 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Meets or Exceeds Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 250 kbit/s
- Five Drivers and Three Receivers
- Low Standby Current . . . 1 μ A Typical
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Always-Active Noninverting Receiver Output (ROUT1B)
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)



description/ordering information

The MAX3238 consists of five line drivers, three line receivers, and a dual charge-pump circuit with ± 15 -kV ESD (HBM) protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between notebook and subnotebook computer applications. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT1B), which allows applications using the ring indicator to transmit data while the device is powered down. These devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

ORDERING INFORMATION[†]

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP (DB)	Tape and reel	MAX3238IDBRQ1	MAX3238Q
	TSSOP (PW)	Tape and reel	MAX3238IPWRQ1	MB3238Q

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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MAX3238-Q1
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description/ordering information (continued)

Flexible control options for power management are featured when the serial port and driver inputs are inactive. The auto-powerdown plus feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense valid signal transitions on all receiver and driver inputs for approximately 30 s, the built-in charge pump and drivers are powered down, reducing the supply current to 1 µA. By disconnecting the serial port or placing the peripheral drivers off, auto-powerdown plus occurs if there is no activity in the logic levels for the driver inputs. Auto-powerdown plus can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown plus enabled, the device automatically activates once a valid signal is applied to any receiver or driver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 µs. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 µs. Refer to Figure 5 for receiver input levels.

Function Tables

EACH DRIVER

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 s	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 s	L	
L	L	H	>30 s	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 s	Z	

H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS				OUTPUTS		RECEIVER STATUS
RIN1	RIN2-RIN3	FORCEOFF	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1B	ROUT	
L	X	L	X	L	Z	Powered off while ROUT1B is active
H	X	L	X	H	Z	
L	L	H	<30 s	L	H	Normal operation with auto-powerdown plus disabled/enabled
L	H	H	<30 s	L	L	
H	L	H	<30 s	H	H	
H	H	H	<30 s	H	L	
Open	Open	H	>30 s	L	H	

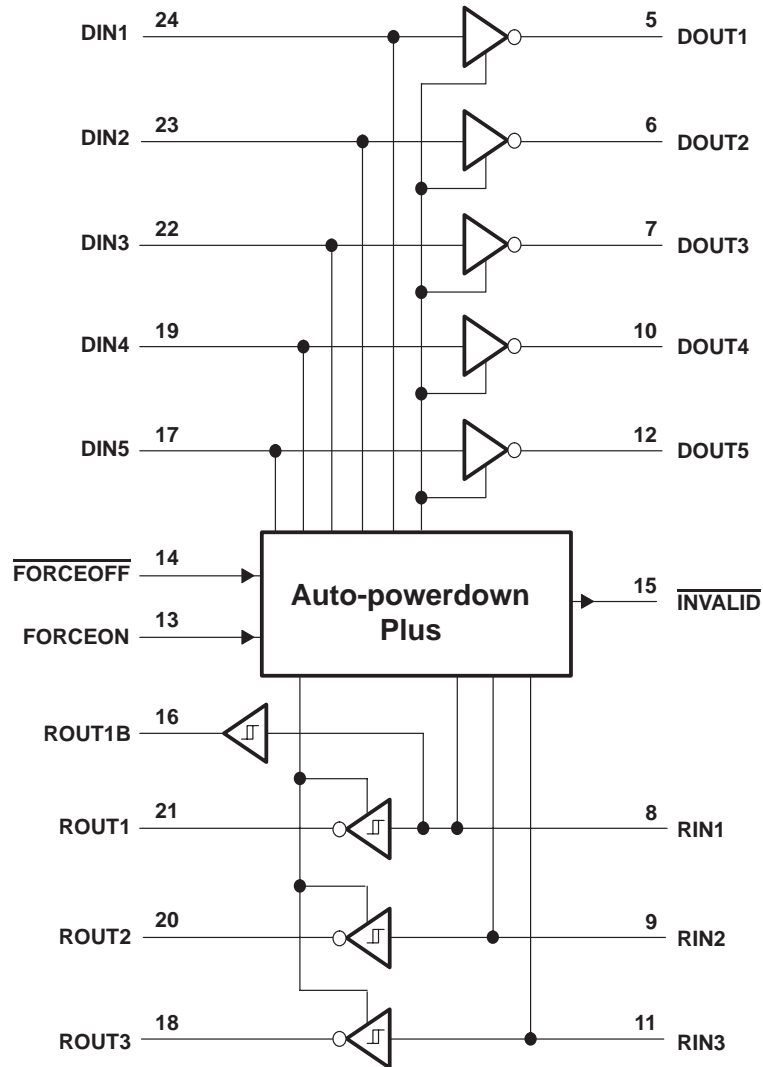
H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off



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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, V_I : Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, V_O : Driver	–13.2 V to 13.2 V
Receiver (INVALID)	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	62°C/W
PW package	62°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

			MIN	NOM	MAX	UNIT	
Supply voltage		$V_{CC} = 3.3$ V	3	3.3	3.6	V	
		$V_{CC} = 5$ V	4.5	5	5.5		
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	$V_{CC} = 3.3$ V		2	V	
			$V_{CC} = 5$ V		2.4		
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON			0.8	V	
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	0			5.5	V
V_I	Receiver input voltage		–25			25	V
T_A	Operating free-air temperature	MAX3238I	–40			85	°C

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.15 V; C1–C4 = 0.22 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; and C1 = 0.047 μ F and C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT	
I_l	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON		\pm 0.01	\pm 1	μ A	
I_{CC}	Supply current ($T_A = 25^\circ\text{C}$)	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.5	2	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10	μ A

‡ All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.15 V; C1–C4 = 0.22 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; and C1 = 0.047 μ F and C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH} High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL} Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	-5	-5.4		V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS} Short-circuit output current‡	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
	V _{CC} = 5.5 V, V _O = 0 V		±40	±100	
r _o Output resistance	V _{CC} , V ₊ , and V ₋ = 0 V, V _O = ±2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND, V _O = ±12 V, V _{CC} = 0 to 5.5 V			±25	μA

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Maximum data rate	C _L = 1000 pF, One DOUT switching, R _L = 3 kΩ, See Figure 1	150	250		kbit/s
t _{sk(p)} Pulse skew§	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2		100		ns
SR(tr) Slew rate, transition region (see Figure 1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 pF to 1000 pF	6	30	V/μs
		C _L = 150 pF to 2500 pF	4	30	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6 V	V _{CC} - 0.1 V		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
I _{off}	Output leakage current (except ROUT1B)	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3		150		ns
t _{PHL}	Propagation delay time, high- to low-level output			150		
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4		200		ns
t _{dis}	Output disable time			200		
t _{sk(p)}	Pulse skew‡	See Figure 3		50		ns

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.



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AUTO-POWERDOWN PLUS SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{T+} (valid)	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}			2.7	V
V _{T-} (valid)	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-2.7			V
V _T (invalid)	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-0.3		0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} - 0.6			V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _{CC}			0.4	V

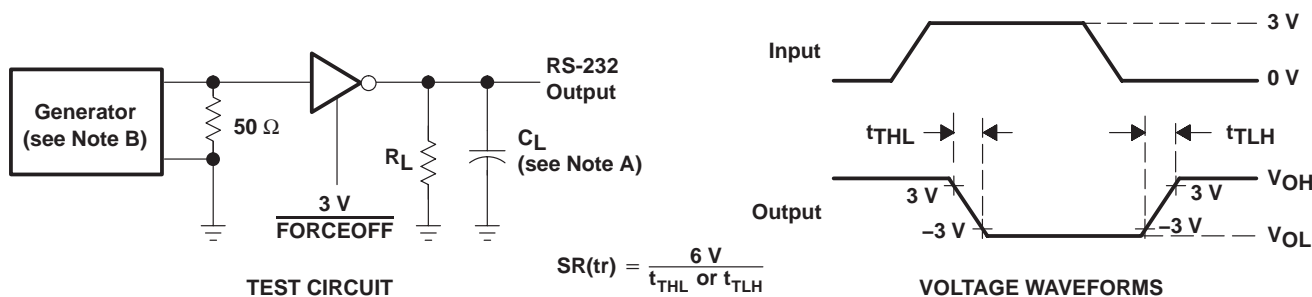
† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		MIN	TYP†	MAX	UNIT
t _{valid}	Propagation delay time, low- to high-level output		0.1		μs
t _{invalid}	Propagation delay time, high- to low-level output		50		μs
t _{en}	Supply enable time		25		μs
t _{dis}	Receiver or driver edge to auto-powerdown plus	15	30	60	s

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



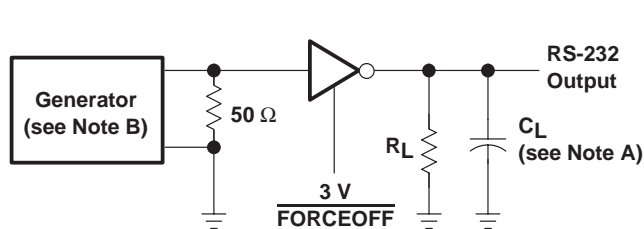
- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 1. Driver Slew Rate

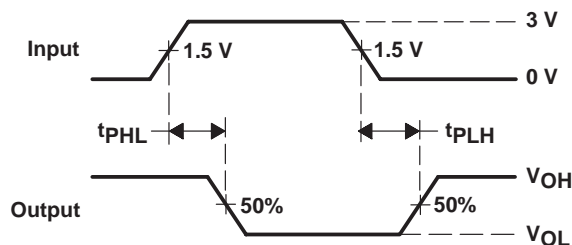
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PARAMETER MEASUREMENT INFORMATION



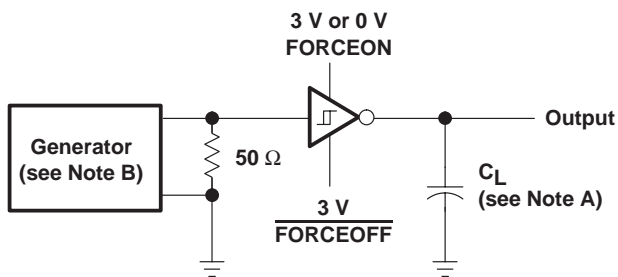
TEST CIRCUIT



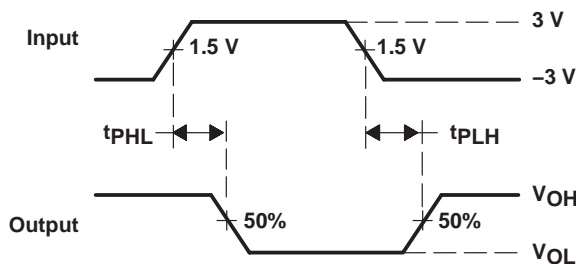
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 2. Driver Pulse Skew



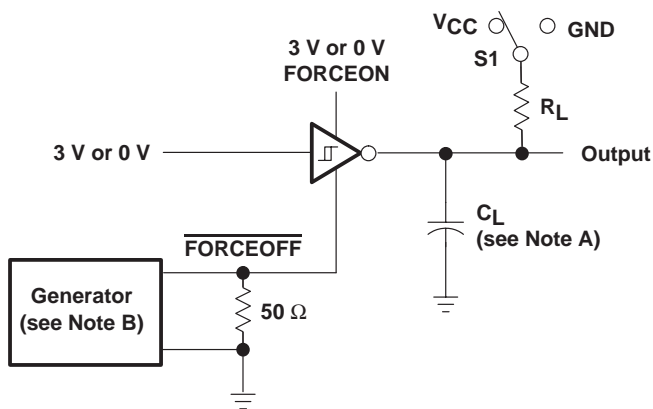
TEST CIRCUIT



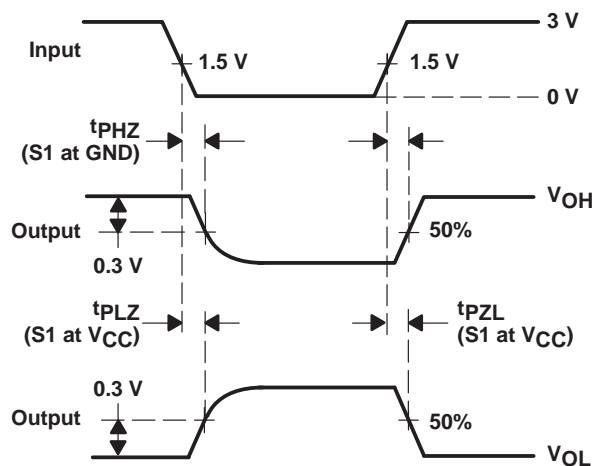
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Receiver Propagation Delay Times



TEST CIRCUIT



VOLTAGE WAVEFORMS

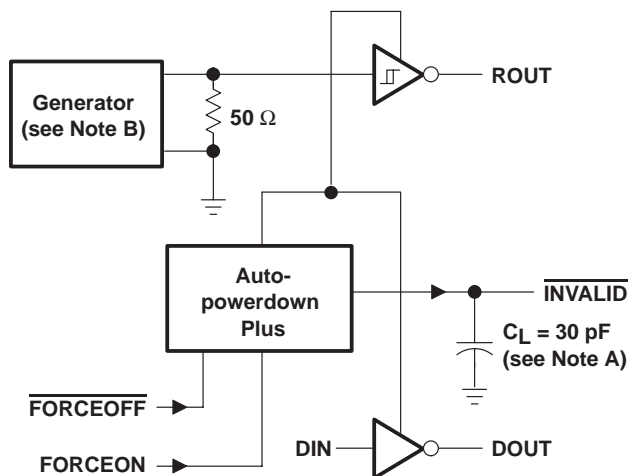
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
 C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 4. Receiver Enable and Disable Times

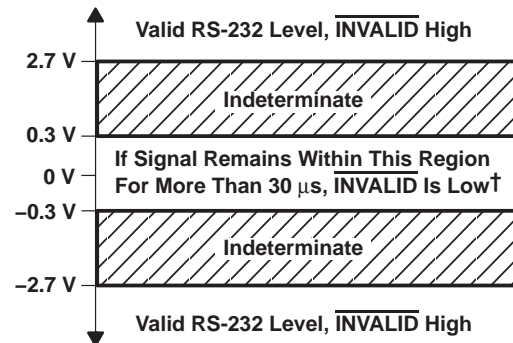
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



† Auto-powerdown plus disables drivers and reduces supply current to 1 μ A.

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

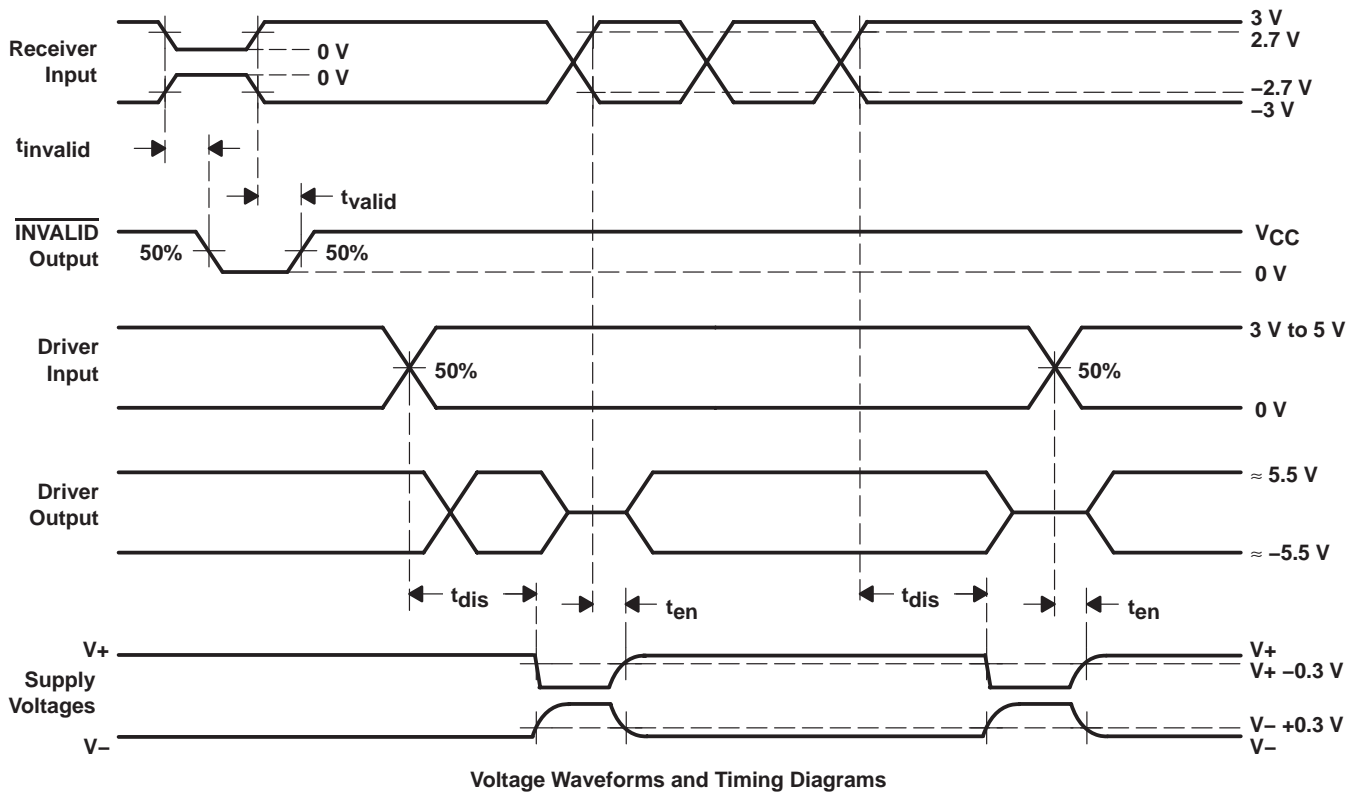
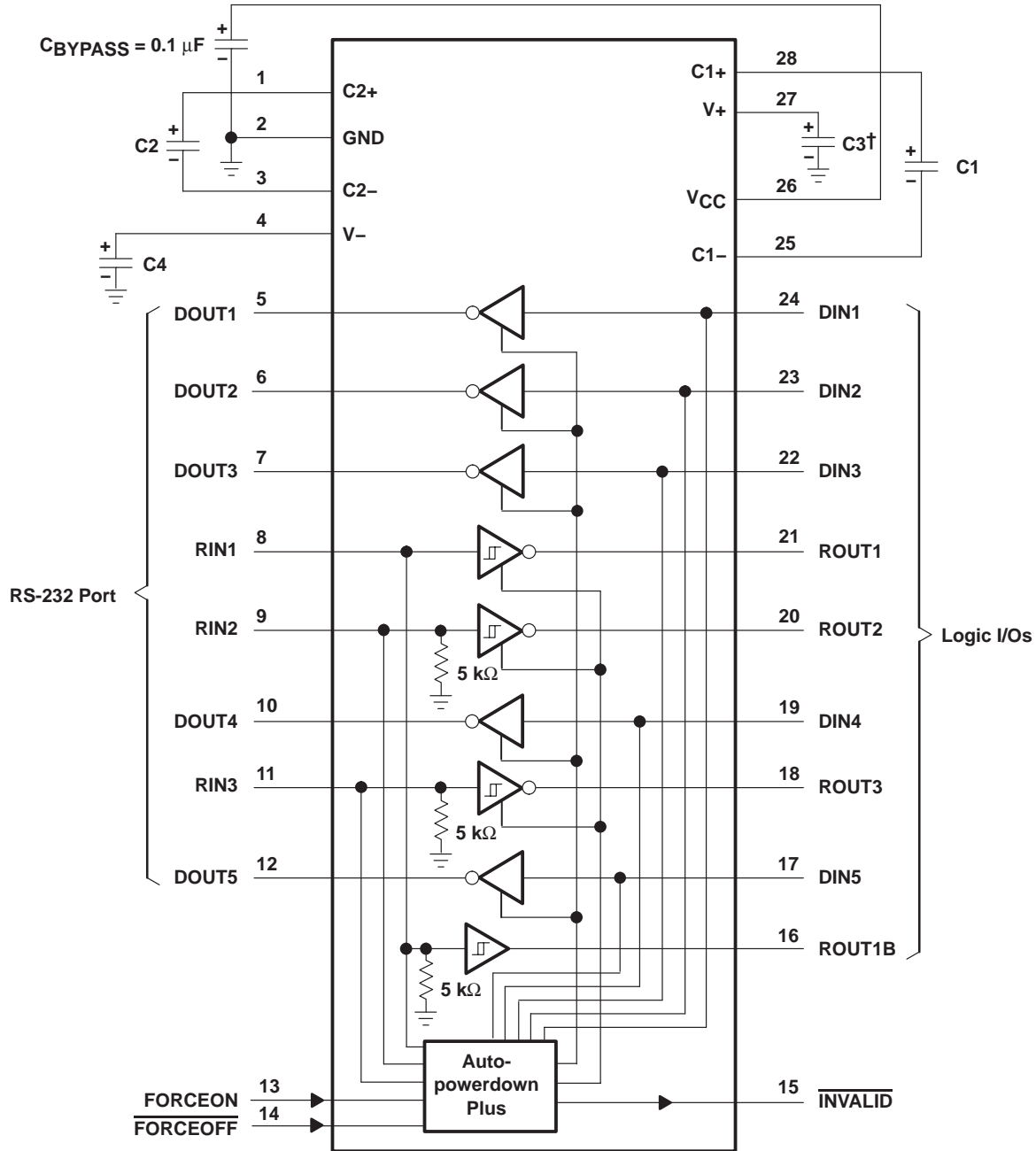


Figure 5. $\overline{\text{INVALID}}$ Propagation-Delay Times and Supply-Enabling Time

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APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.15 V	0.1 μF	0.1 μF
3.3 V ± 0.3 V	0.22 μF	0.22 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.22 μF	1 μF

Figure 6. Typical Operating Circuit and Capacitor Values



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3238IDBG4Q1	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3238Q	Samples
MAX3238IDBRG4Q1	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3238Q	Samples
MAX3238IPWG4Q1	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3238Q	Samples
MAX3238IPWQ1	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3238Q	Samples
MAX3238IPWRG4Q1	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3238Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF MAX3238-Q1 :

- Catalog: [MAX3238](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3238IDBRG4Q1	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3238IDBRG4Q1	SSOP	DB	28	2000	367.0	367.0	38.0

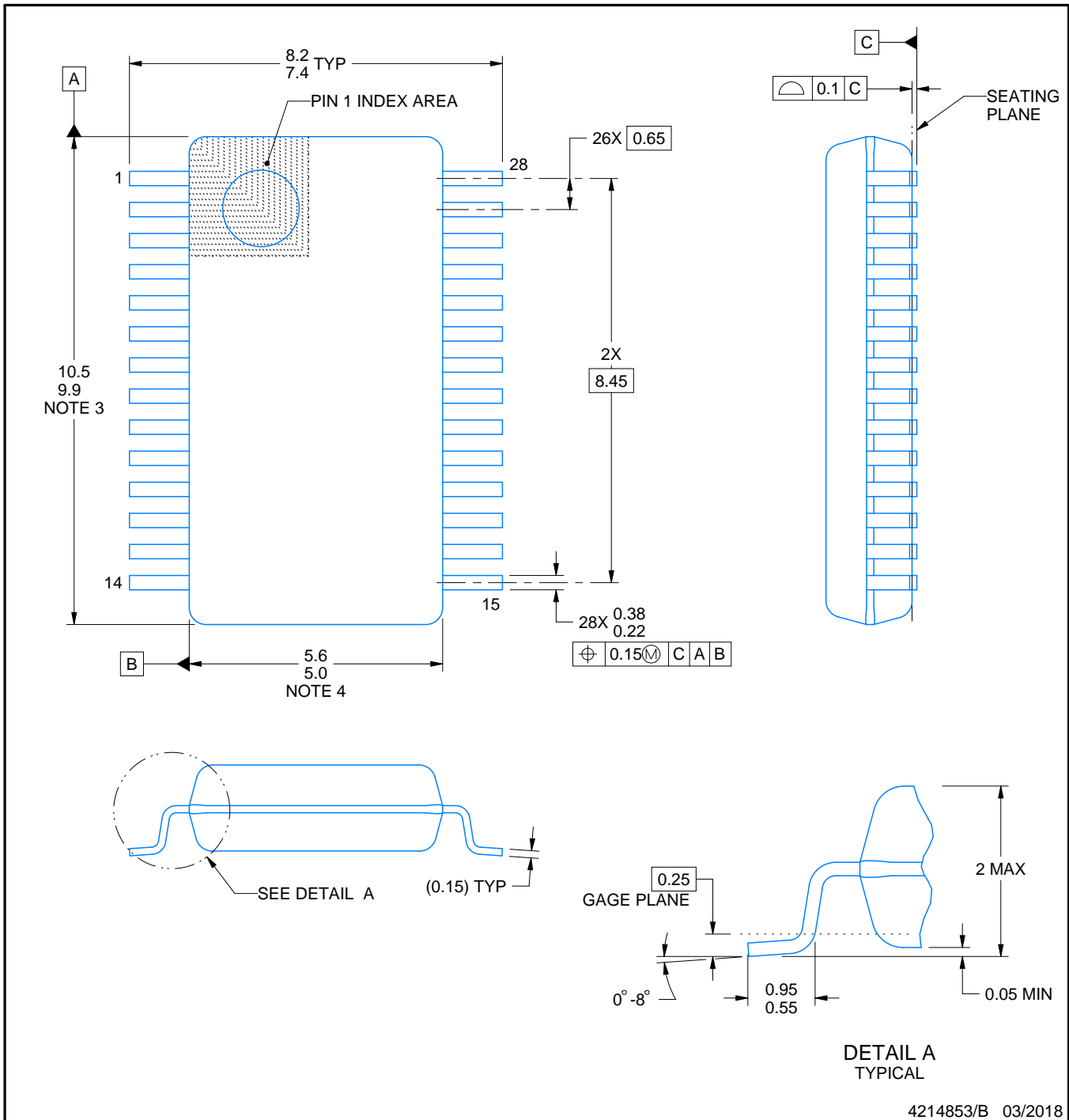
DB0028A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES:

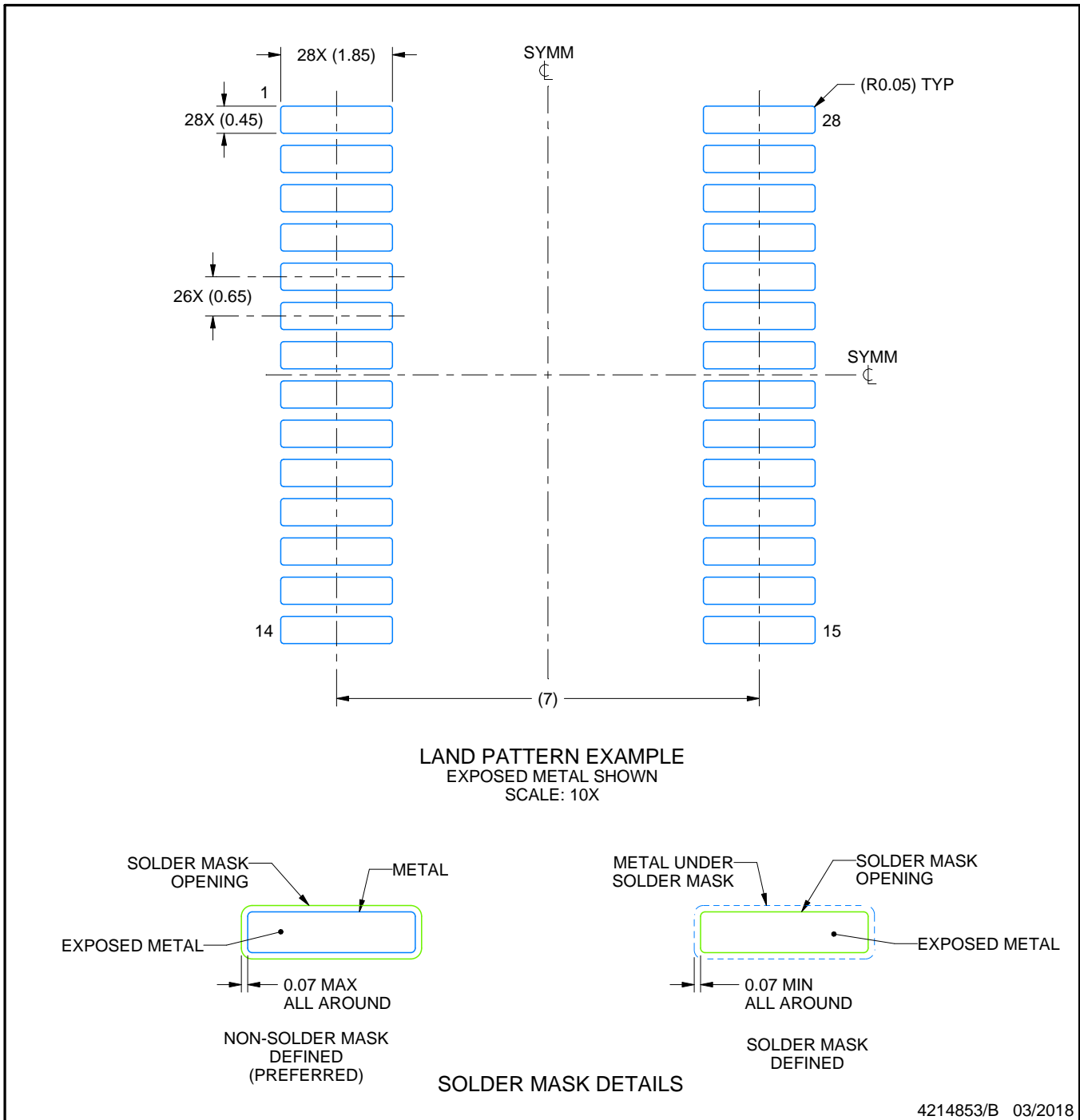
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

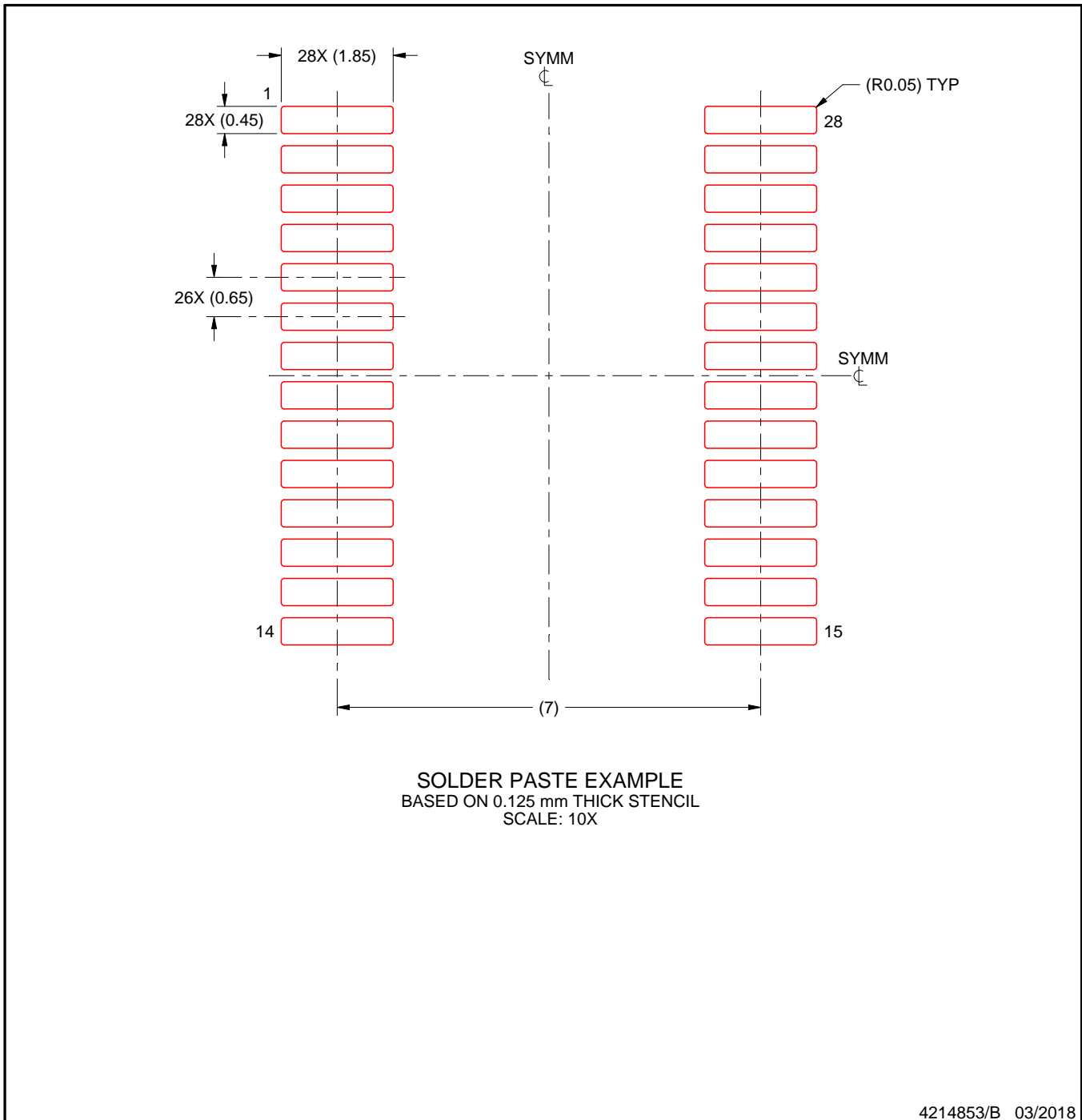
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

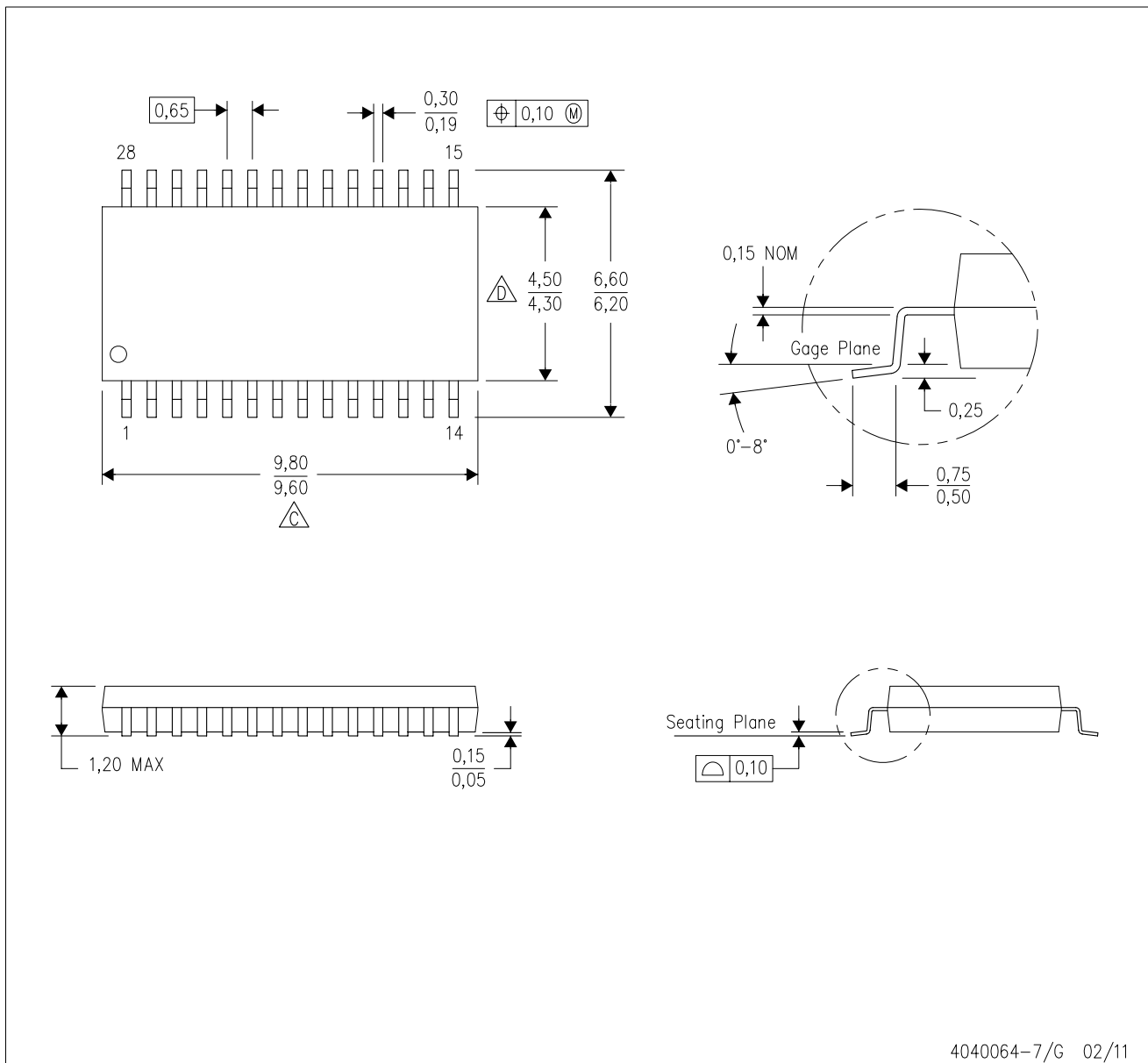


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

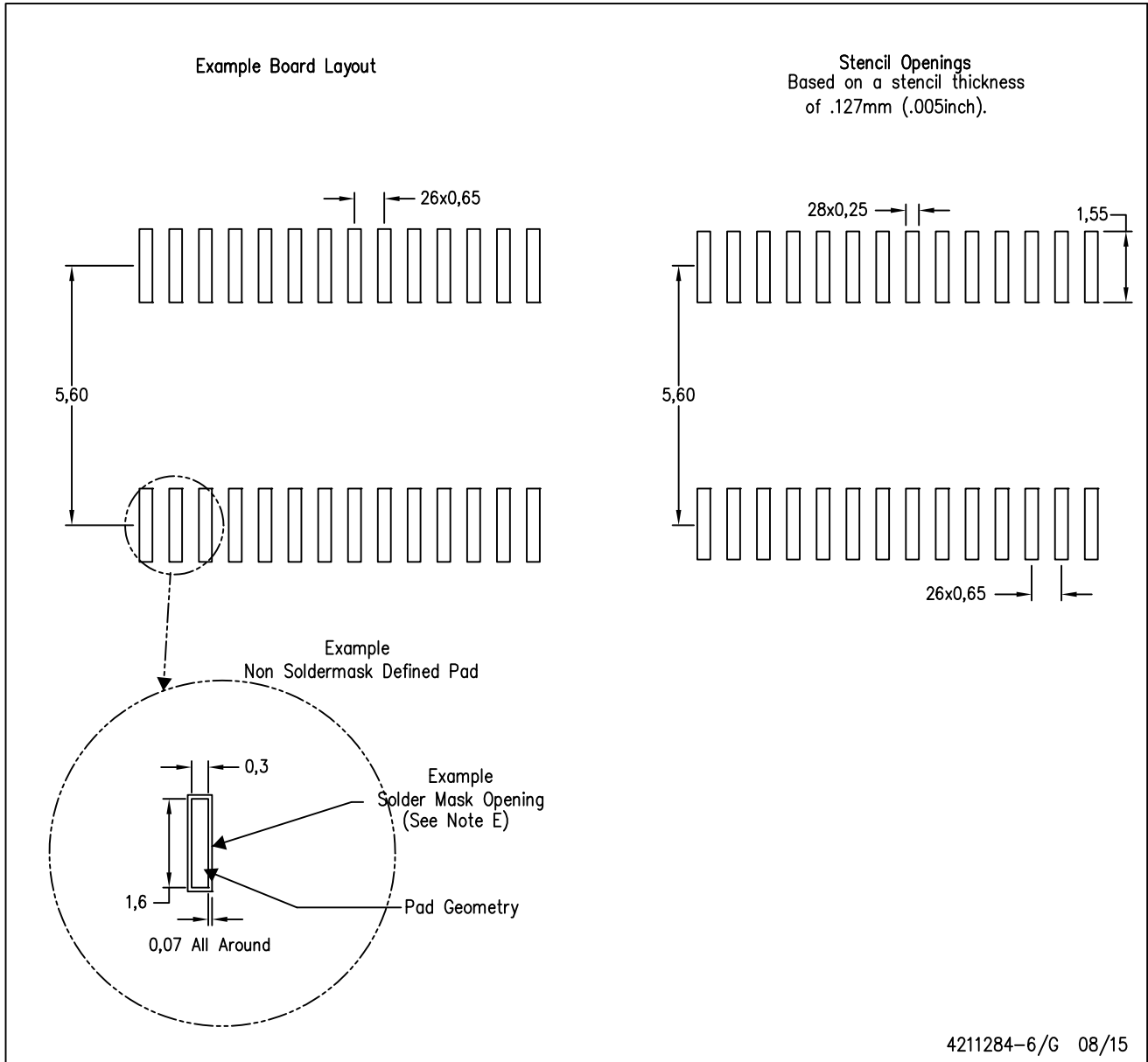


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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