THE DATASHEET OF

TRS222CN

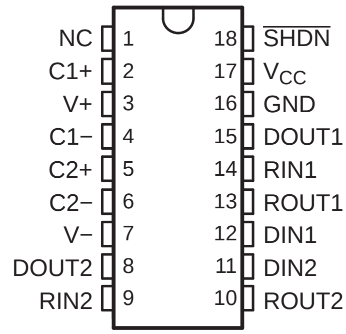
TRS222
5-V DUAL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

SLLS813 – JULY 2007

FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Operates up to 200 kbit/s**
- **Low Supply Current in Shutdown Mode . . . 2 µA Typical**
- **External Capacitors . . . 4 × 0.1 µF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DW OR N PACKAGE (TOP VIEW)



APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION/ORDERING INFORMATION

The TRS222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/µs driver output slew rate. By using shutdown ($\overline{SHDN}$), all receivers can be disabled.

ORDERING INFORMATION

T_A	PACKAGE (1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	TRS222CN	TRS222CN
	SOIC – DW	Tube of 20	TRS222CDW	TRS222C
		Reel of 1000	TRS222CDWR	
–40°C to 85°C	PDIP – N	Tube of 20	TRS222IN	TRS222IN
	SOIC – DW	Tube of 20	TRS222IDW	TRS222I
		Reel of 1000	TRS222IDWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION TABLES

Each Driver[(1)]

INPUT DIN	OUTPUT DOUT
L	H
H	L

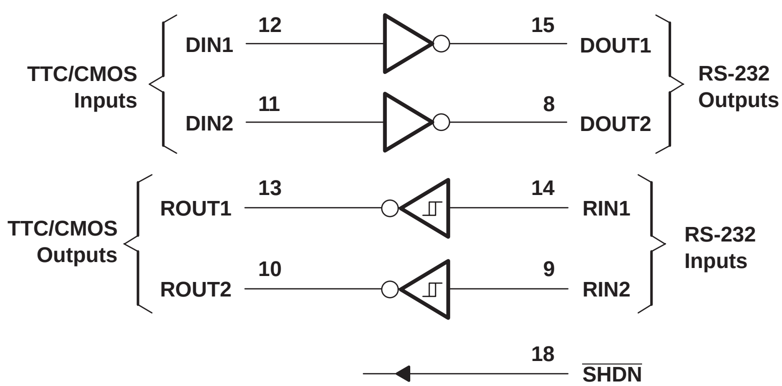
(1) H = high level, L = low level

Each Receiver[(1)]

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V_I	Input voltage range	Drivers	–0.3	V_{CC} – 0.3	V
		Receivers		±30	
V_O	Output voltage range	Drivers		±15	V
		Receivers	–0.3	V_{CC} + 0.3	
D_{OUT}	Short-circuit duration			Continuous	
θ_{JA}	Package thermal impedance(3)(4)	DW package		58	°C/W
		N package		TBD	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

See Figure 4

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
	Shutdown high-level input voltage	$\overline{SHDN}$	2			
V_{IL}	Driver and control low-level input voltage	DIN			0.8	V
	Shutdown low-level input voltage	$\overline{SHDN}$			0.8	
V_I	Driver input voltage	DIN	0		5.5	V
	Receiver input voltage		–30		30	
T_A	Operating free-air temperature	TRS222C	0		70	°C
		TRS222I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5 V,	$\overline{SHDN}$ = V_{CC}	No load		4	10	mA
				3 kΩ on both inputs		15		
	Shutdown supply current					2	50	µA
$\overline{SHDN}$	Shutdown input leakage current						±1	µA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	8		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–8		V
I_{IH}	Driver high-level input current	DIN = V_{CC}			5	40	μA
	Control high-level input current	$\overline{SHDN}$ = V_{CC}			0.01	1	
I_{IL}	Driver low-level input current	DIN = 0 V			–5	–40	μA
	Control low-level input current	$\overline{SHDN}$ = 0 V			–0.01	–1	
I_{OS}	Short-circuit output current[3]	V_{CC} = 5.5 V,	V_O = 0 V	±7	±22		mA
I_{off}	Output leakage current	V_{CC} = 5.5 V, $\overline{SHDN}$ = GND,	V_O = ±10 V		±0.01	±10	μA
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10 M		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
	Data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See Figure 1	200			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	See Figure 1			1.5	3.5	μs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	See Figure 1			1.3	3.5	μs
$t_{PHL(D)}$ – $t_{PLH(D)}$	Driver (+ to –) propagation delay difference				300		ns
$t_{sk(p)}$	Pulse skew[3]	C_L = 150 pF to 2500 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	C_L = 50 pF to 2500 pF, V_{CC} = 5 V	R_L = 3 kΩ to 7 kΩ,	6	12	30	V/μs
t_{ET}	Driver output enable time (after $\overline{SHDN}$ goes high)				250		μs
t_{DT}	Driver output disable time (after $\overline{SHDN}$ goes low)				300		ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

RECEIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	3.5	V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	I_{OH} = 3.2 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5 V	0.8	1.3		V
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

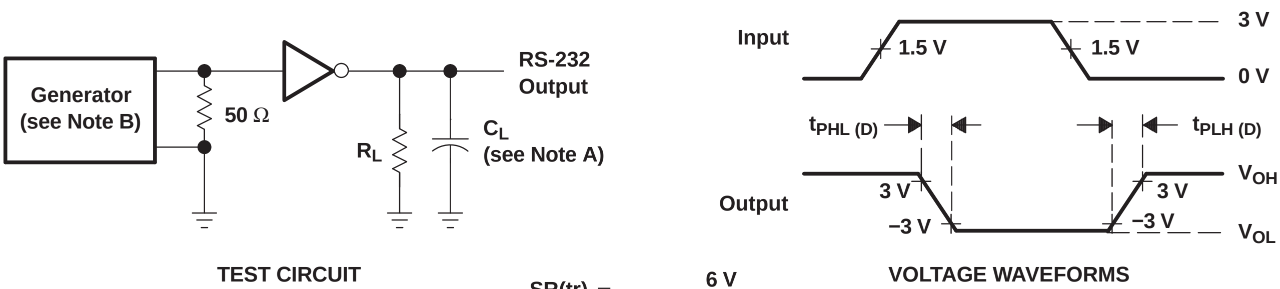
PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150 pF		0.6	1	µs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150 pF		0.5	1	µs
$t_{PHL(R)}$– $t_{PLH(R)}$	Receiver (+ to –) propagation delay difference			100		ns
$t_{sk(p)}$	Pulse skew(3)			100		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

ESD Protection

PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	Human-Body Model	±15	kV

PARAMETER MEASUREMENT INFORMATION

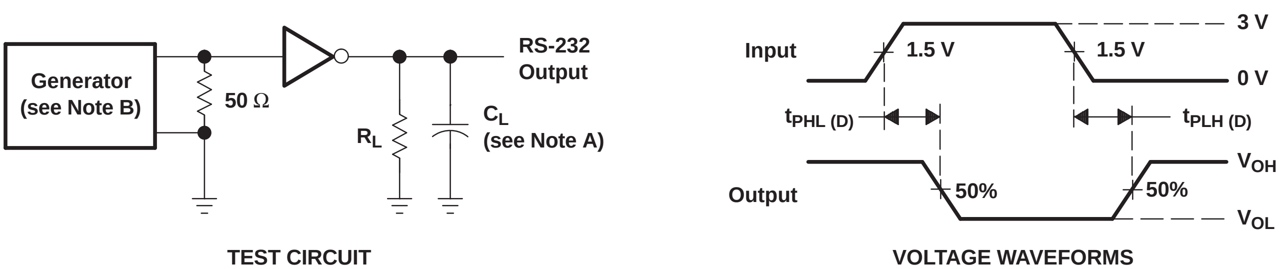


$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)}\ \text{or}\ t_{PLH\ (D)}}$$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

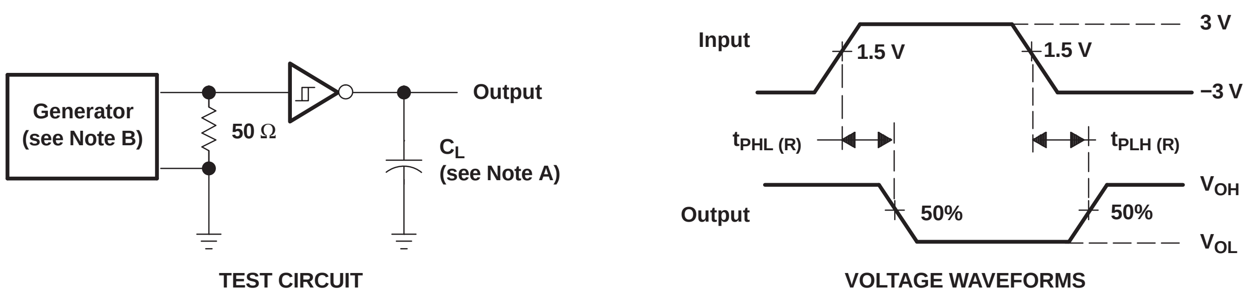
Figure 1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 2. Driver Pulse Skew

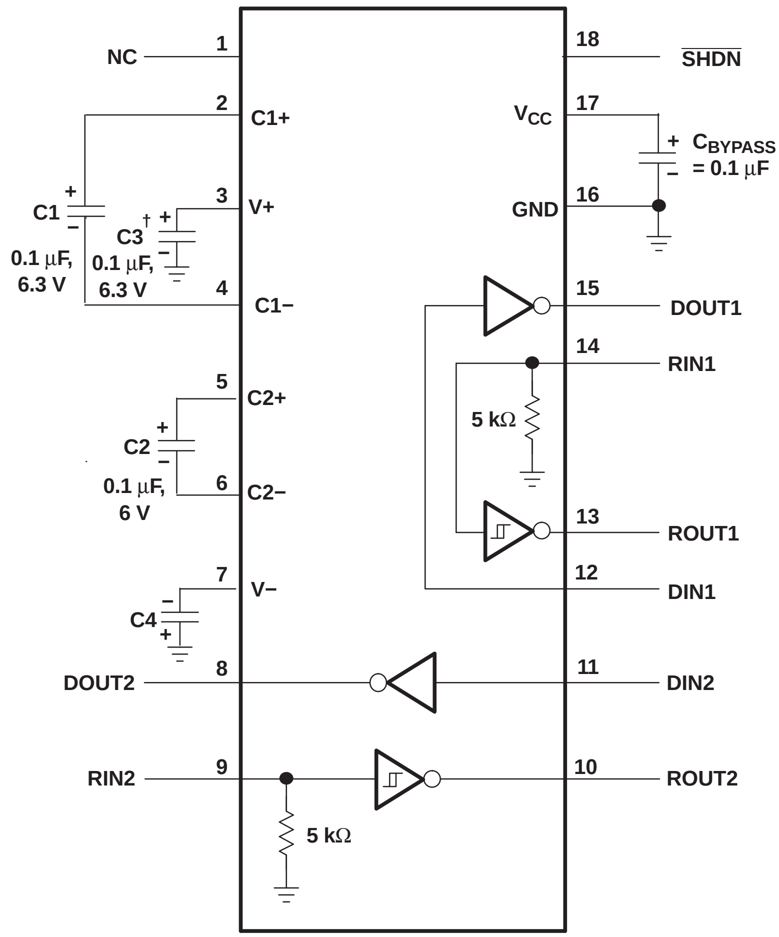


A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION (continued)

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The TRS222 requires 0.1-μF capacitors, although capacitors up to 10 μF can be used without harm. Ceramic dielectrics are suggested for the 0.1-μF capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 μF) to reduce the output impedance at V+ and V–.

Bypass V_{CC} to ground with at least 0.1 μF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

Electrostatic Discharge (ESD) Protection

TI TRS222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15 kV when powered down.

ESD Test Conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-kΩ resistor.

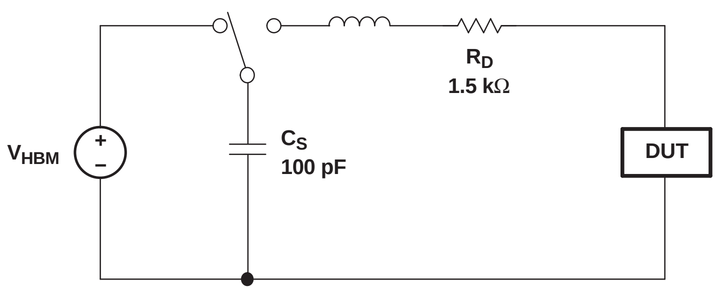


Figure 5. HBM ESD Test Circuit

APPLICATION INFORMATION (continued)

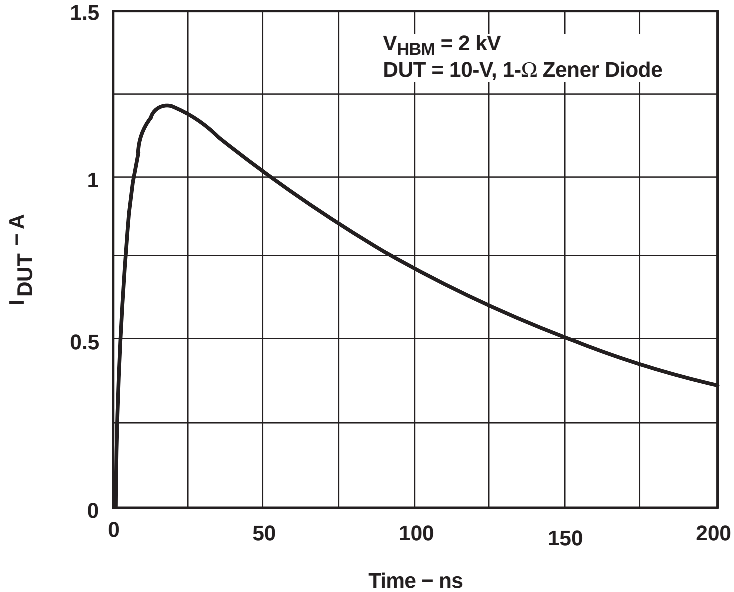


Figure 6. Typical HBM Current Waveform

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TRS222CDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CN	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS222CNE4	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS222IDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IN	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS222INE4	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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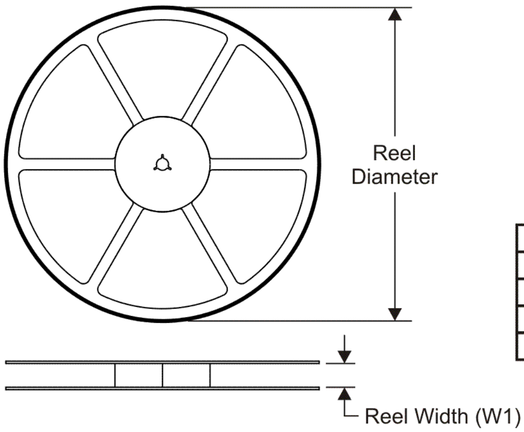
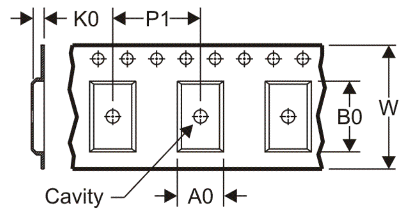
TAPE AND REEL INFORMATION

REEL DIMENSIONS

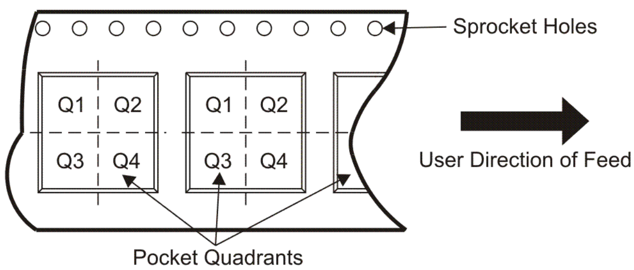


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

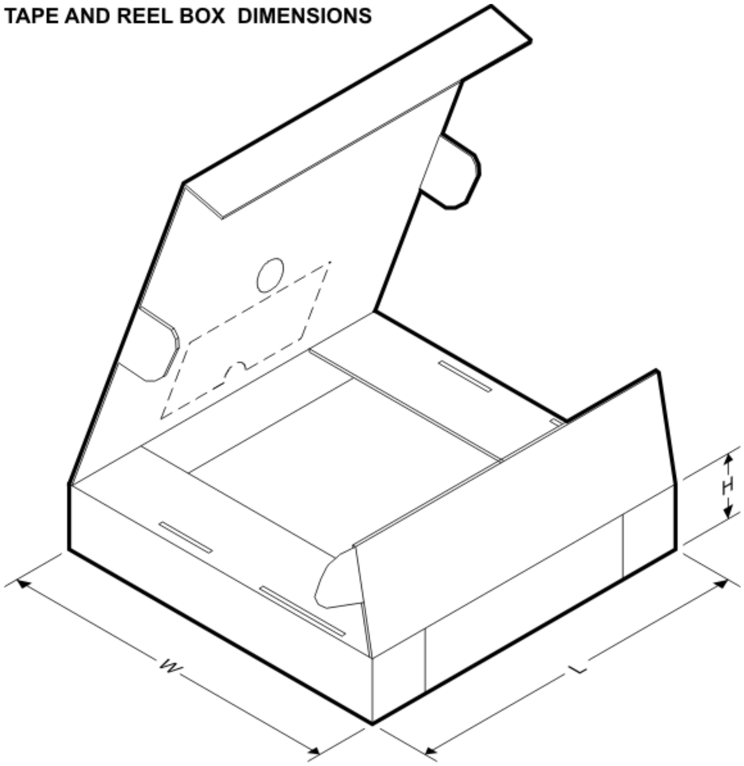
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS222CDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
TRS222IDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

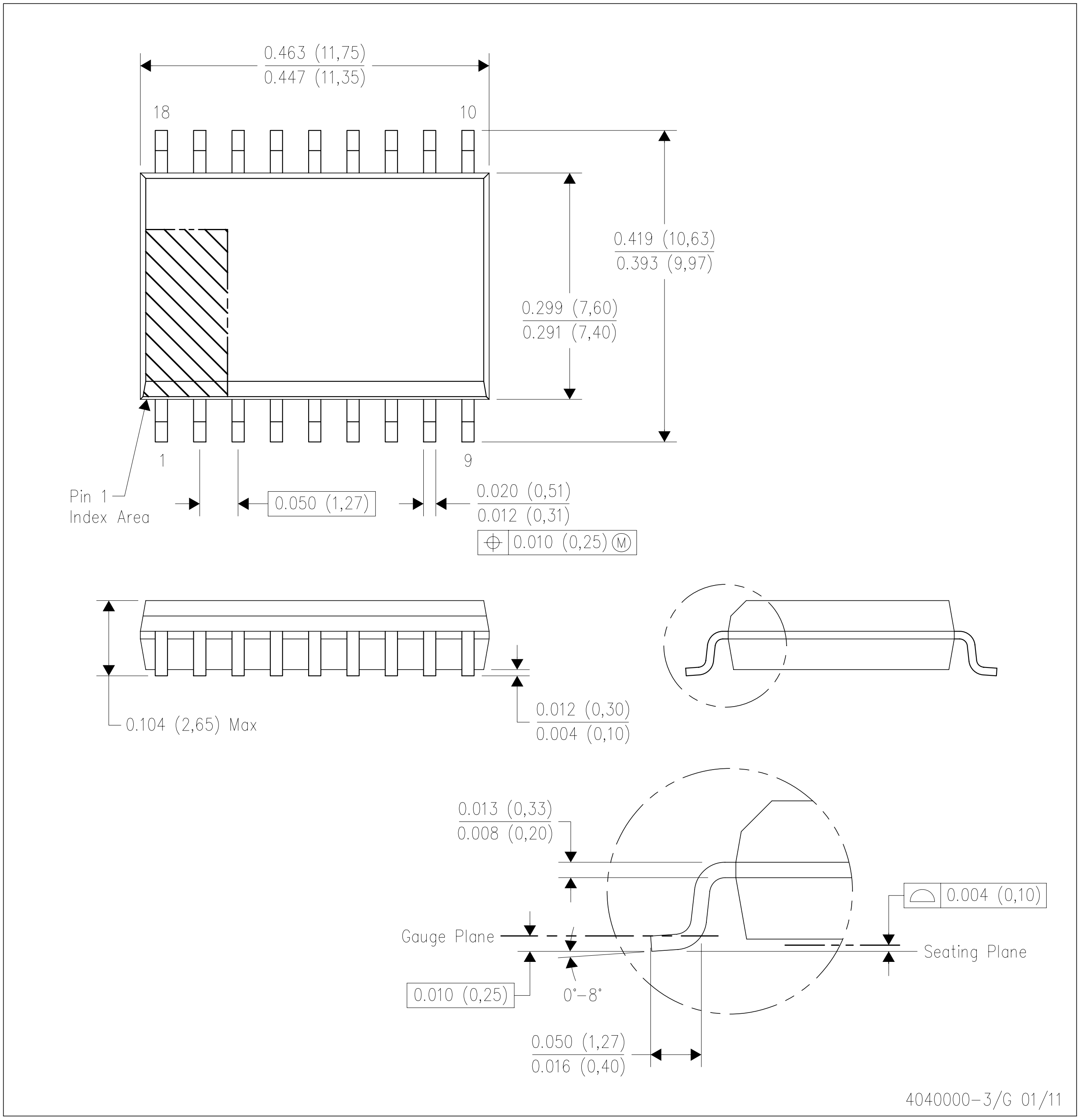
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

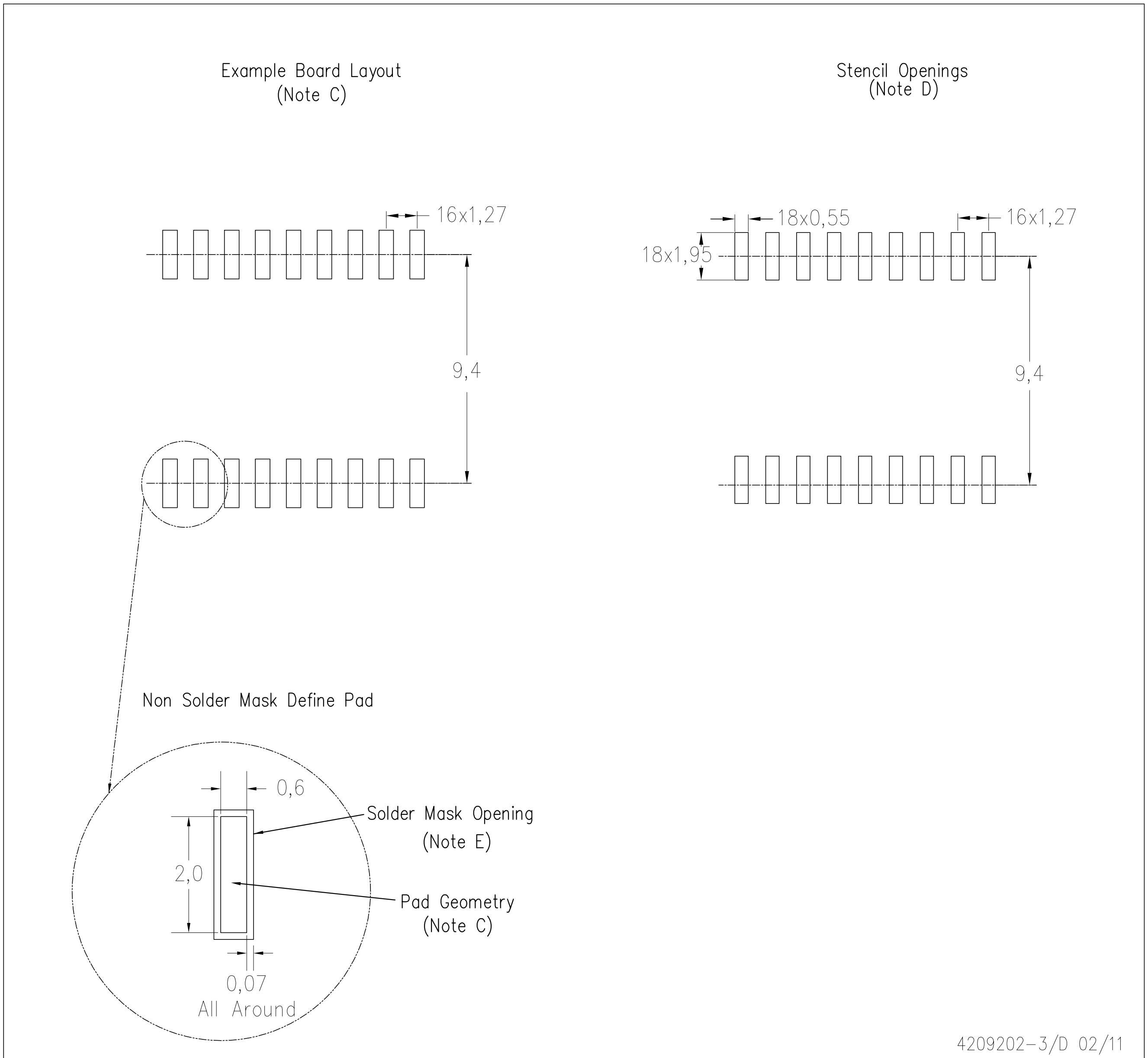
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS222CDWR	SOIC	DW	18	2000	370.0	355.0	55.0
TRS222IDWR	SOIC	DW	18	2000	370.0	355.0	55.0

DW (R-PDSO-G18) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AB.

DW (R-PDSO-G18) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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