



**THE DATASHEET OF  
CSD16325Q5**



# N-Channel NexFET Power MOSFETs

## 1 Features

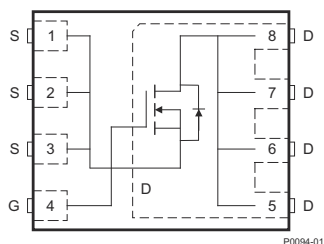
- Optimized for 5 V Gate Drive
- Ultralow  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

## 2 Applications

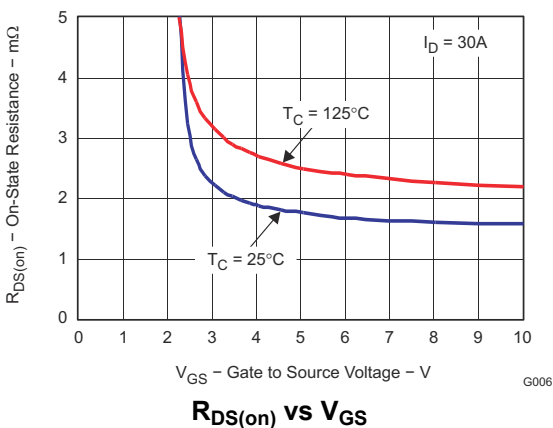
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

## 3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5 V gate drive applications.



Top View



## Product Summary

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5 V)	18	nC
$Q_{gd}$	Gate Charge Gate to Drain	3.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3\text{ V}$	2.1 mΩ
		$V_{GS} = 4.5\text{ V}$	1.7 mΩ
		$V_{GS} = 8\text{ V}$	1.5 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

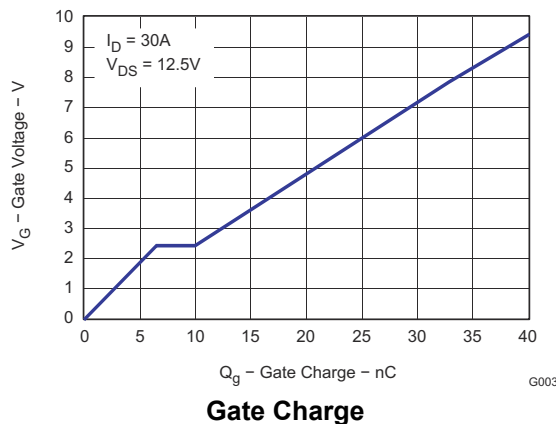
## Ordering Information

Device	Package	Media	Qty	Ship
CSD16325Q5	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current <sup>(1)</sup>	33	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	200	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 100\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	500	mJ

- (1) Typical  $R_{\theta JA} = 38^\circ\text{C/W}$  on 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$



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## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision C (April 2010) to Revision D (October 2023) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... **1**

### Changes from Revision B (April 2010) to Revision C (April 2010) Page

- Changed  $R_{DS(on)}$ ,  $V_{GS} = 3\text{ V}$  in the Electrical Characteristics table From: 2.7 to 2.9 in the max column..... **3**

## 4 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

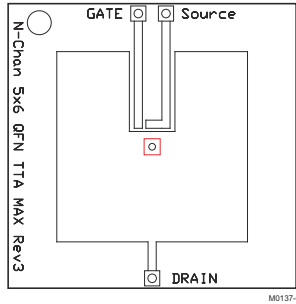
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$V_{DSS}$	Drain to Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = +10/-8\text{ V}$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3\text{ V}, I_D = 30\text{ A}$		2.1	2.9	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		1.7	2.2	m $\Omega$
		$V_{GS} = 8\text{ V}, I_D = 30\text{ A}$		1.5	2	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		159		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 12.5\text{ V},$ $f = 1\text{ MHz}$		3070	4000	pF
$C_{oss}$	Output Capacitance			2190	2850	pF
$C_{riss}$	Reverse Transfer Capacitance			120	150	pF
$R_G$	Series Gate Resistance			1.6	3.2	$\Omega$
$Q_g$	Gate Charge Total (4.5 V)			18	25	nC
$Q_{gd}$	Gate Charge – Gate to Drain	$V_{DS} = 12.5\text{ V},$ $I_{DS} = 30\text{ A}$		3.5		nC
$Q_{gs}$	Gate Charge – Gate to Source			6.6		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			3.3		nC
$Q_{oss}$	Output Charge	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}$		43		nC
$t_{d(on)}$	Turn On Delay Time			10.5		ns
$t_r$	Rise Time	$V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 30\text{ A}, R_G = 2\ \Omega$		16		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
$t_f$	Fall Time			12		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{DS} = 30\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 10\text{ V}, I_F = 30\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		63		nC
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 10\text{ V}, I_F = 30\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		47		ns

## 5 Thermal Characteristics

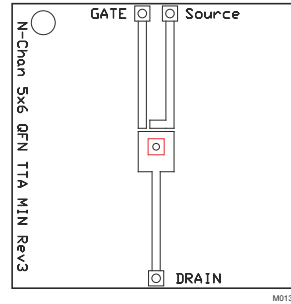
( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1) (2)</sup>			50	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch  $\times$  1.5-inch (3.81-cm  $\times$  3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



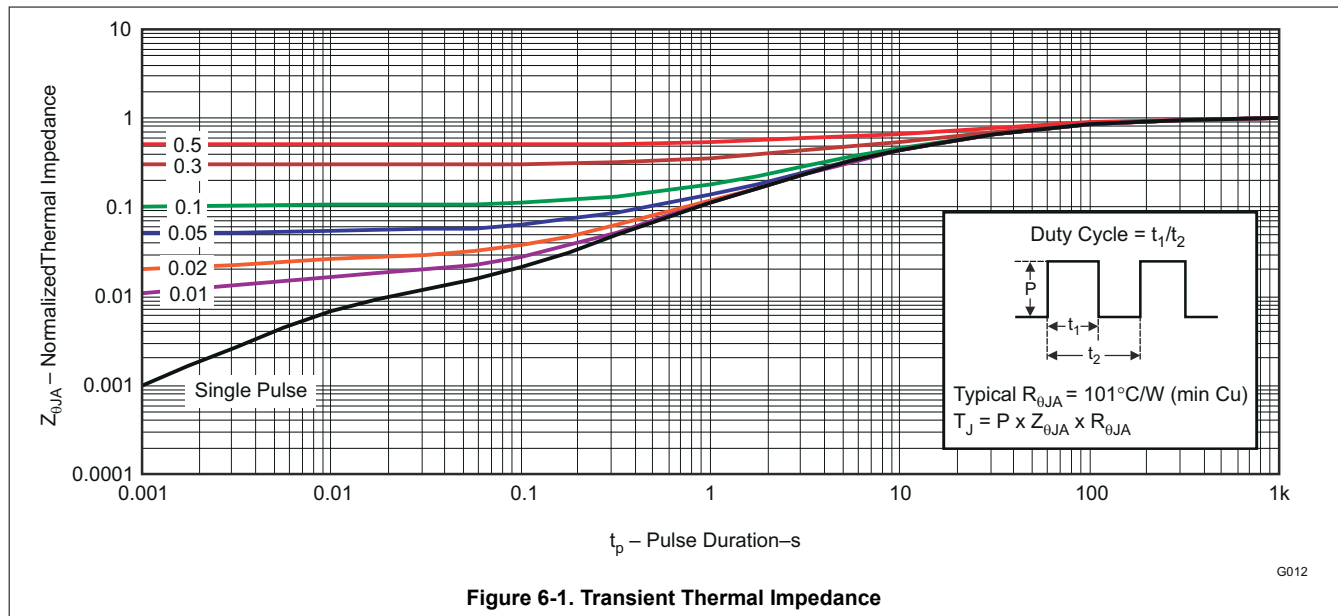
Max  $R_{\theta JA}$  = 50°C/W  
when mounted on 1 inch<sup>2</sup>  
(6.45 cm<sup>2</sup>) of 2-oz. (0.071-  
mm thick) Cu.



Max  $R_{\theta JA}$  = 126°C/W when  
mounted on minimum pad  
area of 2-oz. (0.071-mm  
thick) Cu.

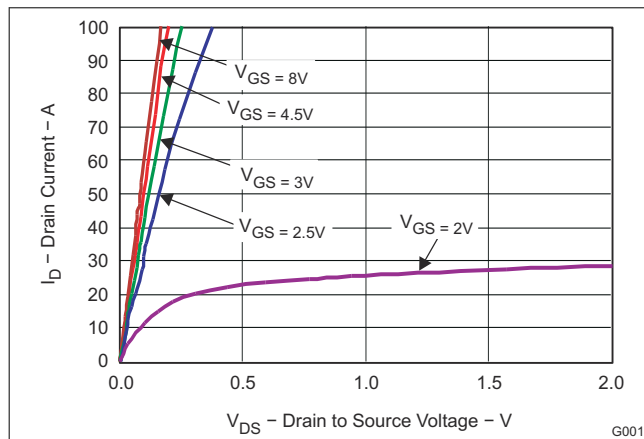
## 6 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



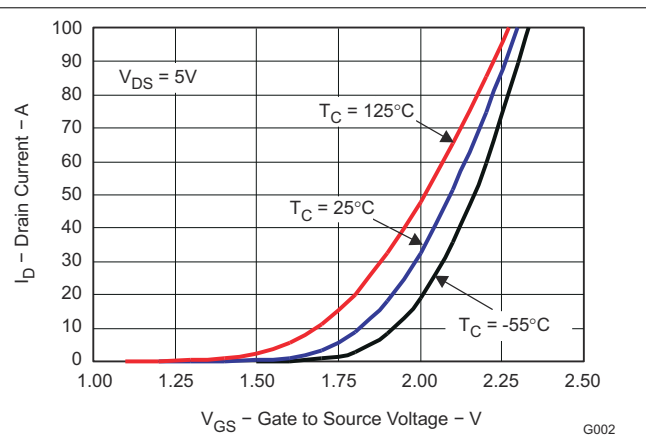
## 6 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



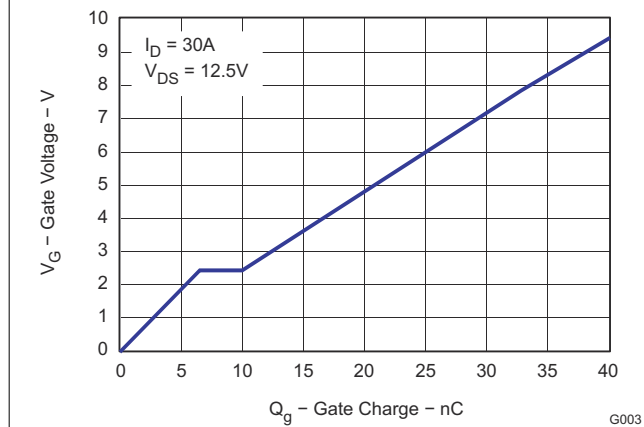
**Figure 6-2. Saturation Characteristics**

G001



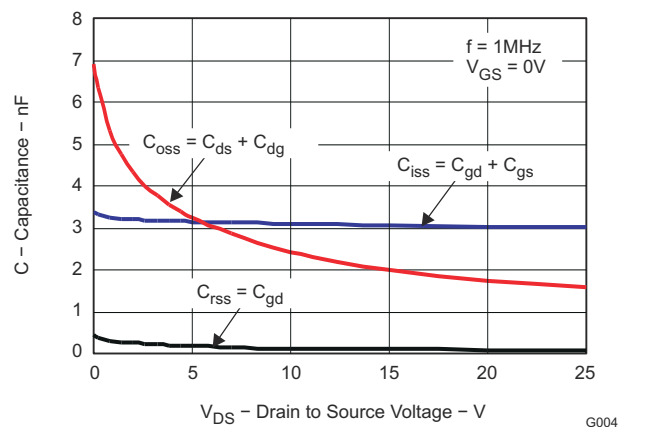
**Figure 6-3. Transfer Characteristics**

G002



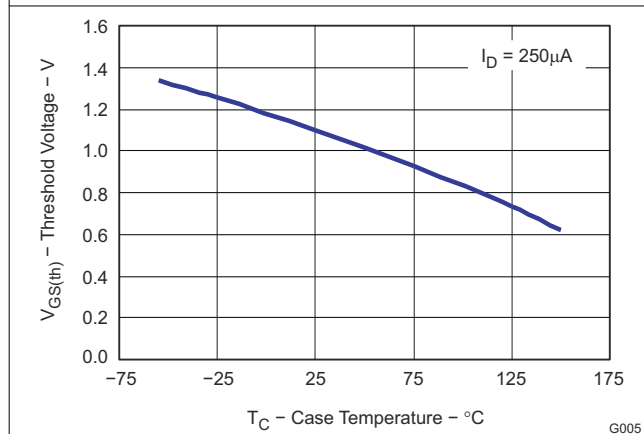
**Figure 6-4. Gate Charge**

G003



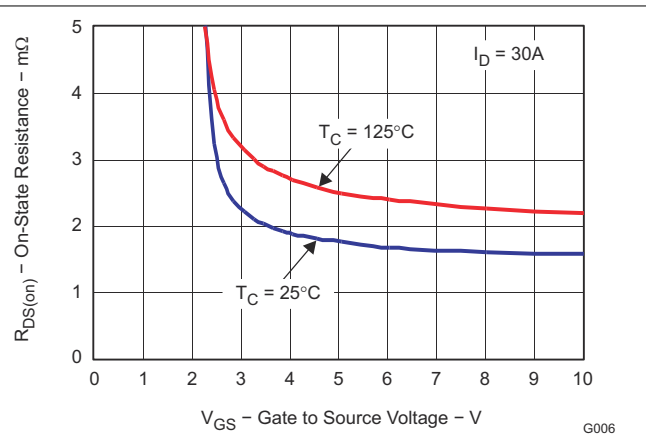
**Figure 6-5. Capacitance**

G004



**Figure 6-6. Threshold Voltage vs. Temperature**

G005

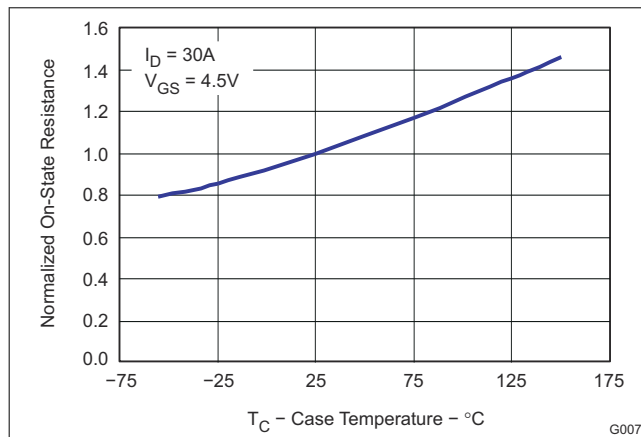


**Figure 6-7. On-State Resistance vs. Gate to Source Voltage**

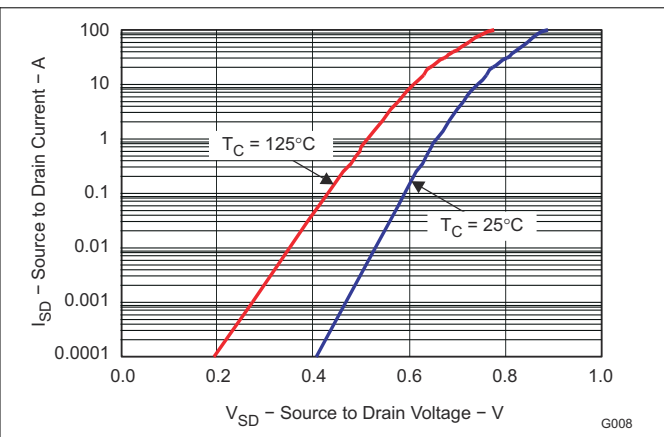
G006

## 6 Typical MOSFET Characteristics (continued)

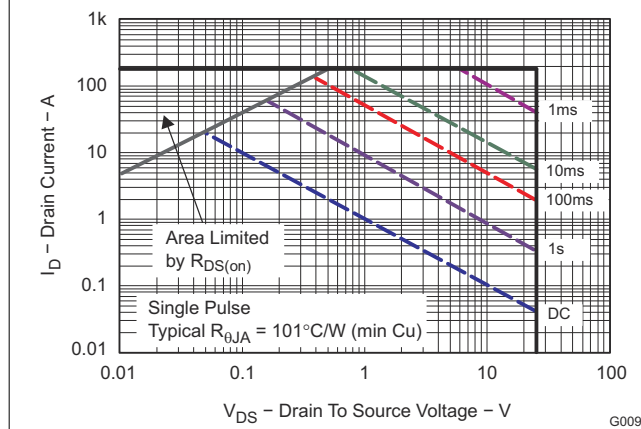
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



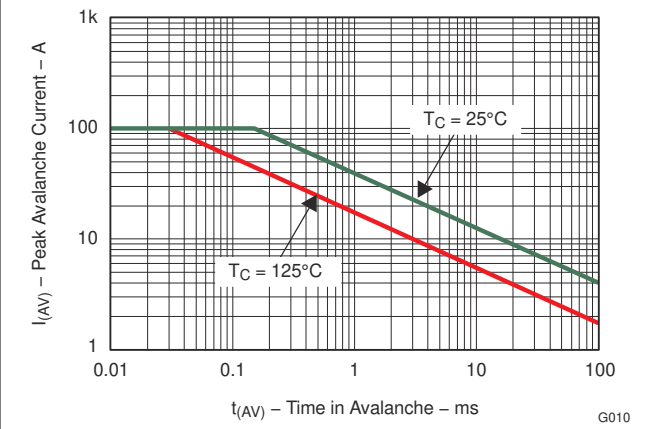
**Figure 6-8. Normalized On-State Resistance vs. Temperature**



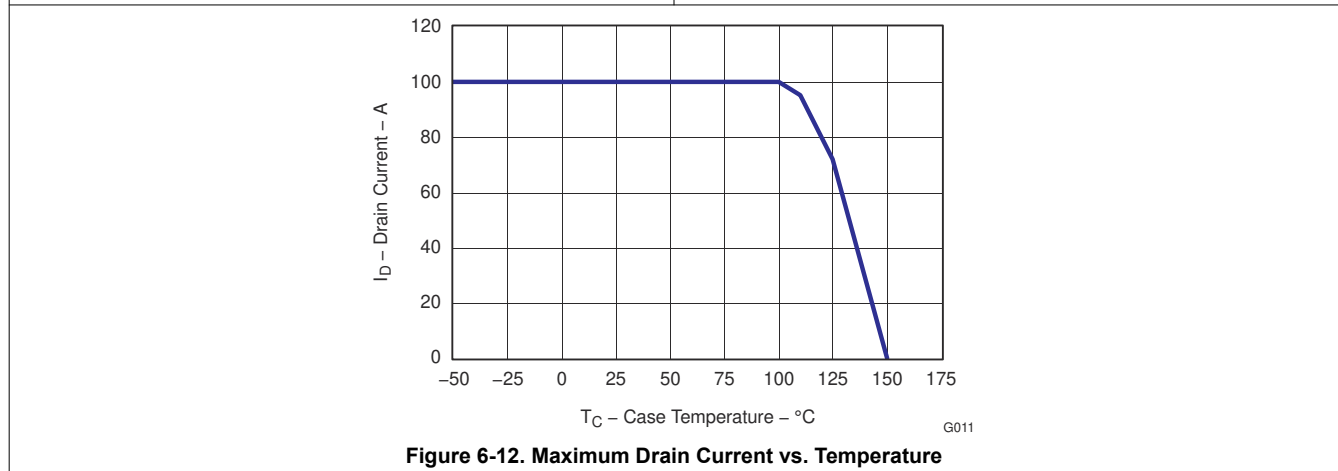
**Figure 6-9. Typical Diode Forward Voltage**



**Figure 6-10. Maximum Safe Operating Area**



**Figure 6-11. Single Pulse Unclamped Inductive Switching**



**Figure 6-12. Maximum Drain Current vs. Temperature**

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16325Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16325	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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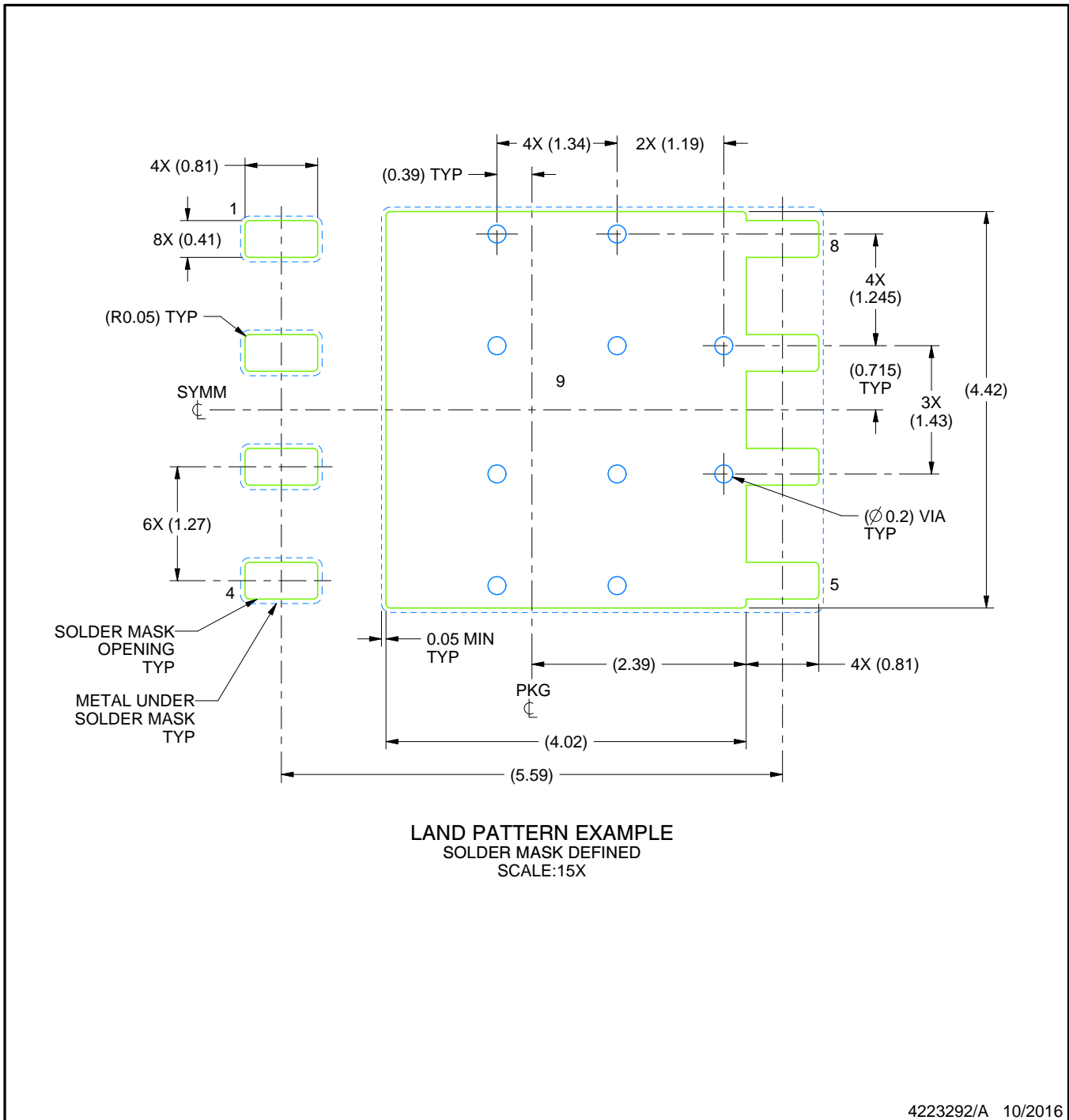


# EXAMPLE BOARD LAYOUT

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

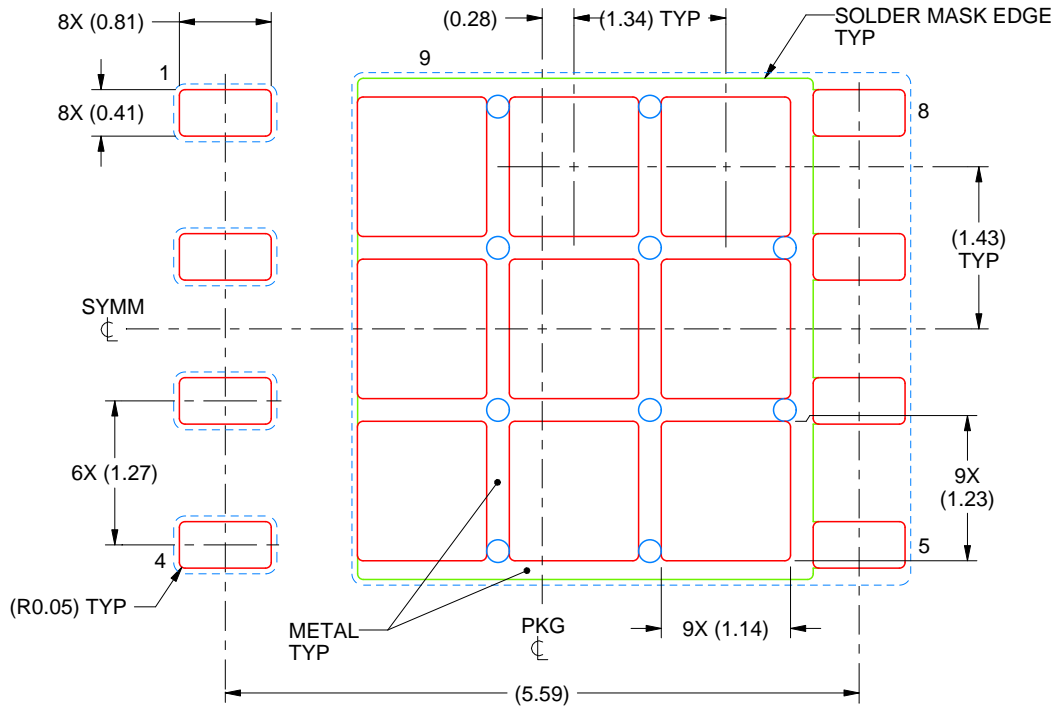
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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