To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

3823 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0146-0202
Rev.2.02
Jun.19.2007

DESCRIPTION

The 3823 group is the 8-bit microcomputer based on the 740 family core technology.

The 3823 group has the LCD drive control circuit, an 8-channel A/D converter, a serial interface, a watchdog timer, a ROM correction function, and as additional functions.

The various microcomputers in the 3823 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

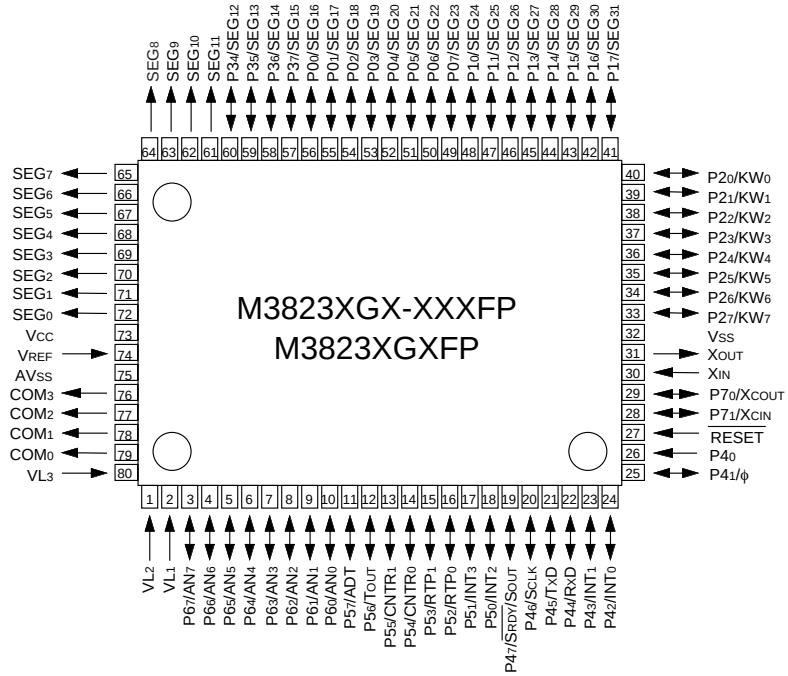
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.4 µs
  (at f(XIN) = 10 MHz, High-speed mode)
- Memory size
  ROM ..... 16 K to 60 K bytes
  RAM ..... 640 to 2560 bytes
- ROM correction function ..... 32 bytes × 2 blocks
- Watchdog timer ..... 8-bit × 1
- Programmable input/output ports 49
- Input ports 5
- Software pull-up/pull-down resistors (Ports P0-P7 except port $P4_0$)
- Interrupts ..... 17 sources, 16 vectors
  (includes key input interrupt)
- Key Input Interrupt (Key-on Wake-Up) 8
- Timers ..... 8-bit × 3, 16-bit × 2
- Serial interface ..... 8-bit × 1 (UART or Clock-synchronized)
- A/D converter ..... 10-bit × 8 channels or 8-bit × 8 channels
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty 1/2, 1/3, 1/4
  Common output 4
  Segment output 32
- Main clock generating circuits ..... Built-in feedback resistor
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Sub-clock generating circuits
  (connect to external quartz-crystal oscillator or on-chip oscillator)
- Power source voltage
  In frequency/2 mode (f(XIN) ≤ 10 MHz) ..... 4.5 to 5.5 V
  In frequency/2 mode (f(XIN) ≤ 8 MHz) ..... 4.0 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 10 MHz) ..... 2.5 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 8 MHz) ..... 2.0 to 5.5 V
  In frequency/4 mode (f(XIN) ≤ 5 MHz) ..... 1.8 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 10 MHz) ..... 2.5 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 8 MHz) ..... 2.0 to 5.5 V
  In frequency/8 mode (f(XIN) ≤ 5 MHz) ..... 1.8 to 5.5 V
  In low-speed mode ..... 1.8 to 5.5 V
- Power dissipation
  In frequency/2 mode ..... 18 mW (std.)
  (at f(XIN) = 8 MHz, Vcc = 5 V, Ta = 25 °C)
  In low-speed mode at XCIN ..... 18 µW (std.)
  (at f(XIN) stopped, f(XCIN) = 32 kHz, Vcc = 2.5 V, Ta = 25 °C)
  In low-speed mode at on-chip oscillator ..... 35 µW (std.)
  (at f(XIN) stopped, f(XCIN) = stopped, Vcc = 2.5 V, Ta = 25 °C)
- Operating temperature range ..... – 20 to 85 °C

APPLICATIONS

Camera, audio equipment, household appliances, consumer electronics, etc.

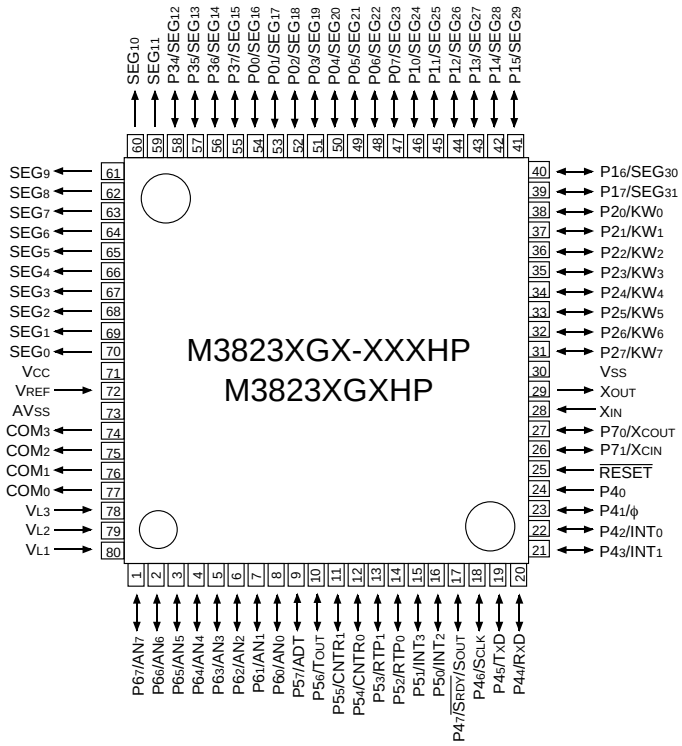
PIN CONFIGURATION (TOP VIEW)



Package code : PRQP0080GB-A (80P6N-A) (80-pin plastic-molded QFP)

Fig. 1 M3823XGX-XXXFP pin configuration

PIN CONFIGURATION (TOP VIEW)



Package code : PLQP0080KB-A (80P6Q-A) (80-pin plastic-molded LQFP)

Fig. 2 M3823XGX-XXXHP pin configuration

Table 1 Performance overview

Parameter		Function
Number of basic instructions		71
Instruction execution time		0.4 μs (Minimum instruction, f(XIN) 10 MHz, High-speed mode)
Oscillation frequency		10 MHz (Maximum)
Memory sizes	ROM	16 K to 60 K bytes
	RAM	640 to 2560 bytes
Input port	P34-P37, P40	4-bit × 1, 1-bit × 1 (4 pins sharing SEG)
I/O port	P0-P2, P41-P47, P5, P6, P70, P71	8-bit × 5, 7-bit × 1, 2 bit × 1 (16 pins sharing SEG)
Interrupt		17 sources, 16 vectors (includes key input interrupt)
Timer		8-bit × 3, 16-bit × 2
Serial interface		8-bit × 1 (UART or Clock-synchronized)
A/D converter		10-bit × 8 channels or 8 bit × 8 channels
Watchdog timer		8-bit × 1
ROM correction function		32 bytes × 2 blocks
LCD drive control circuit	Bias	1/2, 1/3
	Duty	2, 3, 4
	Common output	4
	Segment output	32
Main clock generating circuits		Built-in feedback resistor (connect to external ceramic rasonator or quartz-crystal oscillator)
Sub-clock generating circuits		Built-in feedback resistor (connect to external quartz-crystal oscillator or on-chip oscillator)
Power source voltage	In frequency/2 mode (f(XIN) ≤ 10MHz)	4.5 to 5.5V
	In frequency/2 mode (f(XIN) ≤ 8MHz)	4.0 to 5.5V
	In frequency/4 mode (f(XIN) ≤ 10MHz)	2.5 to 5.5V
	In frequency/4 mode (f(XIN) ≤ 8MHz)	2.0 to 5.5V
	In frequency/4 mode (f(XIN) ≤ 5MHz)	1.8 to 5.5V
	In frequency/8 mode (f(XIN) ≤ 10MHz)	2.5 to 5.5V
	In frequency/8 mode (f(XIN) ≤ 8MHz)	2.0 to 5.5V
	In frequency/8 mode (f(XIN) ≤ 5MHz)	1.8 to 5.5V
	In low-speed mode	1.8 to 5.5V
Power dissipation	In frequency/2 mode	Std. 18 mW (Vcc = 5V, f(XIN) = 8MHz, Ta = 25 °C)
	In low-speed mode at XCIN	Std. 18 μW (Vcc = 2.5V, f(XIN) = stopped, f(XCIN) = 32kHz, Ta = 25 °C)
	In low-speed mode at on-chip oscillator	Std. 35 μW (Vcc = 2.5V, f(XIN) = stopped, f(XCIN) = stopped, Ta = 25 °C)
Input/Output characteristics	Input/Output withstand voltage	VCC
	Output current	10mA
Operating temperature range		-20 to 85 °C
Device structure		CMOS sillicon gate
Package		80-pin plastic molded LQFP/QFP

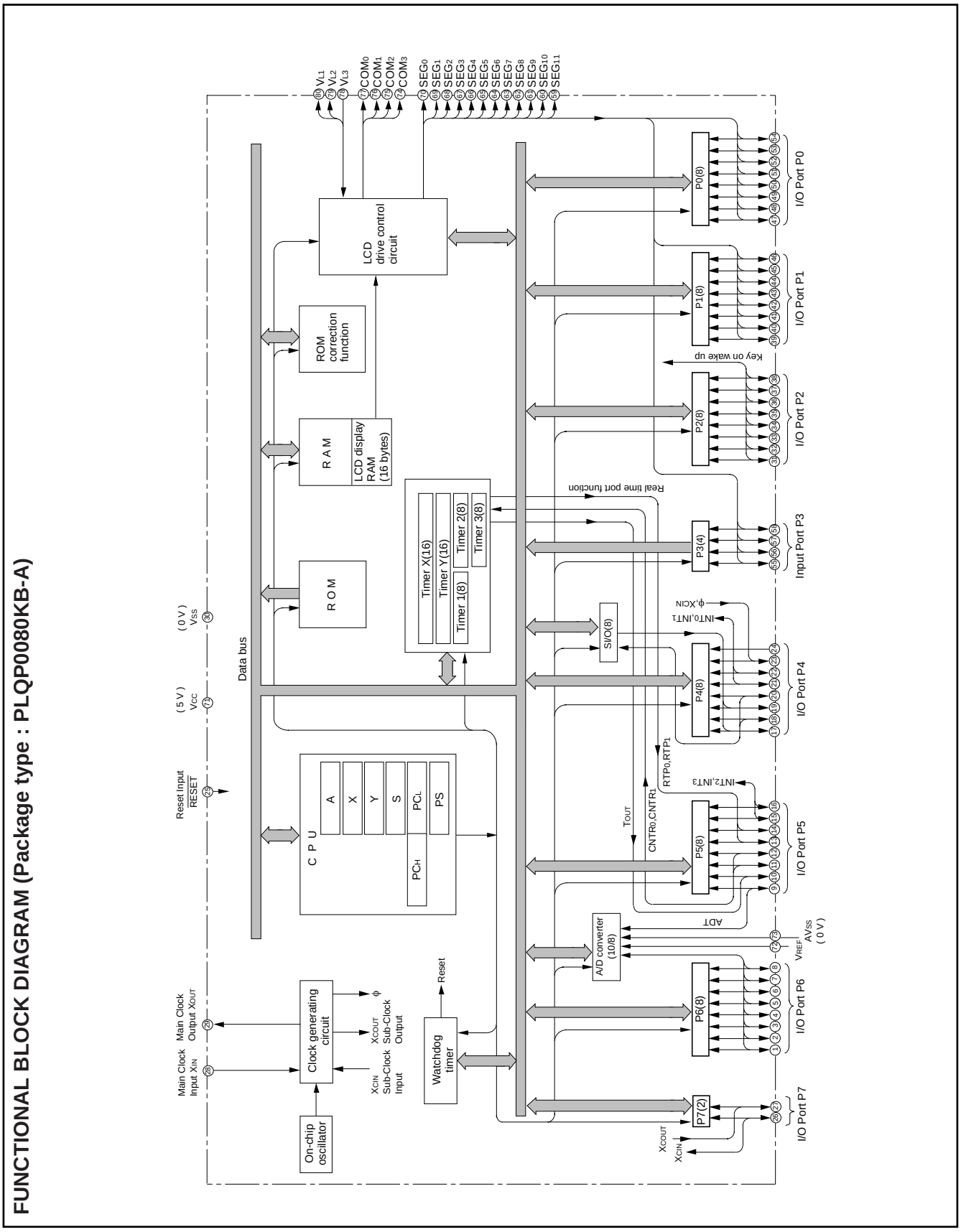


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 2 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of power source to V_{CC}, and 0 V to V_{SS}. (For the limits of V_{CC}, refer to "Recommended operating conditions").	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A/D converter.	
AV_{SS}	Analog power source	•GND input pin for A/D converter. •Connect to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L".	
X_{IN}	Clock input	•Input and output pins for the main clock generating circuit. •Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. •Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. •This clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
V_{L1}–V_{L3}	LCD power source	•Input 0 ≤ V_{L1} ≤ V_{L2} ≤ V_{L3} voltage. •Input 0 – V_{L3} voltage to LCD.	
COM_0–COM_3	Common output	•LCD common output pins. •COM_2 and COM_3 are not used at 1/2 duty ratio. •COM_3 is not used at 1/3 duty ratio.	
SEG_0–SEG_{11}	Segment output	•LCD segment output pins.	
$P0_0/SEG_{16}$–$P0_7/SEG_{23}$	I/O port P0	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each port to be individually programmed as either input or output. •Pull-down control is enabled.	•LCD segment output pins
$P1_0/SEG_{24}$–$P1_7/SEG_{31}$	I/O port P1		
$P2_0/KW_0$ – $P2_7/KW_7$	I/O port P2	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Key input (key-on wake-up) interrupt input pins
$P3_4/SEG_{12}$ – $P3_7/SEG_{15}$	Input port P3	•4-bit input port. •CMOS compatible input level. •Pull-down control is enabled.	•LCD segment output pins

Table 3 Pin description (2)

Pin	Name	Function	Function except a port function
$P4_0$	Input port P4	•1-bit Input port. •CMOS compatible input level.	•QzROM program power pin
$P4_1/\phi$	I/O port P4	•7-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•ϕ clock output pin
$P4_2/INT_0$, $P4_3/INT_1$			•Interrupt input pins
$P4_4/RxD$, $P4_5/TxD$, $P4_6/SCLK$, $P4_7/SRDY/SOUT$			•Serial interface function pins
$P5_0/INT_2$, $P5_1/INT_3$	I/O port P5	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Interrupt input pins
$P5_2/RTP_0$, $P5_3/RTP_1$			•Real time port function pins
$P5_4/CNTR_0$, $P5_5/CNTR_1$			•Timer X, Y function pins
$P5_6/TOUT$			•Timer 2 output pins
$P5_7/ADT$			•A/D trigger input pins
$P6_0/AN_0$–$P6_7/AN_7$	I/O port P6	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•A/D conversion input pins
$P7_0/XCOUT$, $P7_1/XCIN$	I/O port P7	•2-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Sub-clock generating circuit I/O pins. (Connect a resonator. External clock cannot be used.)

PART NUMBERING

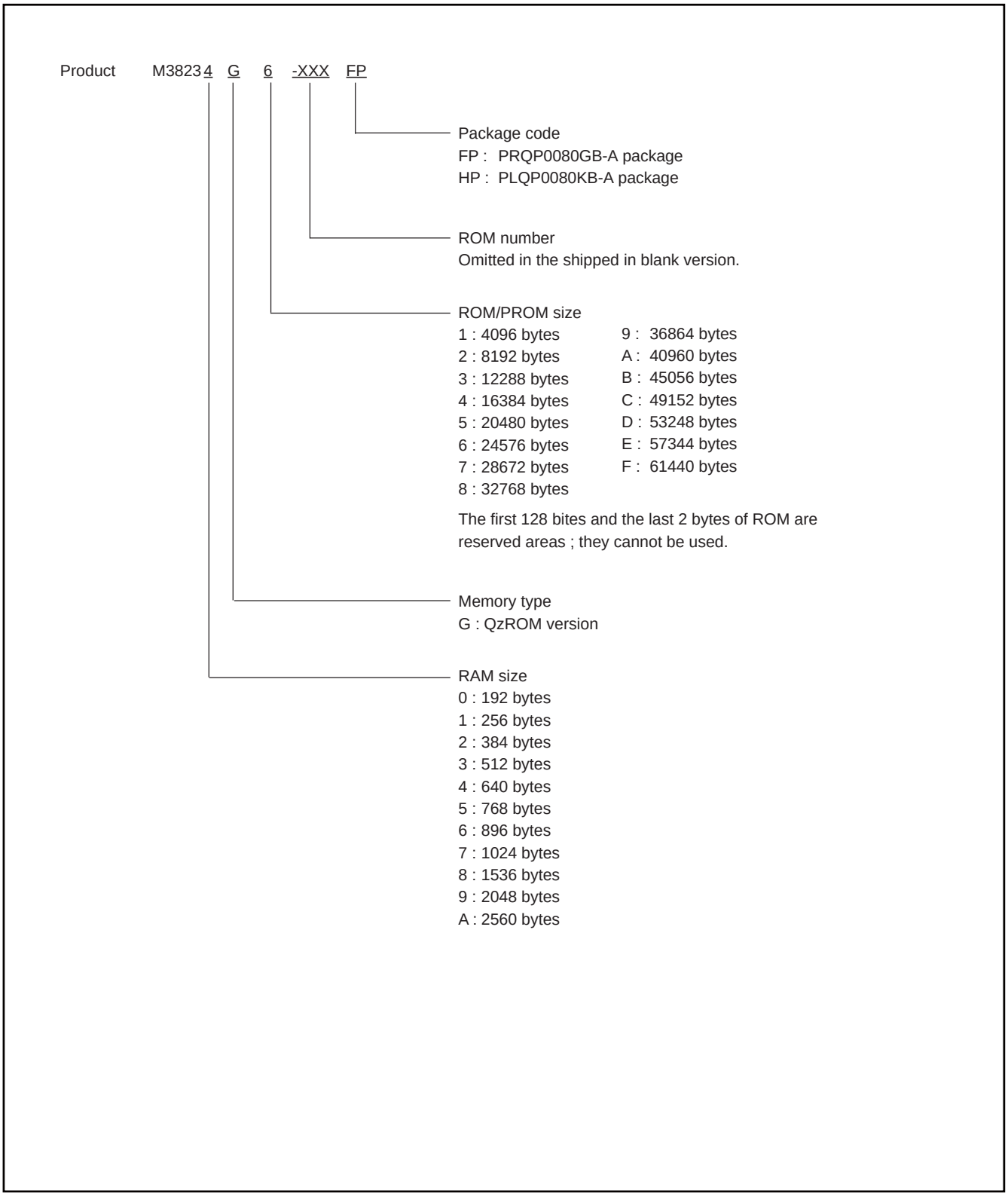


Fig. 4 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3823 group as follows:

Memory Type

Support for QzROM version.

Memory Size

ROM size ..... 16 K to 60 K bytes
RAM size ..... 640 to 2560 bytes

Package

PRQP0080GB-A ..... 0.8 mm-pitch plastic molded QFP
PLQP0080KB-A ..... 0.5 mm-pitch plastic molded LQFP

Memory Expansion Plan

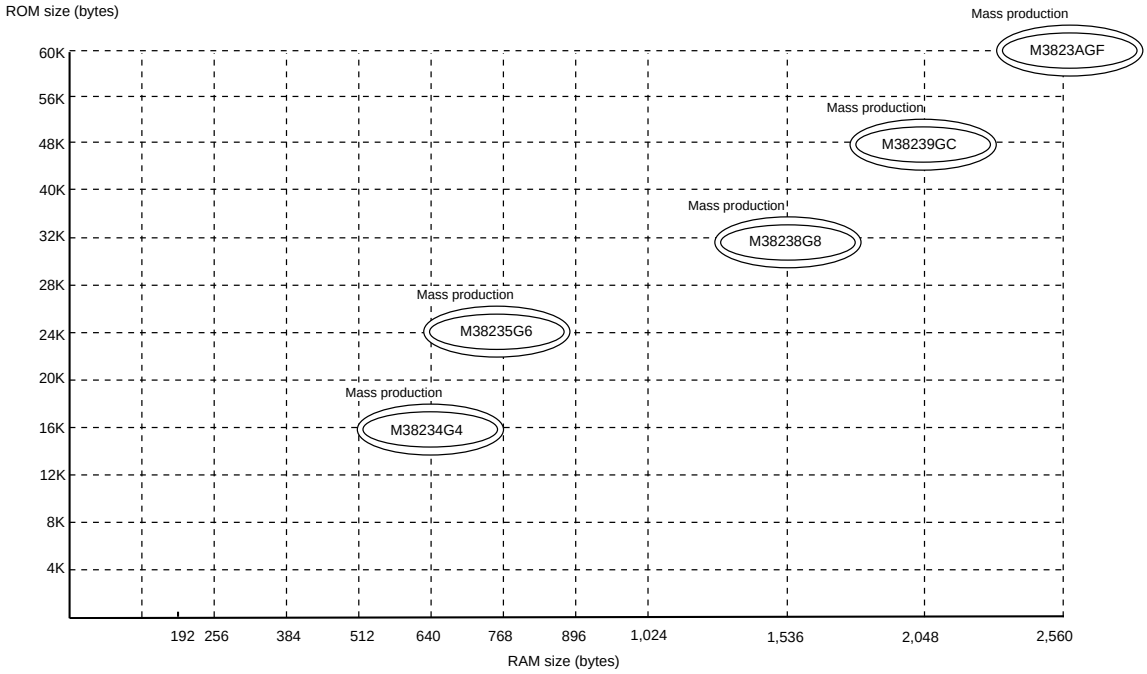


Fig. 5 Memory expansion plan

Currently products are listed below.

Table 4 List of products

Part No.	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M3823AGF-XXXFP	61440 (61310)	2560 **(Note 1)**	PRQP0080GB-A	
M3823AGF-XXXHP			PLQP0080KB-A	
M3823AGFFP			PRQP0080GB-A	Blank
M3823AGFHP			PLQP0080KB-A	Blank
M38239GC-XXXFP	49152 (49022)	2048 **(Note 2)**	PRQP0080GB-A	
M38239GC-XXXHP			PLQP0080KB-A	
M38239GCFP			PRQP0080GB-A	Blank
M38239GCHP			PLQP0080KB-A	Blank
M38238G8-XXXFP	32768 (32638)	1536 **(Note 2)**	PRQP0080GB-A	
M38238G8-XXXHP			PLQP0080KB-A	
M38238G8FP			PRQP0080GB-A	Blank
M38238G8HP			PLQP0080KB-A	Blank
M38235G6-XXXFP	24576 (24446)	768 **(Note 2)**	PRQP0080GB-A	
M38235G6-XXXHP			PLQP0080KB-A	
M38235G6FP			PRQP0080GB-A	Blank
M38235G6HP			PLQP0080KB-A	Blank
M38234G4-XXXFP	16384 (16254)	640 **(Note 2)**	PRQP0080GB-A	
M38234G4-XXXHP			PLQP0080KB-A	
M38234G4FP			PRQP0080GB-A	Blank
M38234G4HP			PLQP0080KB-A	Blank

Note 1: RAM size includes RAM for LCD display and ROM corrections.
Note 2: RAM size includes RAM for LCD display.

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3823 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

The central processing unit (CPU) has six registers. Figure 6 shows the 740 Family CPU register structure.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.

Store registers other than those described in Table 4 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

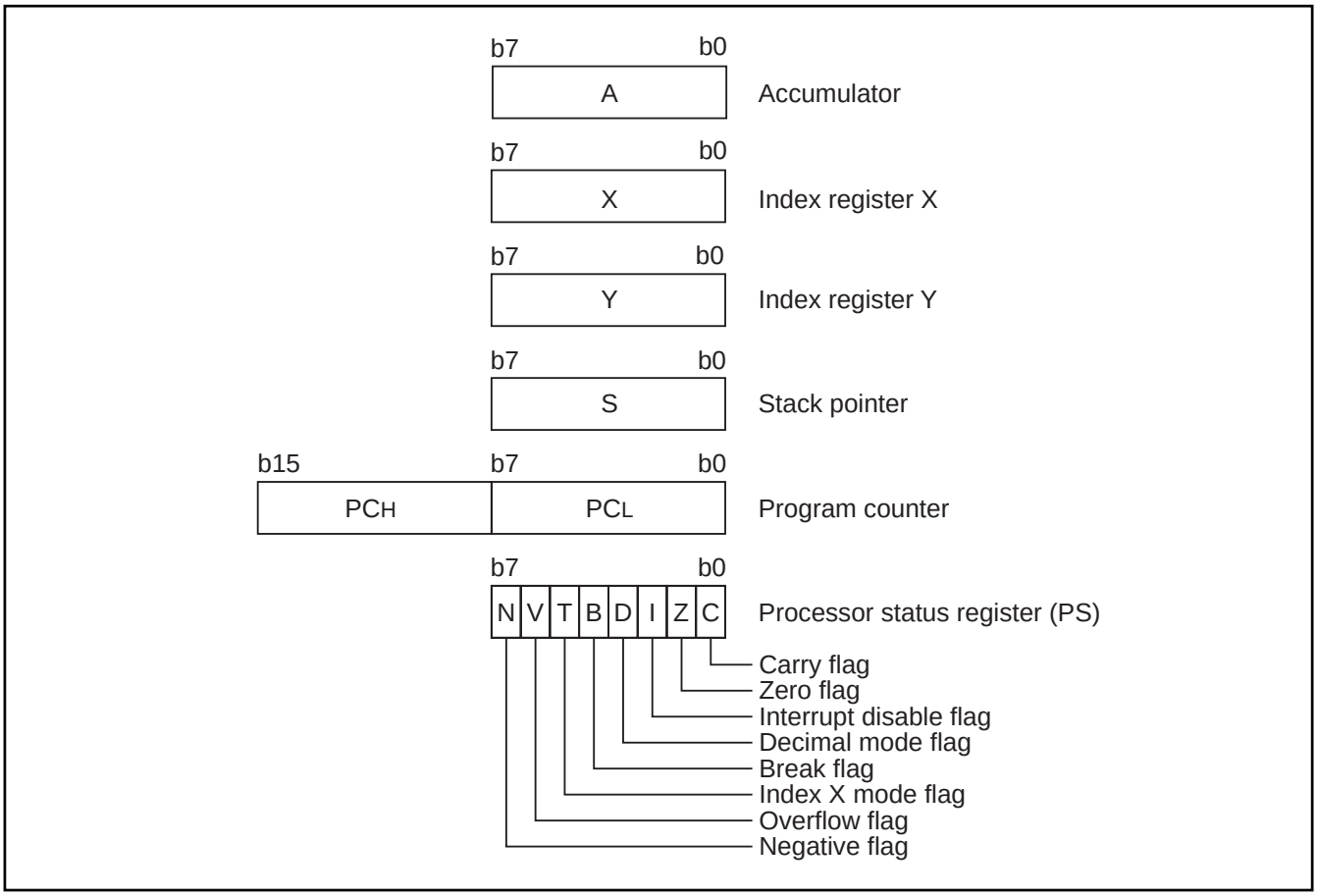


Fig. 6 740 Family CPU register structure

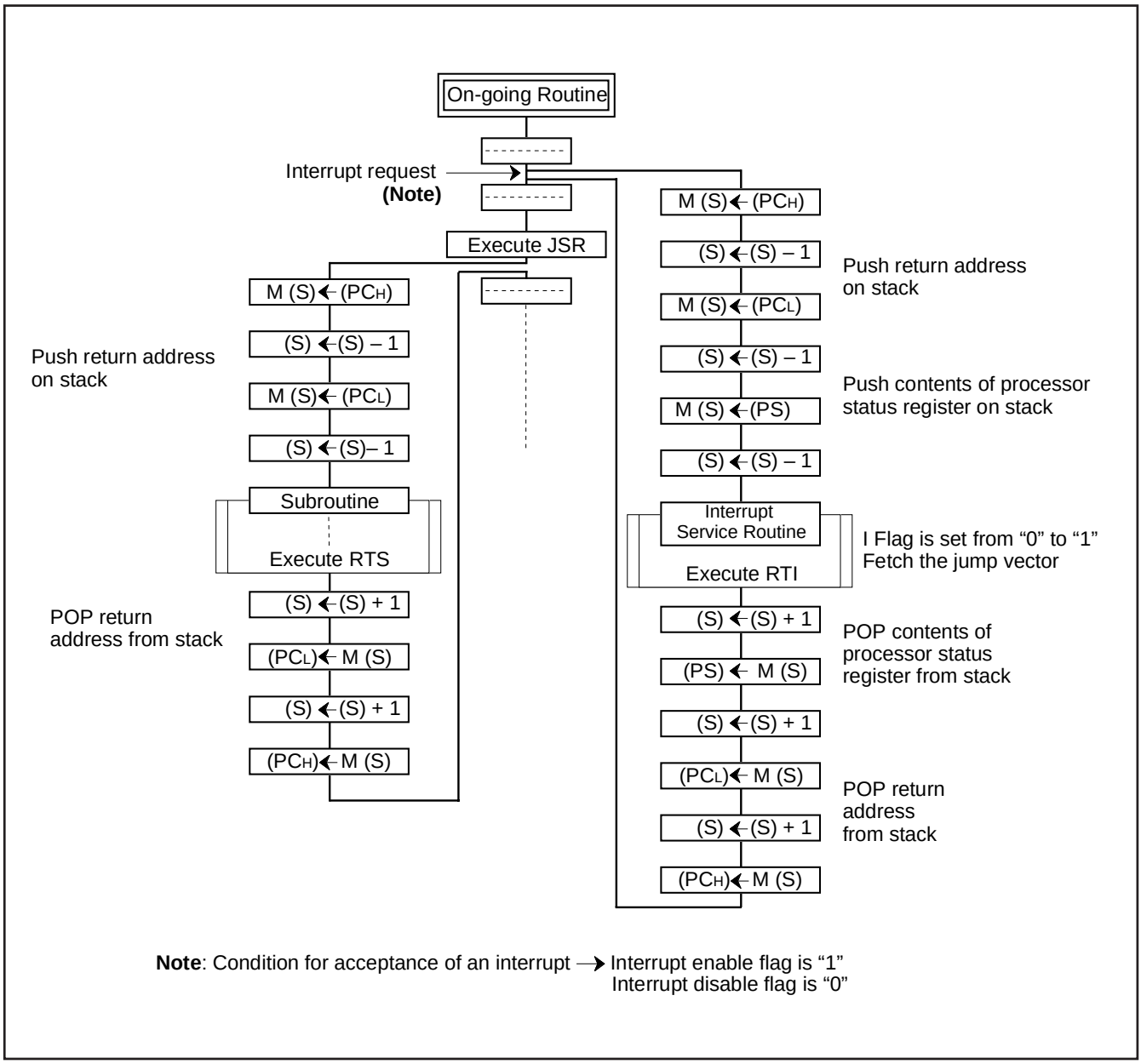


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

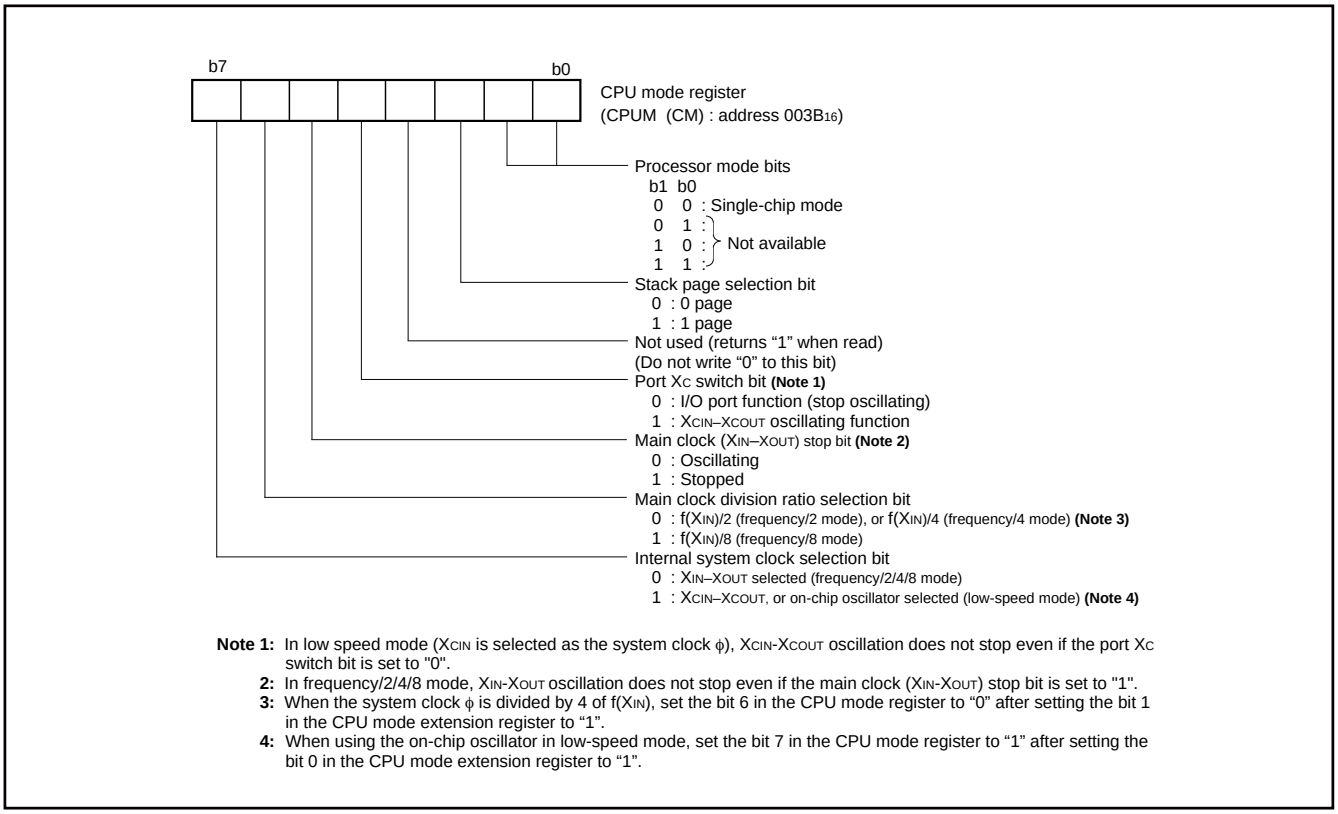
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 6 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.
The CPU mode register is allocated at address 003B16.

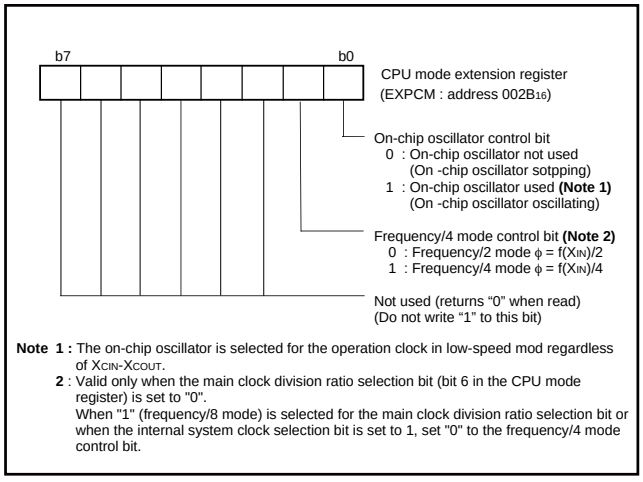


Note 1: In low speed mode (XCIN is selected as the system clock ϕ), XCIN-XCOUT oscillation does not stop even if the port XC switch bit is set to "0".
2: In frequency/2/4/8 mode, XIN-XOUT oscillation does not stop even if the main clock (XIN-XOUT) stop bit is set to "1".
3: When the system clock ϕ is divided by 4 of f(XIN), set the bit 6 in the CPU mode register to "0" after setting the bit 1 in the CPU mode extension register to "1".
4: When using the on-chip oscillator in low-speed mode, set the bit 7 in the CPU mode register to "1" after setting the bit 0 in the CPU mode extension register to "1".

Fig. 8 Structure of CPU mode register

[CPU Mode Extension Register (EXPCM)] 002B16

f(XIN) divided by 4 for the system clock f and the on-chip oscillator for the system clock f in low-speed mode can be selected by setting the CPU mode extension register. When the system clock f is divided by 4 of f(XIN), set the bit 6 in the CPU mode register to "0" after setting the bit 1 in the CPU mode extension register to "1". When using the on-chip oscillator in low-speed mode, set the bit 7 in the CPU mode register to "1" after setting the bit 0 in the CPU mode extension register to "1".



Note 1 : The on-chip oscillator is selected for the operation clock in low-speed mod regardless of XCIN-XCOUT.
2 : Valid only when the main clock division ratio selection bit (bit 6 in the CPU mode register) is set to "0".
When "1" (frequency/8 mode) is selected for the main clock division ratio selection bit or when the internal system clock selection bit is set to 1, set "0" to the frequency/4 mode control bit.

Fig. 9 Structure of CPU mode extension register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function register (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Code Protect Address

"00_{16}" is written into ROM code protect address (other than the user ROM area) when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00_{16}" or "FF_{16}" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
640	$02BF_{16}$
768	$033F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$
2560	$0A3F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
16384	$C000_{16}$	$C080_{16}$
24576	$A000_{16}$	$A080_{16}$
32768	8000_{16}	8080_{16}
49152	4000_{16}	4080_{16}
61440	1000_{16}	1080_{16}

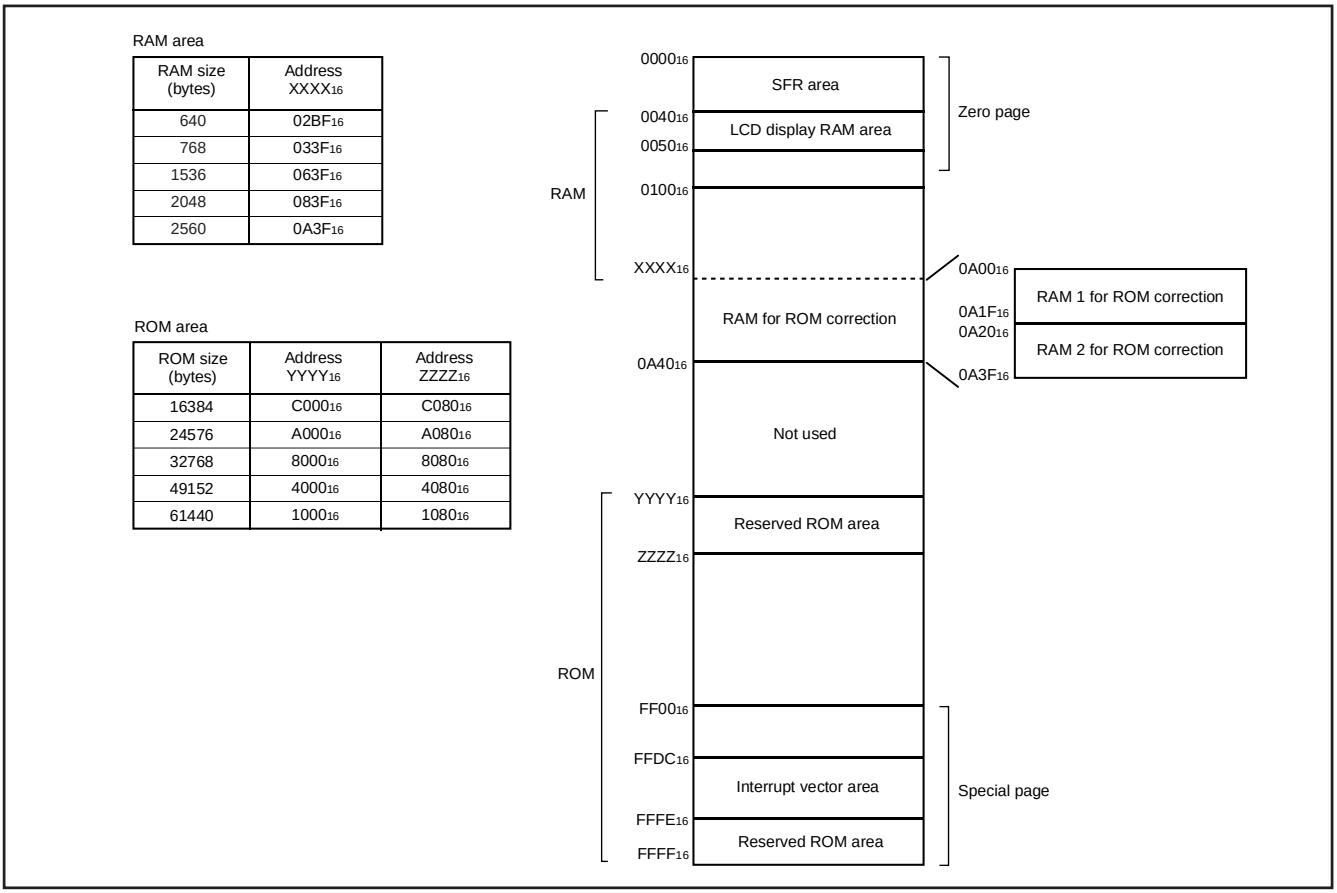


Fig. 10 Memory map diagram

0000₁₆	Port P0 register (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 register (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 register (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 register (P3)
0007₁₆	
0008₁₆	Port P4 register (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 register (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 register (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 register (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	ROM correction address 1 high-order register (RCA1H)
0011₁₆	ROM correction address 1 low-order register (RCA1L)
0012₁₆	ROM correction address 2 high-order register (RCA2H)
0013₁₆	ROM correction address 2 low-order register (RCA2L)
0014₁₆	ROM correction enable register (RCR)
0015₁₆	
0016₁₆	PULL register A (PULLA)
0017₁₆	PULL register B (PULLB)
0018₁₆	Transmit/Receive buffer register(TB/RB)
0019₁₆	Serial I/O status register (SIOSTS)
001A₁₆	Serial I/O control register (SIO1CON)
001B₁₆	UART control register (UARTCON)
001C₁₆	Baud rate generator (BRG)
001D₁₆	
001E₁₆	
001F₁₆	

0020₁₆	Timer X low-order register (TXL)
0021₁₆	Timer X high-order register (TXH)
0022₁₆	Timer Y low-order register (TYL)
0023₁₆	Timer Y high-order register (TYH)
0024₁₆	Timer 1 register (T1)
0025₁₆	Timer 2 register (T2)
0026₁₆	Timer 3 register (T3)
0027₁₆	Timer X mode register (TXM)
0028₁₆	Timer Y mode register (TYM)
0029₁₆	Timer 123 mode register (T123M)
002A₁₆	ϕ output control register (CKOUT)
002B₁₆	CPU mode expansion register (EXPCM)
002C₁₆	Temporary data register 0 (TD0)
002D₁₆	Temporary data register 1 (TD1)
002E₁₆	Temporary data register 2 (TD2)
002F₁₆	RRF register (RRFR)
0030₁₆	Peripheral function expansion register (EXP)
0031₁₆	
0032₁₆	
0033₁₆	
0034₁₆	AD control register (ADCON)
0035₁₆	AD conversion high-order register (ADH)
0036₁₆	AD conversion low-order register (ADL)
0037₁₆	Watchdog timer register (WDT)
0038₁₆	Segment output enable register (SEG)
0039₁₆	LCD mode register (LM)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1(IREQ1)
003D₁₆	Interrupt request register 2(IREQ2)
003E₁₆	Interrupt control register 1(ICON1)
003F₁₆	Interrupt control register 2(ICON2)

Note: Do not access to the SFR area including nothing.

Fig. 11 Memory map of special function register (SFR)

I/O PORTS

Direction Registers (ports P2, P41-P47, and P5-P7)

The 3823 group has 49 programmable I/O pins arranged in seven I/O ports (ports P0–P2, P41–P47 and P5-P7). The I/O ports P2, P41–P47 and P5-P7 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Direction Registers (ports P0 and P1)

Ports P0 and P1 have direction registers which determine the input/output direction of each individual port.

Each port in a direction register corresponds to one port, each port can be set to be input or output. When “0” is written to the bit 0 of a direction register, that port becomes an input port. When “1” is written to that port, that port becomes an output port. Bits 1 to 7 of ports P0 and P1 direction registers are not used.

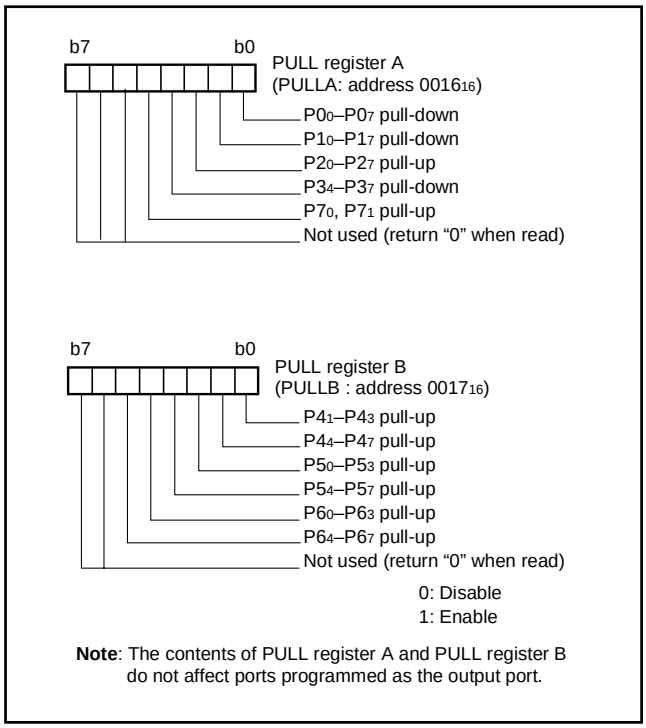
Ports P3 and P40

These ports are only for input.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016$_{16}$) or the PULL register B (address 0017$_{16}$), ports except for port P40 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.



Note: The contents of PULL register A and PULL register B do not affect ports programmed as the output port.

Fig. 12 Structure of PULL register A and PULL register B

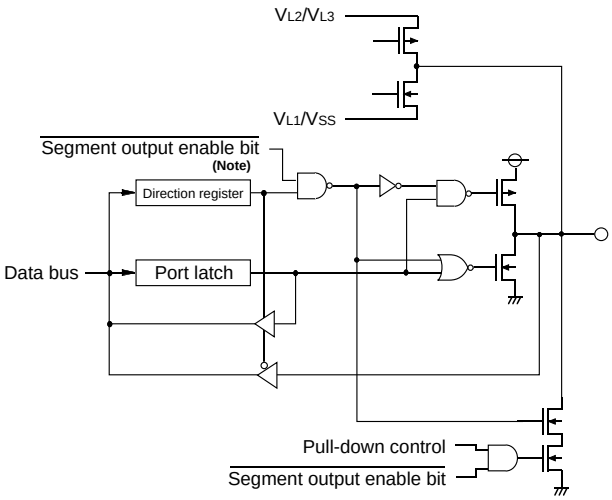
Table 7 List of I/O port function

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P0$_0$/SEG$_{16}$–P0$_7$/SEG$_{23}$	Port P0	Input/output, individual ports	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P1$_0$/SEG$_{24}$–P1$_7$/SEG$_{31}$	Port P1					
P2$_0$/KW$_0$–P2$_7$/KW$_7$	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register 2	(2)
P3$_4$/SEG$_{12}$–P3$_7$/SEG$_{15}$	Port P3	Input	CMOS compatible input level	LCD segment output	PULL register A Segment output enable register	(3)
P4$_0$	Port P4	Input	CMOS compatible input level	QzROM program power pin		(4)
P4$_1$/ϕ		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	ϕ clock output X$_{CIN}$ frequency signal output	PULL register B ϕ output control register Peripheral function extension register	(5)
P4$_2$/INT$_0$, P4$_3$/INT$_1$				External interrupt input	PULL register B Interrupt edge selection register	(2)
P4$_4$/RxD				Serial I/O function input/output	PULL register B	(6)
P4$_5$/TxD					Serial I/O control register	(7)
P4$_6$/SCLK					Serial I/O status register	(8)
P4$_7$/$\overline{\text{SRDY}}$/SOUT					UART control register Peripheral function extension register	(9)
P5$_0$/INT$_2$, P5$_1$/INT$_3$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	PULL register B Interrupt edge selection register	(2)
P5$_2$/RTP$_0$, P5$_3$/RTP$_1$				Real time port function output	PULL register B Timer X mode register	(10)
P5$_4$/CNTR$_0$				Timer X function I/O	PULL register B Timer X mode register	(11)
P5$_5$/CNTR$_1$				Timer Y function input	PULL register B Timer Y mode register	(12)
P5$_6$/TOUT				Timer 2 function output	PULL register B Timer 123 mode register	(13)
P5$_7$/ADT				A/D trigger input	PULL register B	(12)
P6$_0$/AN$_0$–P6$_7$/AN$_7$	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A/D conversion input	A/D control register	(14)
P7$_0$/XCOUT	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	PULL register A CPU mode register	(15)
P7$_1$/XCIN						(16)
COM$_0$–COM$_3$	Common	Output	LCD common output		LCD mode register	(17)
SEG$_0$–SEG$_{11}$	Segment	Output	LCD segment output			(18)

Notes 1: For details of how to use double function ports as function I/O ports, refer to the applicable sections.

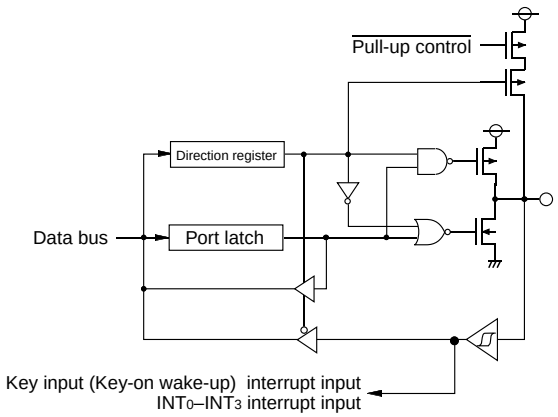
2: When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate. Especially, power source current may increase during execution of the STP and WIT instructions. Fix the unused input pins to "H" or "L" through a resistor.

(1) Ports P0, P1

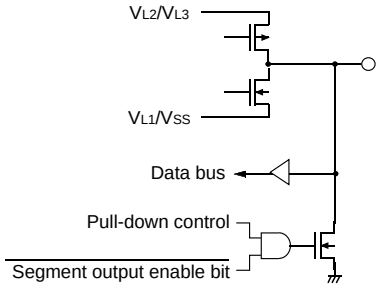


Note: Bit 0 of direction register.

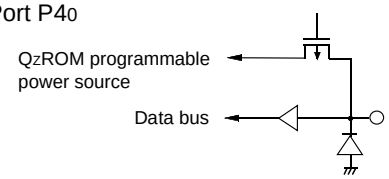
(2) Ports P2, P42, P43, P50, P51



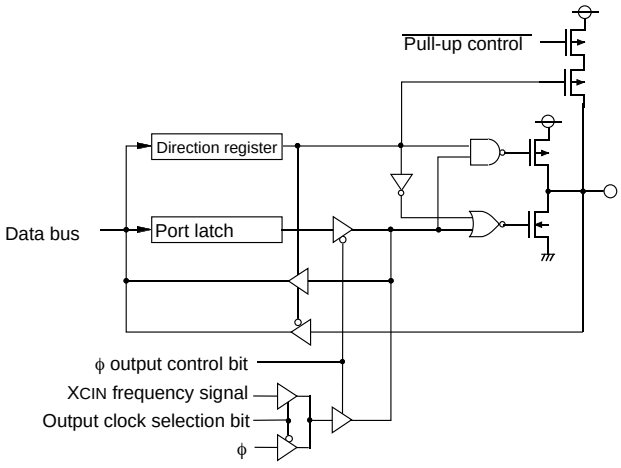
(3) Ports P34–P37



(4) Port P40



(5) Port P41



(6) Port P44

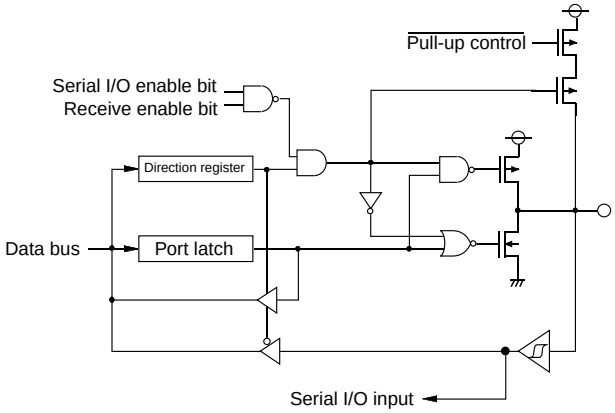


Fig. 13 Port block diagram (1)

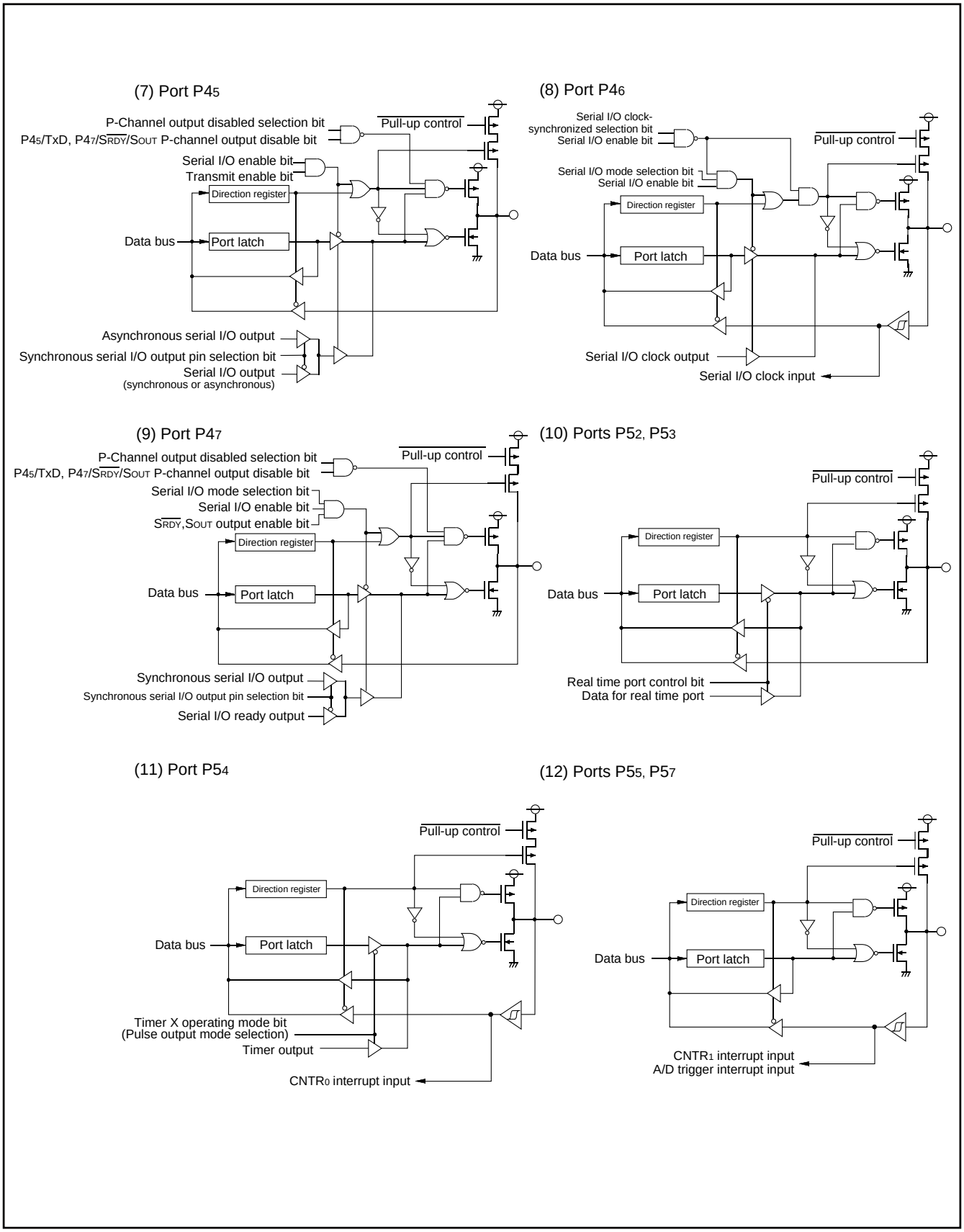
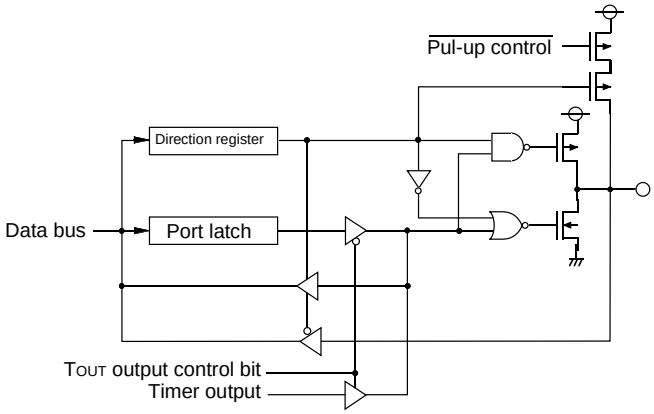
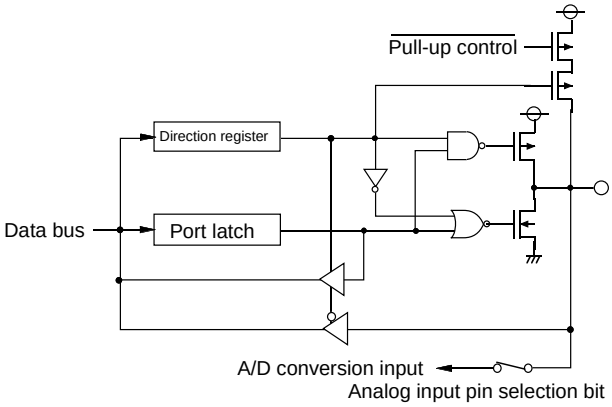


Fig. 14 Port block diagram (2)

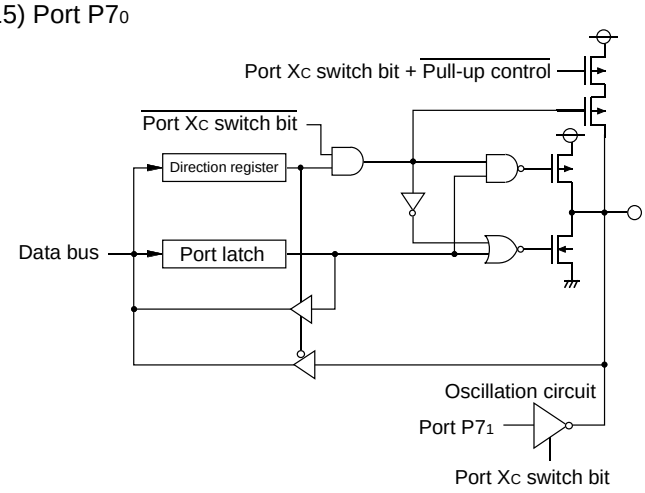
(13) Port $P5_6$



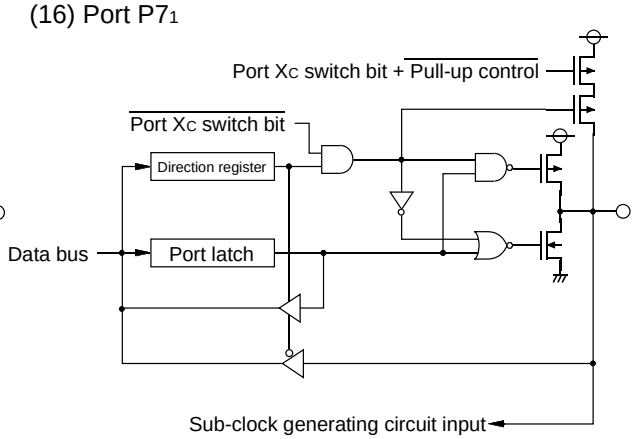
(14) Port P6



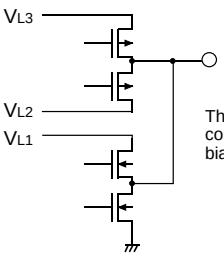
(15) Port $P7_0$



(16) Port $P7_1$

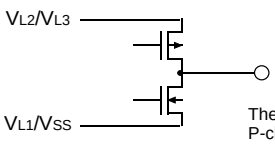


(17) COM_0–COM_3



The gate input signal of each transistor is controlled by the LCD duty ratio and the bias value.

(18) SEG_0–SEG_{11}



The voltage applied to the sources of P-channel and N-channel transistors is the controlled voltage by the bias value.

Fig. 15 Port block diagram (3)

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.

Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used). Pull-down the $P4_0$/(V_{PP}) pin.

We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.

Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 8 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2	Termination 3
P00/SEG16–P17/SEG23	I/O port	When selecting SEG output, open.	–
P10/SEG24–P17/SEG31			
P20/KW0–P27/KW7		When selecting KW function, perform termination of input port.	–
P34/SEG12–P37/SEG15	Input port	When selecting SEG output, open.	–
P40/(VPP)	Input port (pull-down)	–	–
P41/ϕ	I/O port	When selecting ϕ output, open.	–
P42/INT0		When selecting INT0 function, perform termination of input port.	–
P43/INT1		When selecting INT1 function, perform termination of input port.	–
P44/RxD		When selecting RxD function, perform termination of input port.	–
P45/TxD		When selecting TxD function, perform termination of output port.	–
P46/SCLK		When selecting external clock input, perform termination of input port.	When selecting internal clock output, perform termination of output port.
P47/$\overline{\text{SRDY}}$/SOUT		When selecting $\overline{\text{SRDY}}$ function, perform termination of output port.	When selecting SOUT function, perform termination of output port.
P50/INT2		When selecting INT2 function, perform termination of input port.	–
P51/INT3		When selecting INT3 function, perform termination of input port.	–
P52/RTP0		When selecting RTP0 function, perform termination of output port.	–
P53/RTP1		When selecting RTP1 function, perform termination of output port.	–
P54/CNTR0		When selecting CNTR0 input function, perform termination of input port.	When selecting CNTR0 output function, perform termination of output port.
P55/CNTR1		When selecting CNTR1 function, perform termination of input port.	–
P56/TOUT		When selecting TOUT function, perform termination of output port.	–
P57/ADT		When selecting ADT function, perform termination of input port.	–
P60/AN0–P67/AN7		When selecting AN function, these pins can be opened. (A/D conversion result cannot be guaranteed.)	–
P70/XCOUT P71/XCIN		Do not select XCIN-XCOUT oscillation function by program.	–
VL3 (Note)	Connect to VSS	–	–
VL2 (Note)	Connect to VSS	–	–
VL1 (Note)	Connect to VSS	–	–
COM0–COM3	Open	–	–
SEG0–SEG11	Open	–	–
AVSS	Connect to VSS	–	–
VREF	Connect to VCC or VSS	–	–
XOUT	When an external clock is input to the XIN pin, leave the XOUT pin open.	–	–

Note : The termination of VL3, VL2 and VL1 is applied when the bit 3 of the LCD mode register is “0”

INTERRUPTS

The 3823 group interrupts are vector interrupts with a fixed priority scheme, and generated by 16 sources among 17 sources: 8 external, 8 internal, and 1 software.

The interrupt sources, vector addresses (1) , and interrupt priority are shown in Table 9.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Figure 16 shows an interrupt control diagram.

An interrupt requests is accepted when all of the following conditions are satisfied:

- Interrupt disable flag.....“0”
- Interrupt disable request bit .....“1”
- Interrupt enable bit.....“1”

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 9 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Serial I/O reception	4	FFF716	FFF616	At completion of serial interface data reception	Valid when serial interface is selected
Serial I/O transmission	5	FFF516	FFF416	At completion of serial interface transmit shift or when transmission buffer is empty	Valid when serial interface is selected
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 2	8	FFEF16	FFEE16	At timer 2 underflow	
Timer 3	9	FFED16	FFEC16	At timer 3 underflow	
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Timer 1	12	FFE716	FFE616	At timer 1 underflow	
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
Key input (Key-on wake-up)	15	FFE116	FFE016	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (Valid at falling)
ADT	16	FFDF16	FFDE16	At falling of ADT input	Valid when ADT interrupt is selected, External interrupt (Valid at falling)
A/D conversion				At completion of A/D conversion	Valid when A/D interrupt is selected
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

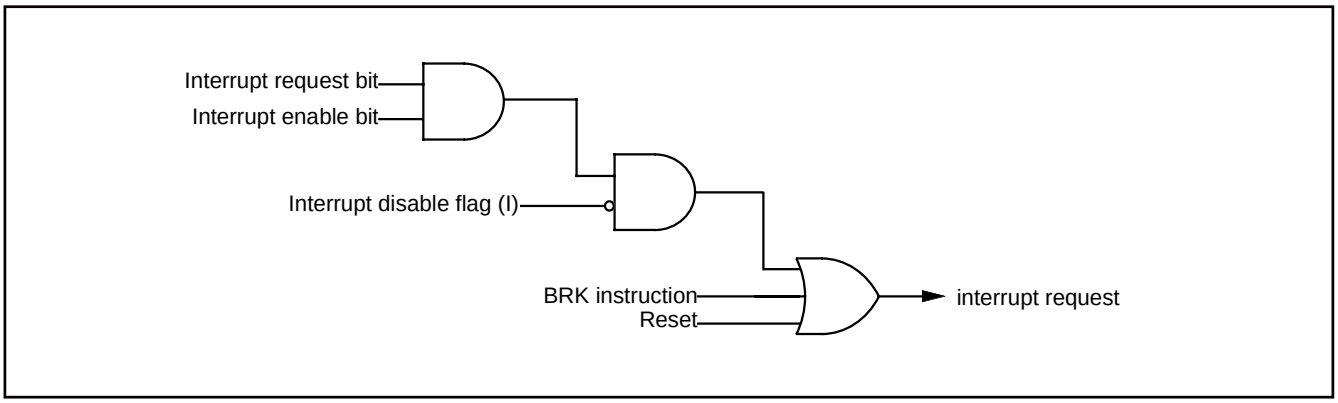


Fig. 16 Interrupt control diagram

Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to “1”, the acceptance of interrupt requests is disabled. When it is set to “0”, acceptance of interrupt requests is enabled. This flag is set to “1” with the SET instruction and set to “0” with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remaines set to “0”. Subsequently, this flag is automatically set to “1” and multiple interrupts are disabled.

To use multiple interrupts, set this flag to “0” with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to “1” and remaines “1” until the request is accepted. When the request is accepted, this bit is automatically set to “0”.

Each interrupt request bit can be set to “0”, but cannot be set to “1”, by software.

Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to “0”, the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to “1”, but the interrupt request is not accepted. When an interrupt enable bit is set to “1”, acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to “0” or “1” by software.

The interrupt enable bit for an unused interrupt should be set to “0”.

Interrupt Source Selection

The following combinations can be selected by the interrupt source selection bit of the AD control register (bit 6 of the address 0039_{16}).

- ADT or A/D conversion (refer Table 9)

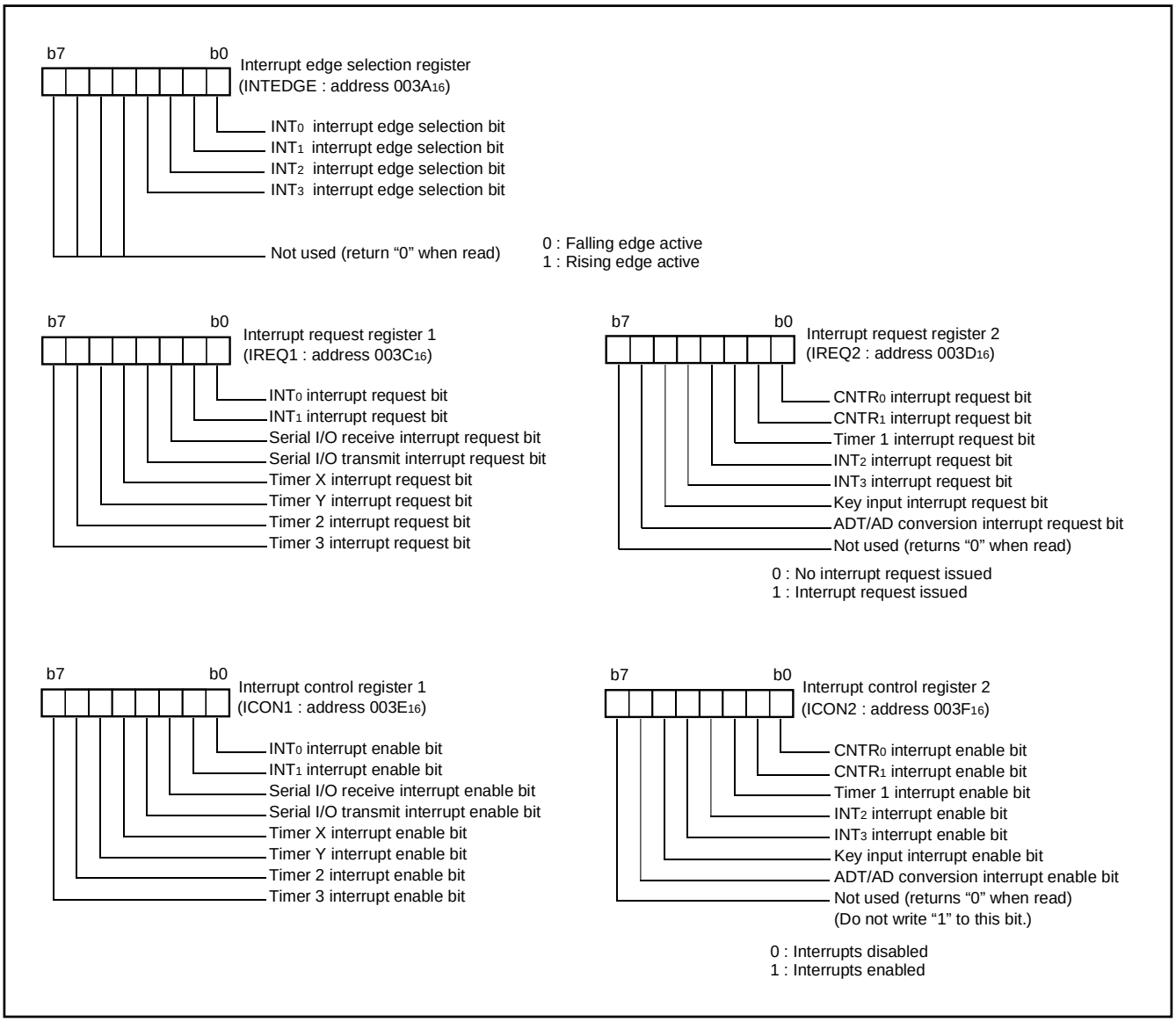


Fig. 17 Structure of interrupt-related registers

Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to “1”.

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Figure 18 shows the time up to execution in the interrupt processing routine, and Figure 19 shows the interrupt sequence.
Figure 20 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.
(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
  1. High-order bits of program counter (PCH)
  2. Low-order bits of program counter (PCL)
  3. Processor status register (PS)
(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.
(4) The interrupt request bit for the corresponding interrupt is set to “0”. Also, the interrupt disable flag is set to “1” and multiple interrupts are disabled.
(5) The interrupt routine is executed.
(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

■Notes

The interrupt request bit may be set to “1” in the following cases.
•When setting the external interrupt active edge
Related registers: Interrupt edge selection register (address 003A16)
Timer X mode register (address 002716)
Timer Y mode register (address 002816)

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.
(1) Set the corresponding enable bit to “0” (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to “0” after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to “1” (enabled).

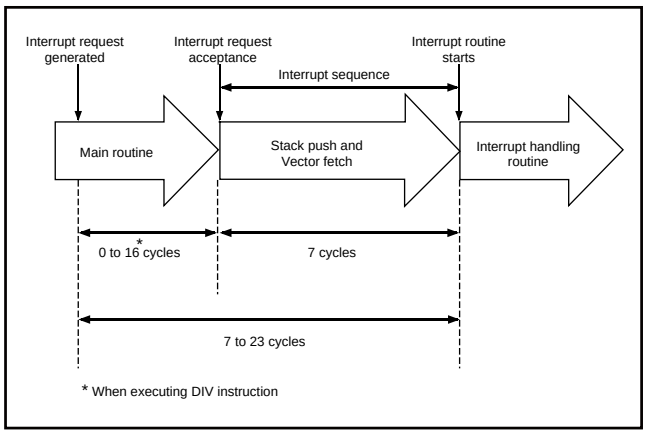


Fig. 18 Time up to execution in interrupt routine

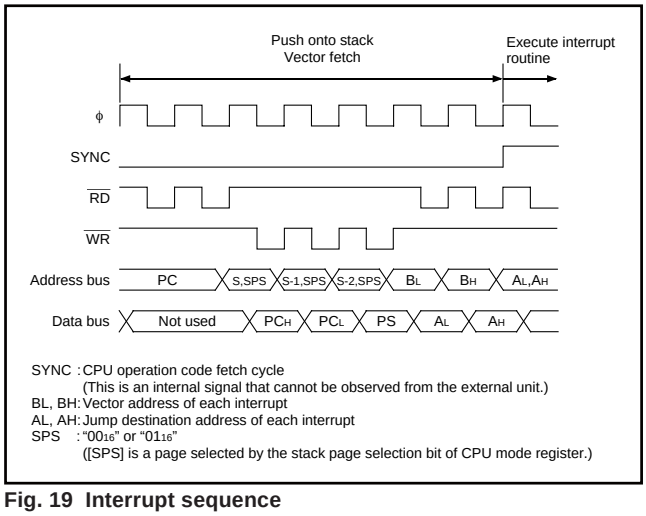
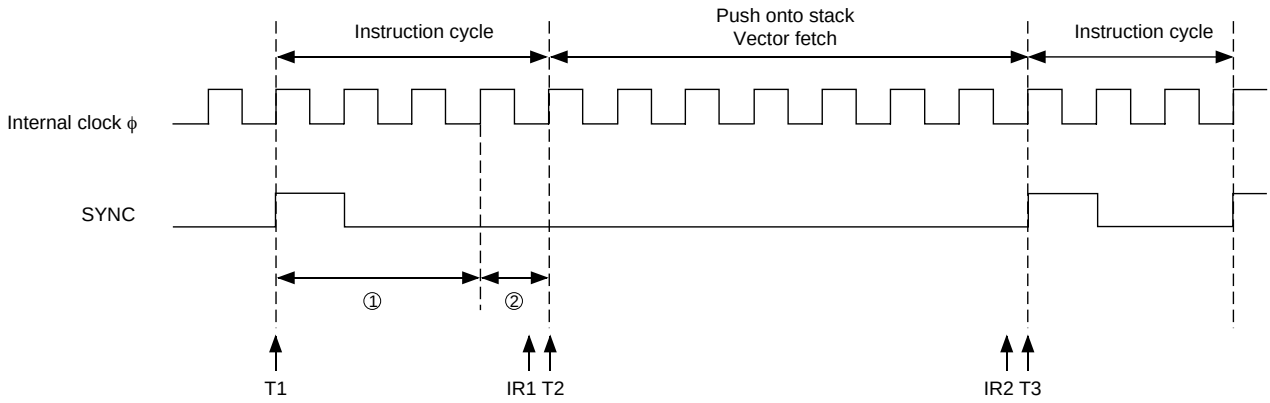


Fig. 19 Interrupt sequence



T1 T2 T3: Interrupt acceptance timing points
IR1 IR2: Timings points at which the interrupt request bit is set to “1”.

Note: Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to “1” at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to “1” at timing point IR1 or IR2. The timing point at which the bit is set to “1” varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to “1” at timing point IR1 or IR2 separately.

Fig. 20 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

Key Input Interrupt (Key-on wake-up)

A Key-on wake-up interrupt request is generated by applying a falling edge to any pin of port P2 that have been set to input mode. In other words, it is gener1ated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports $P2_0$–$P2_3$.

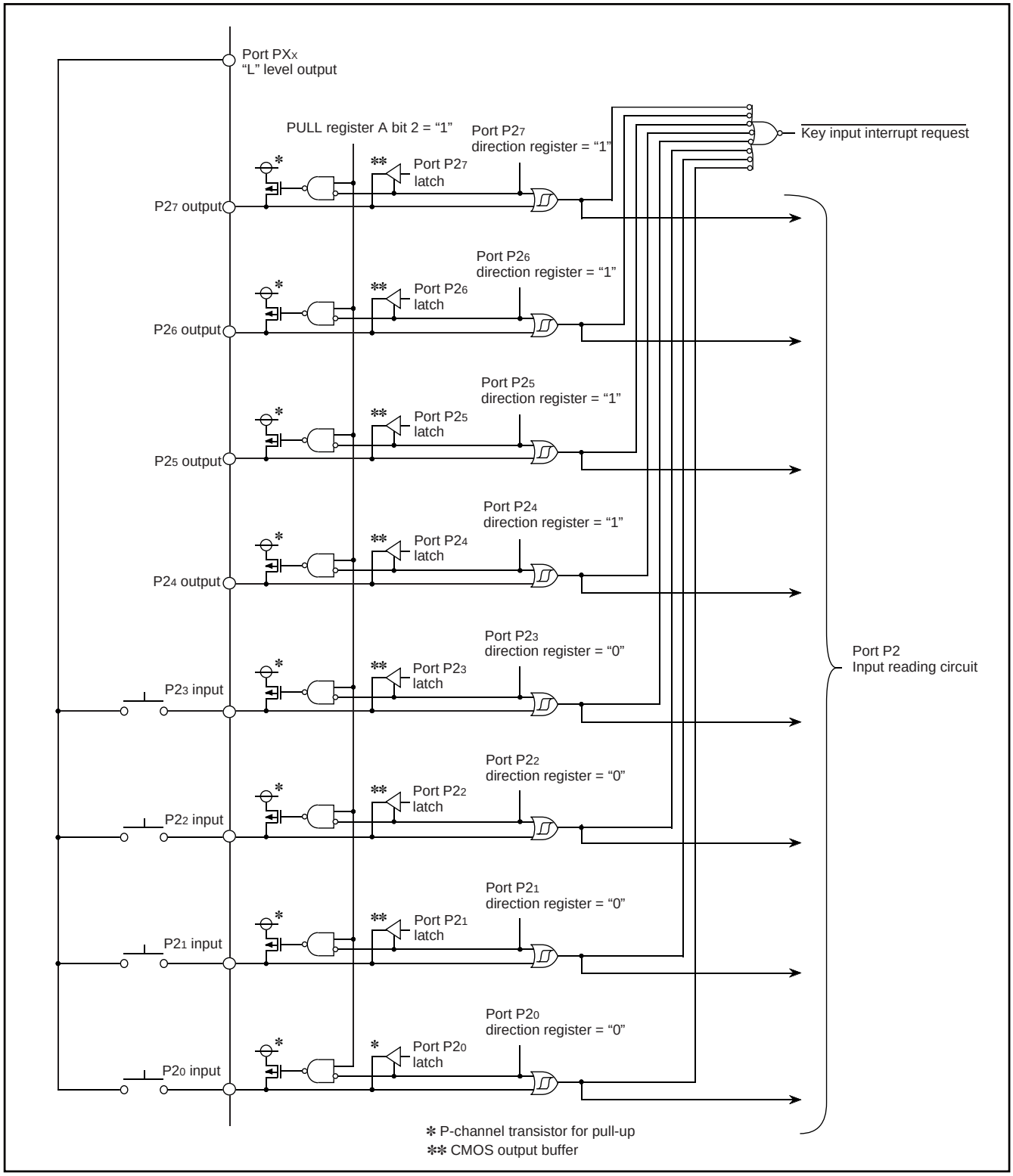


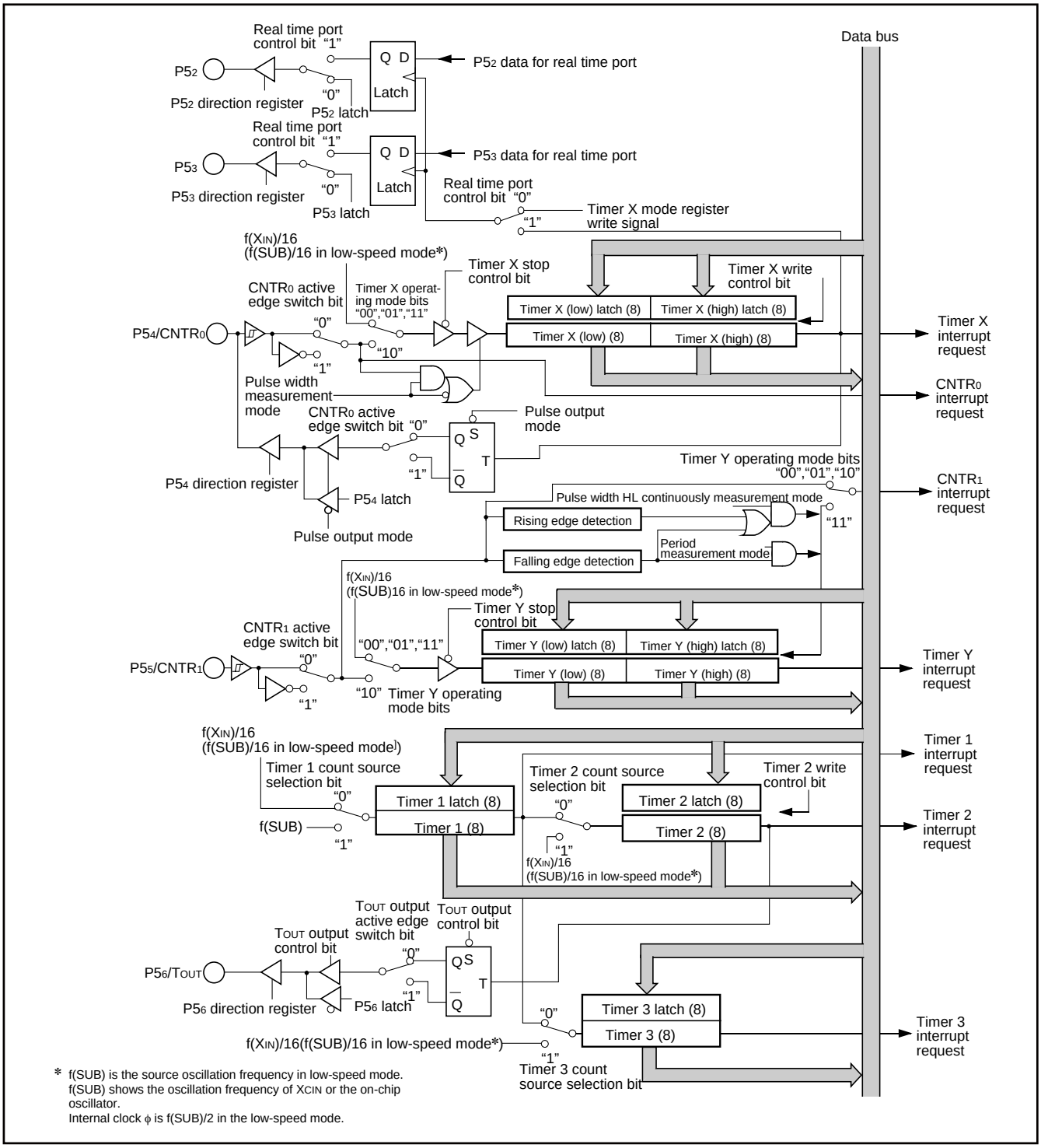
Fig. 21 Connection example when using key input interrupt and port P2 block diagram

TIMERS

The 3823 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.



* f(SUB) is the source oscillation frequency in low-speed mode.
f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.
Internal clock ϕ is f(SUB)/2 in the low-speed mode.

Fig. 22 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer Mode

The timer counts f(XIN)/16 (or f(SUB)/16 in low-speed mode).
f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(XCIN)/2 in the low-speed mode.

(2) Pulse Output Mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR0 pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

(4) Pulse Width Measurement Mode

The count source is f(XIN)/16 (or f(SUB)/16 in low-speed mode). If CNTR0 active edge switch bit is “0”, the timer counts while the input signal of CNTR0 pin is at “H”. If it is “1”, the timer counts while the input signal of CNTR0 pin is at “L”. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

●Timer X write control

If the timer X write control bit is “0”, when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is “1”, when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, when writing in the timer latch at the timer underflow, the value is set in the timer and the latch at one time. Additionally, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

●Real time port control

While the real time port function is valid, data for the real time port are output from ports P52 and P53 each time the timer X underflows. (However, after rewriting a data for real time port, if the real time port control bit is changed from “0” to “1”, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

■Note on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

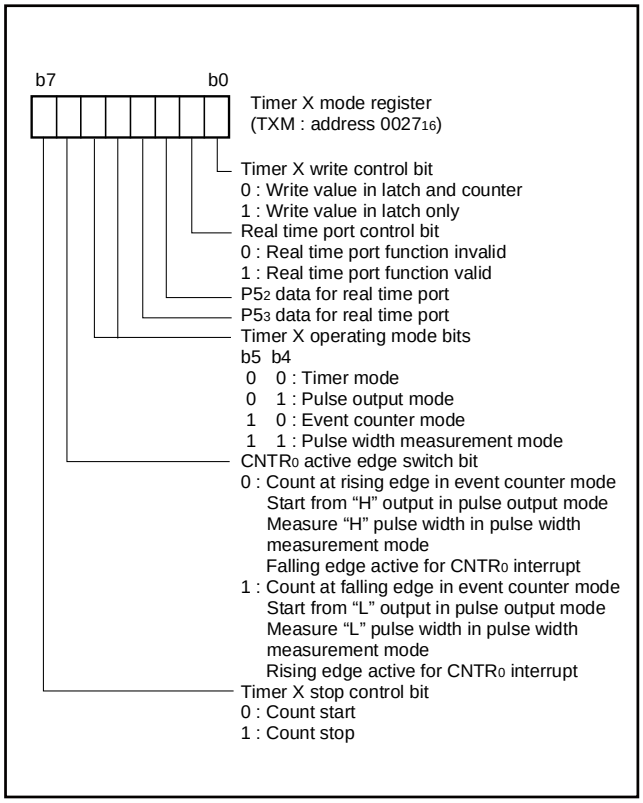


Fig. 23 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer Mode

The timer counts f(XIN)/16 (or f(SUB)/16 in low-speed mode).

(2) Period Measurement Mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(4) Pulse Width HL Continuously Measurement Mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

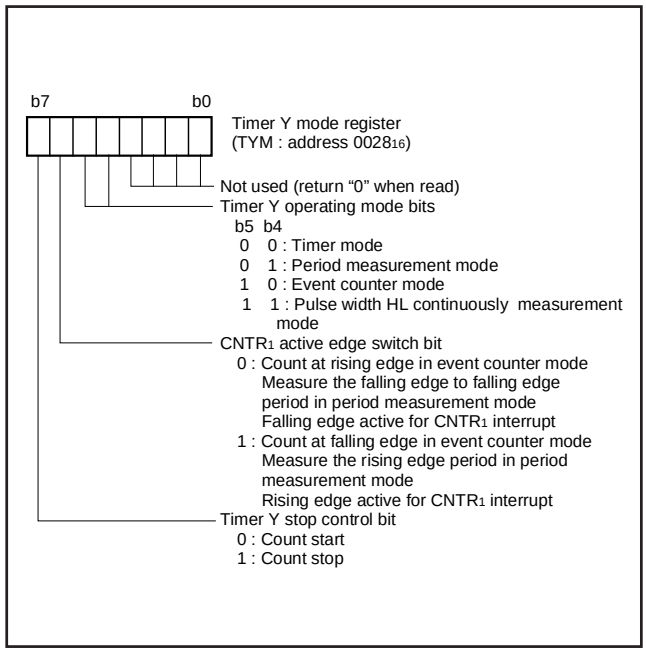


Fig. 24 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer, rewrite the value of timer whenever the count source is changed.

●Timer 2 write control

If the timer 2 write control bit is “0”, when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is “1”, when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 output control

When the timer 2 (TOUT) is output enabled, an inversion signal from the TOUT pin is output each time timer 2 underflows.

In this case, set the port shared with the TOUT pin to the output mode.

■Notes on timer 1 to timer 3

When the count source of timer 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer . If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

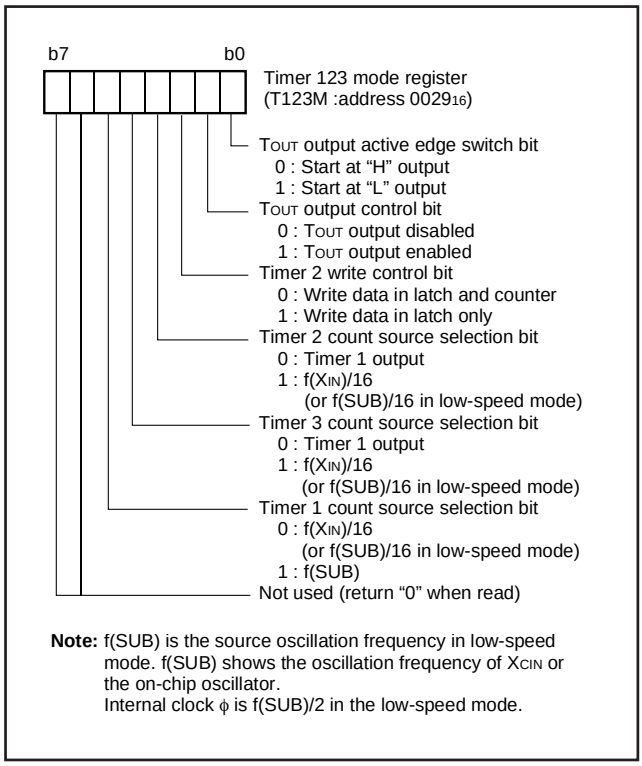


Fig. 25 Structure of timer 123 mode register

SERIAL INTERFACE
Serial I/O

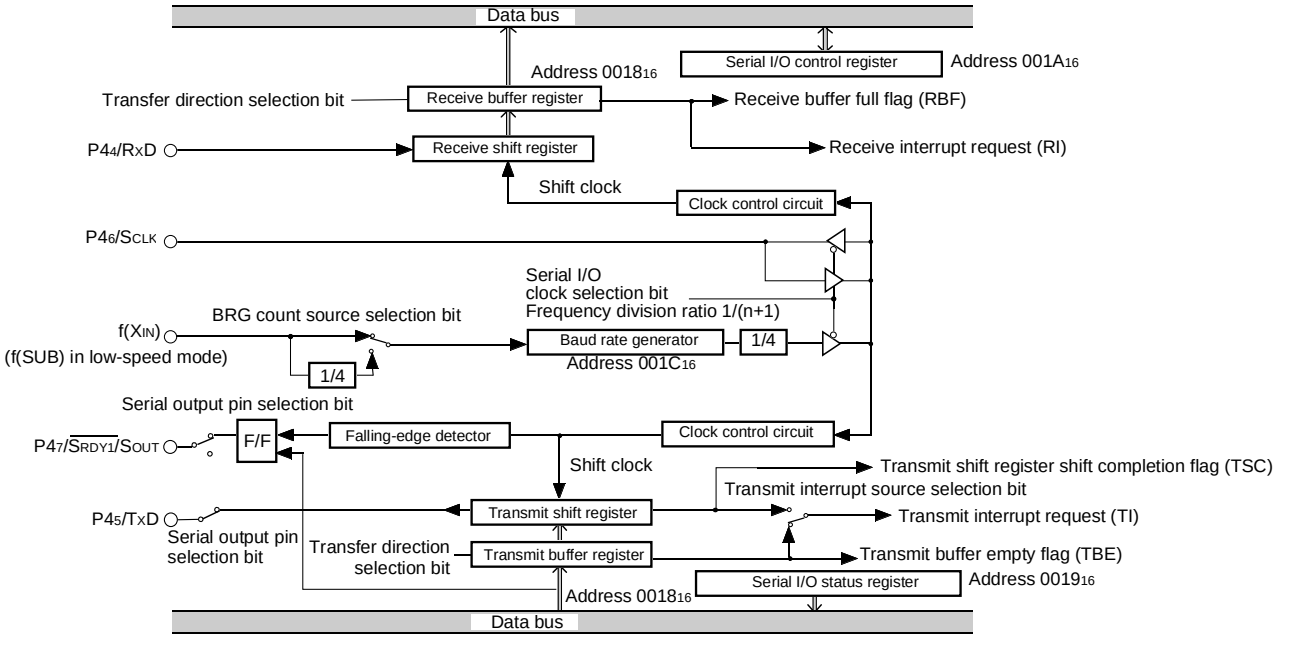
Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O can be selected by setting the mode selection bit of the serial I/O control register to “1”.

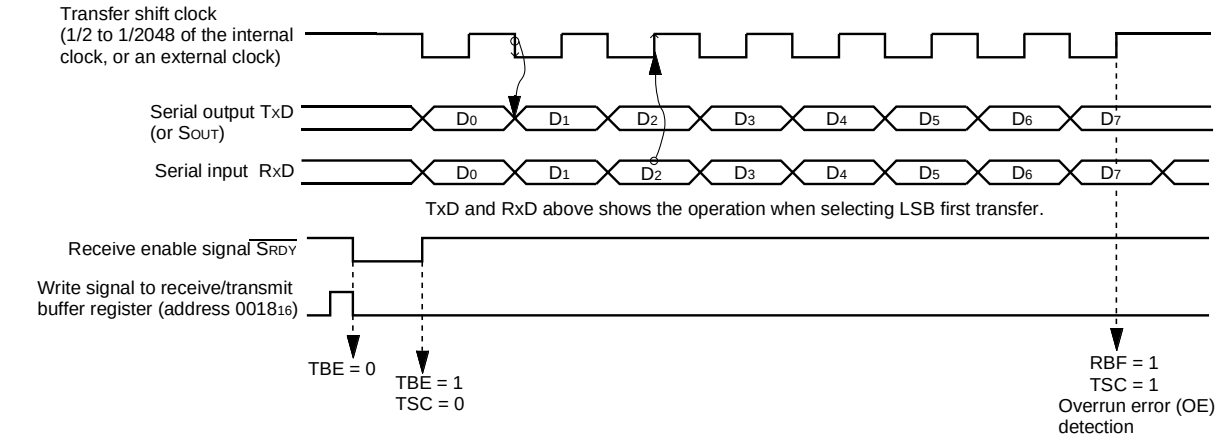
For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

The MSB first transfer is selected as the transfer direction by setting the bit 0 in the peripheral function expansion register to “1”. Also, the synchronous serial I/O output switches to the P47/SRDY/SOUT pin by setting the bit 1 in the peripheral function expansion register to “1”.



Note: f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.

Fig. 26 Block diagram of clock synchronous serial I/O



Notes
1 : The transmit interrupt (TI) can be generated either when the transmit buffer register has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 27 Operation of clock synchronous serial I/O function

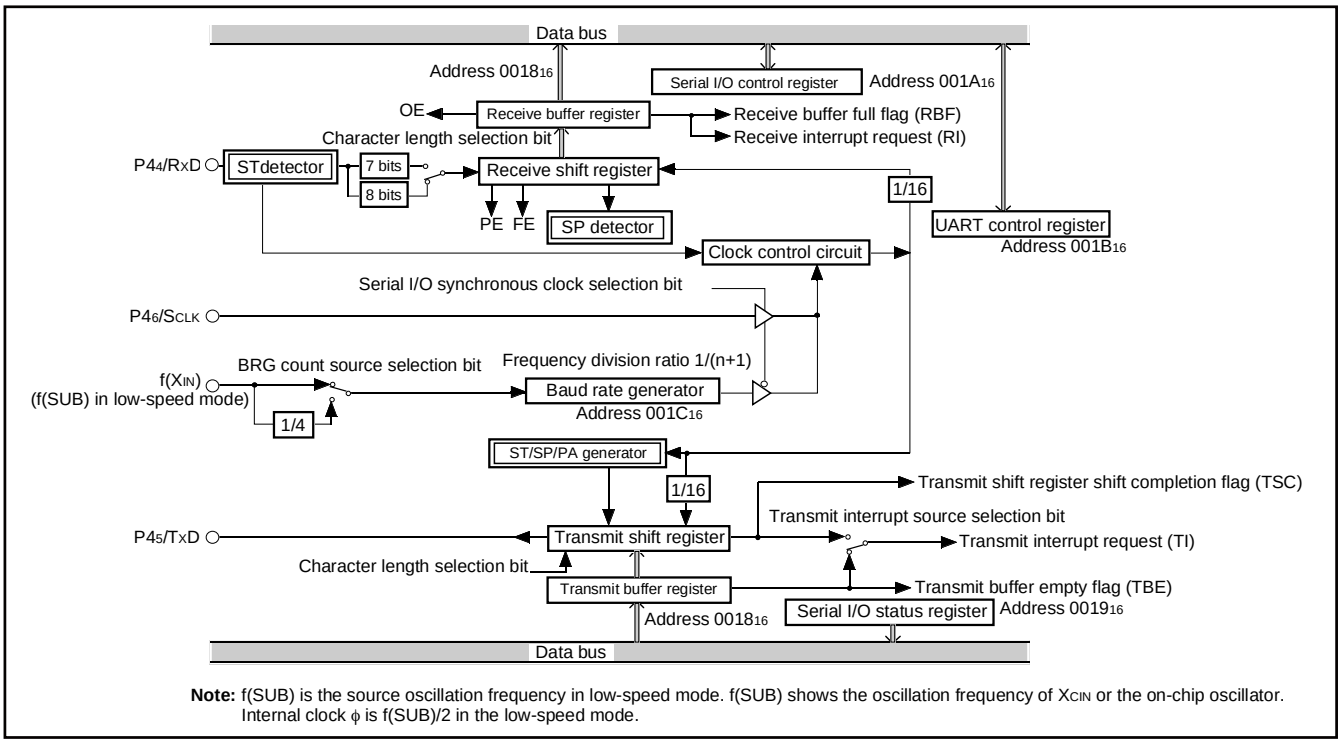
(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

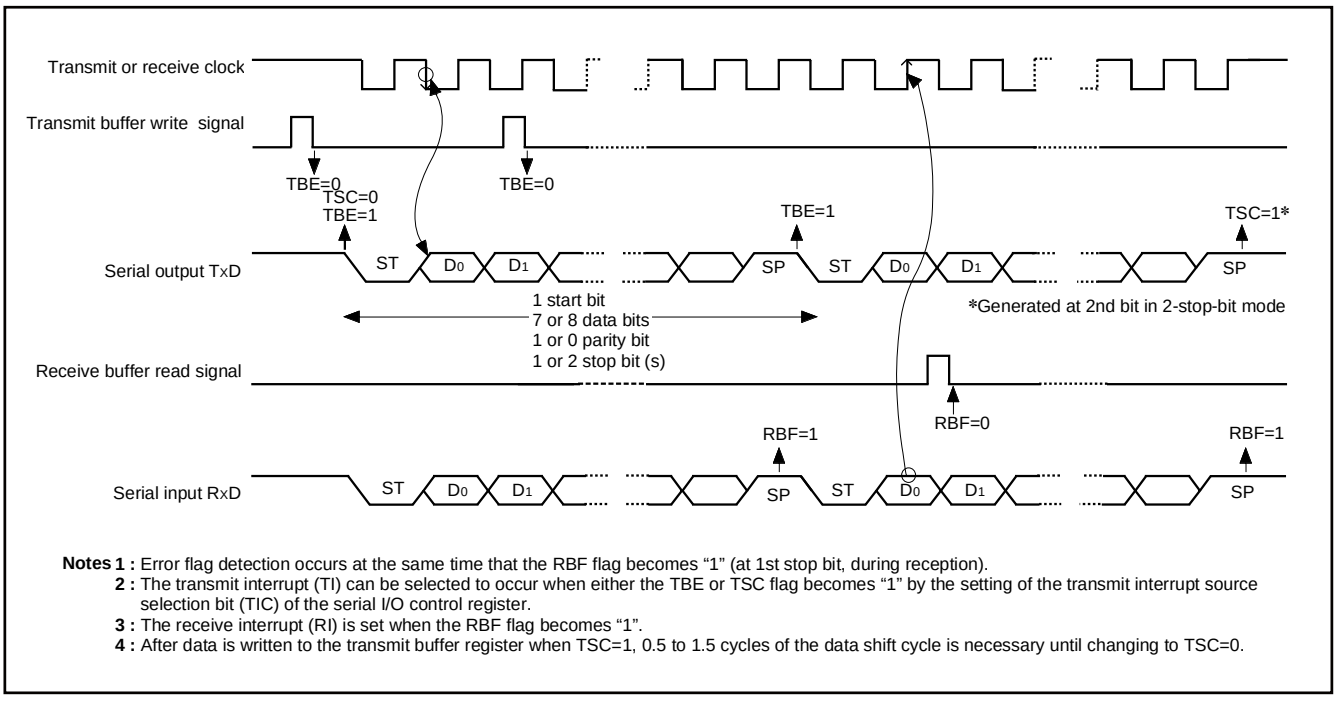
The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.



Note: f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(SUB)/2 in the low-speed mode.

Fig. 28 Block diagram of UART serial I/O

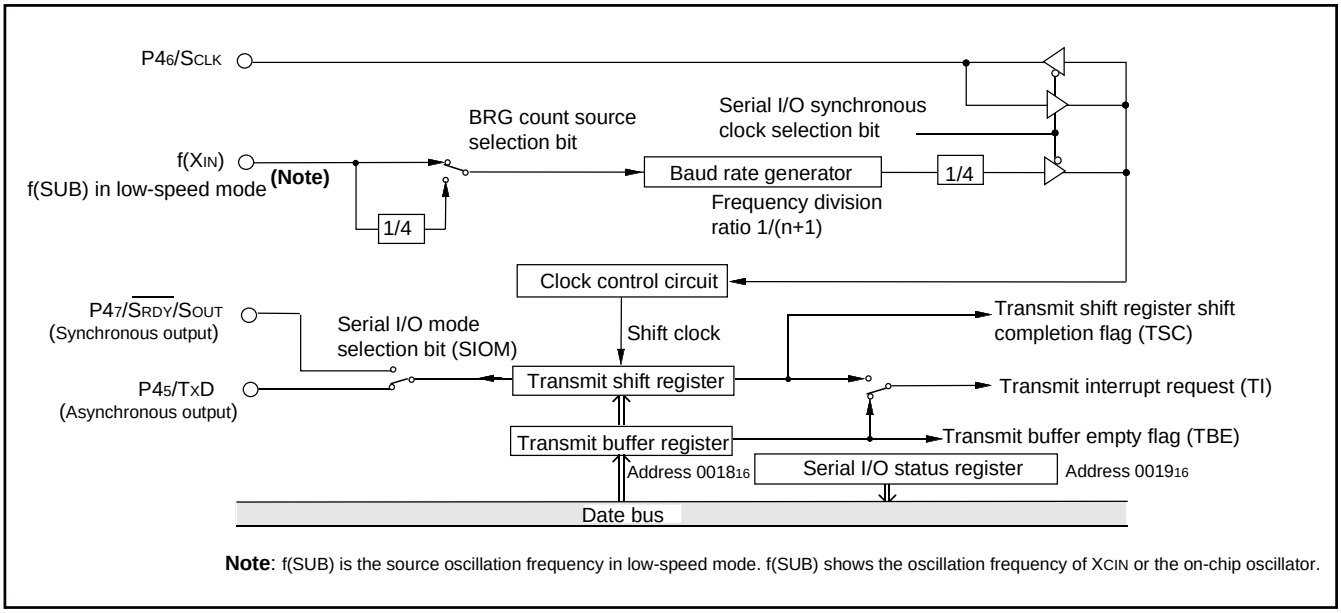


Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes “1” by the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes “1”.
4 : After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 29 Operation of UART serial I/O function

(3) Synchronous/Asynchronous Alternate Transmit Mode

Synchronous/asynchronous alternate transmit mode is selected by setting the transmit enable bit in the serial I/O control register to "1" after setting the synchronous serial I/O output pin selection bit in the peripheral function expansion register to "1". Set the synchronous serial I/O output pin selection bit to "1" when the serial I/O mode selection bit is set to "0". In this mode, transmit cannot be performed continuously. Write to the transmit buffer register after confirming that the transmit shift register is set to "1", and then changing the serial I/O mode selection bit. The $\overline{SRDY}$ output function cannot be used when the clock synchronous serial I/O is selected. Also, when using the internal clock for the transfer clock (the serial I/O synchronous clock selection bit is set to "0"), apply "H" output to the P46 pin. The other operation is the same as clock synchronous serial I/O mode and asynchronous serial I/O mode (UART).



Note: f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.

Fig. 30 Block diagram of synchronous/asynchronous alternate transmit

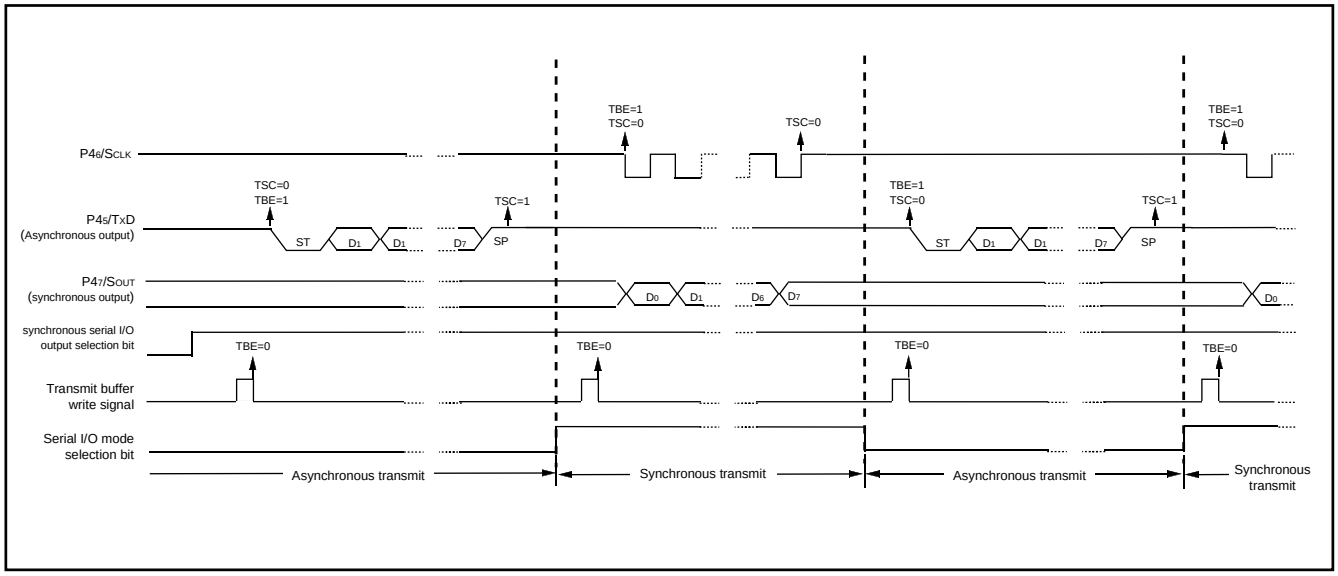


Fig. 31 Operation of synchronous/asynchronous alternate transmit function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing “0” to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)]001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4$_5$/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

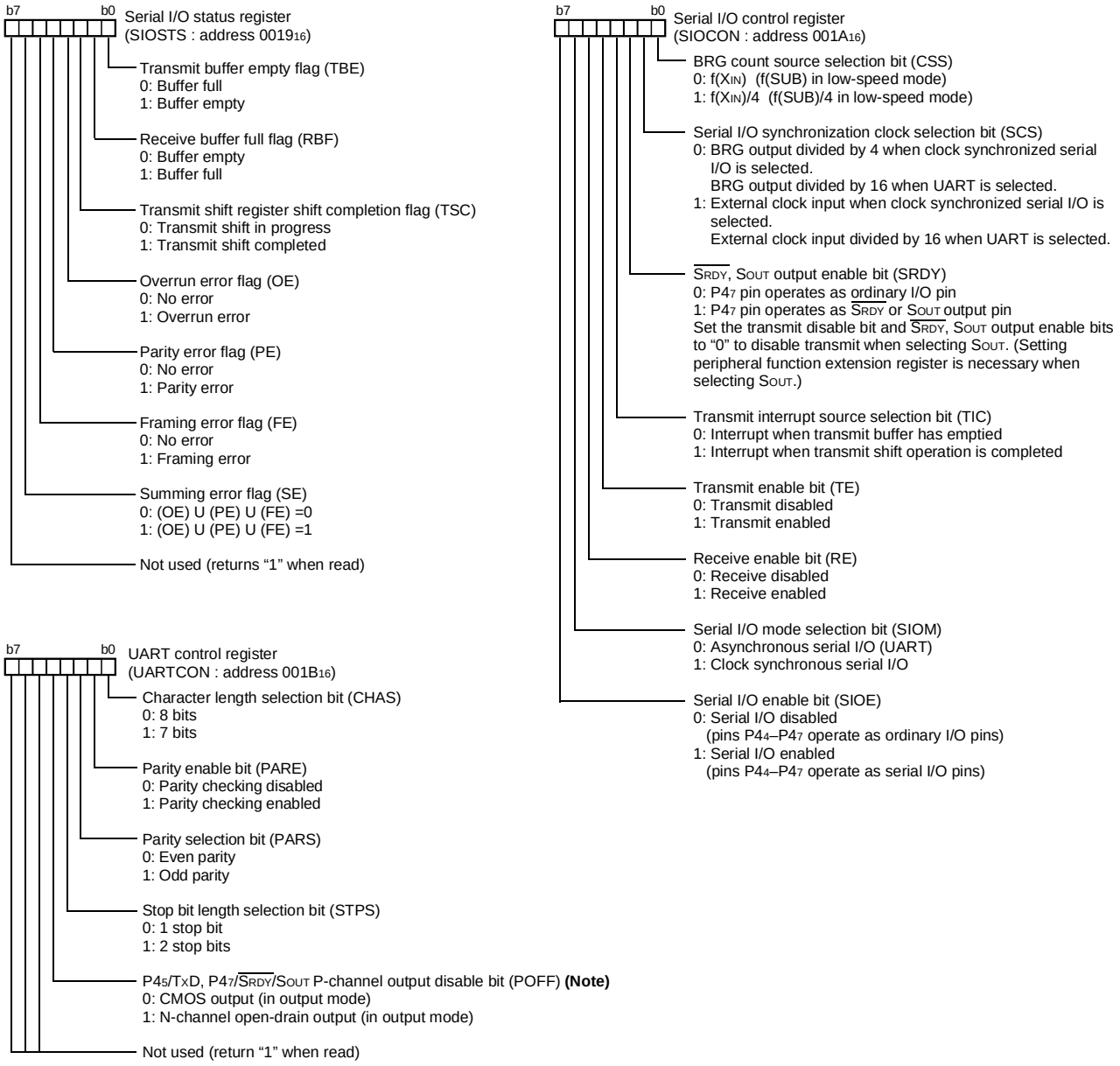
The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.

①Set the serial I/O transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O transmit interrupt enable bit to “1” (enabled).



Notes 1 : The peripheral function extension register is used to choose P45/TxD, P47/SRDY/SOUT.
2 : f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.

Fig. 32 Structure of serial I/O control registers

A/D CONVERTER

[AD Conversion Register (ADH, ADL)] 0035$_{16}$

The AD conversion register is a read-only register that contains the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.The high-order 8 bits of a conversion result is stored in the AD conversion high-order register (address 0035$_{16}$),and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the AD conversion low-order register (address 0036$_{16}$).

The bit 0 in the AD conversion low-order register is used as the conversion mode selection bit. 8-bit A/D mode is selected by setting this bit to “0” and 10-bit A/D mode is selected by setting it to “1”.

[AD Control Register (ADCON)] 0034$_{16}$

The AD control register controls the A/D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A/D conversion. The value of this bit remains at “0” during an A/D conversion, then changes to “1” when the A/D conversion is completed. Writing “0” to this bit starts the A/D conversion. Bit 4 is the V_{REF} input switch bit which controls connection of the resistor ladder and the reference voltage input pin (V_{REF}). The resistor ladder is always connected to V_{REF} when bit 4 is set to "1". When bit 4 is set to “0”, the resistor ladder is cut off from V_{REF} except for A/D conversion performed. When bit 5, which is the AD external trigger valid bit, is set to “1”, this bit enables A/D conversion even by a falling edge of an ADT input. Set the P5$_7$/ADT pin to input mode (set "0" to bit 7 of port P5 direction register) when using an A/D external trigger.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF}, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports P6$_7$/AN$_7$–P6$_0$/AN$_0$, and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the AD conversion register. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”.

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough. Accordingly, set f(X_{IN}) to at least 500kHz during A/D conversion in the middle-or high-speed mode. Also, do not execute the STP or WIT instruction during an A/D conversion.

In the low-speed mode, since the A/D conversion is executed by the built-in self-oscillation circuit, the minimum value of f(X_{IN}) frequency is not limited.

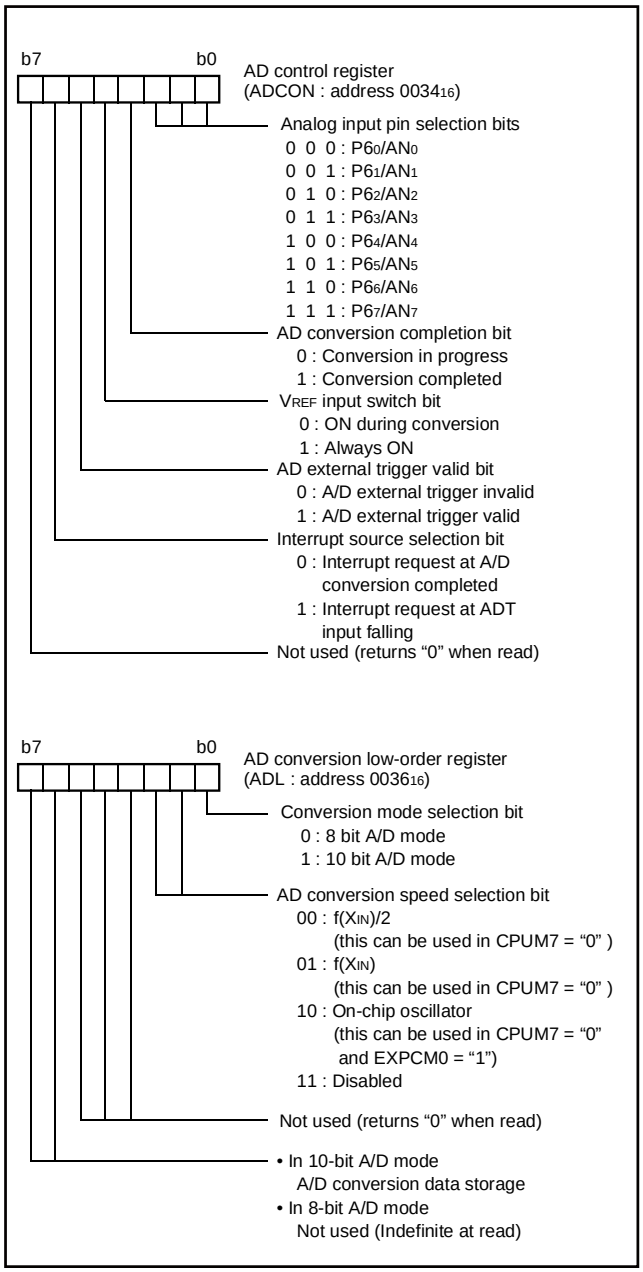
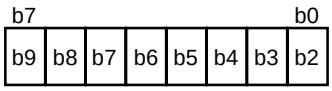


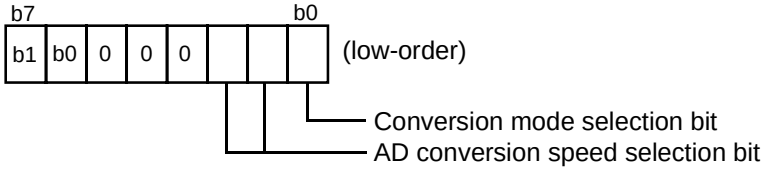
Fig. 33 Structure of AD conversion-related registers

• 10 bit reading (Read address 0035$_{16}$ before 0036$_{16}$)

AD conversion high-order register (Address 0035$_{16}$) ADH



AD conversion low-order register (Address 0036$_{16}$) ADL



Note: The bit 5 to bit 3 of address 0036$_{16}$ become "0" at reading.

• 8 bit reading (Read only address 0035$_{16}$)

(Address 0035$_{16}$)

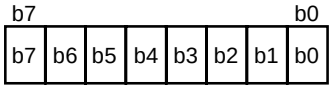


Fig. 34 A/D conversion register reading

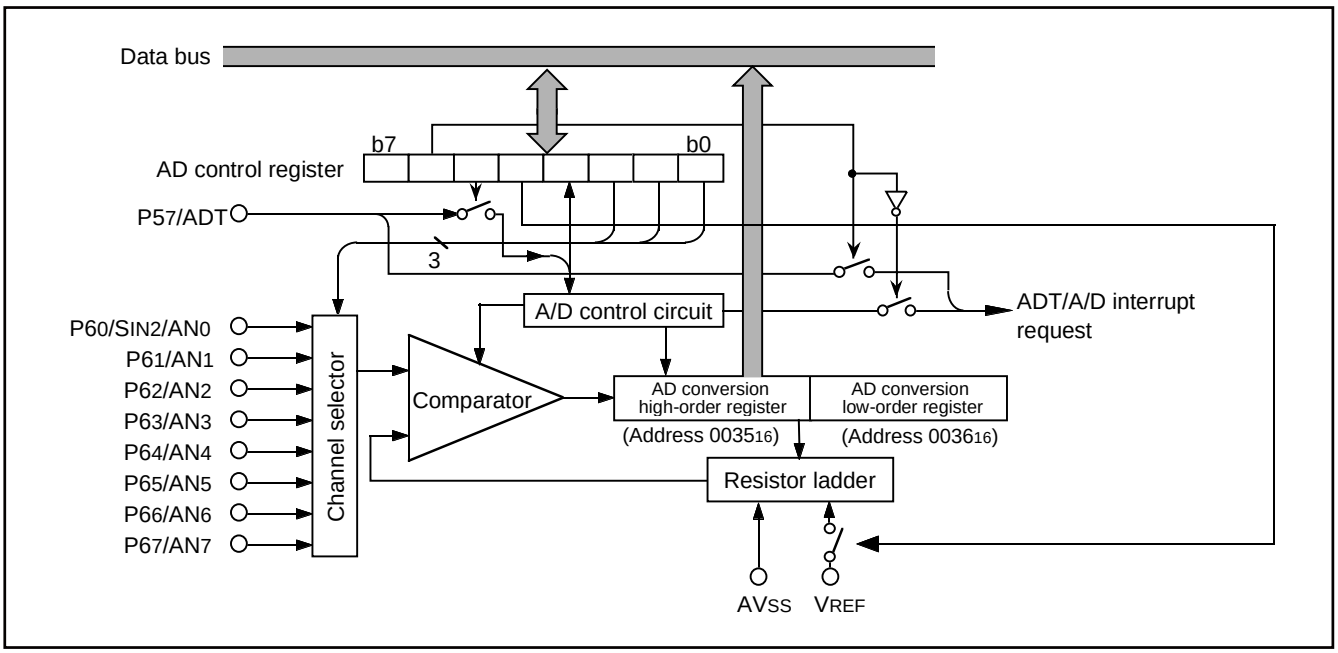


Fig. 35 A/D converter block diagram

LCD DRIVE CONTROL CIRCUIT

The 3823 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

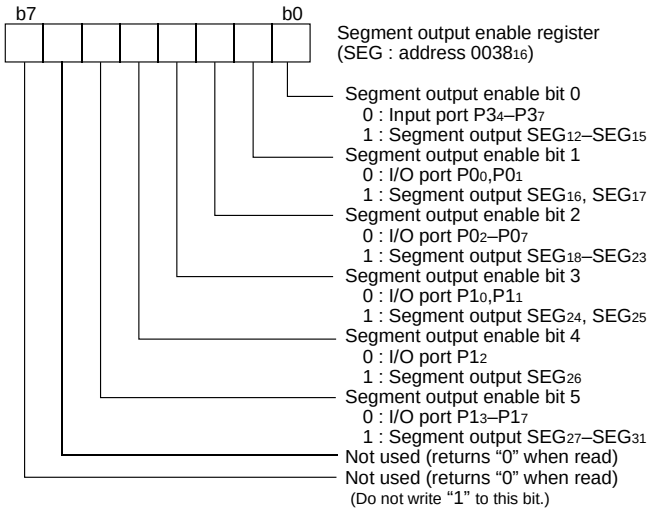
- LCD display RAM
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

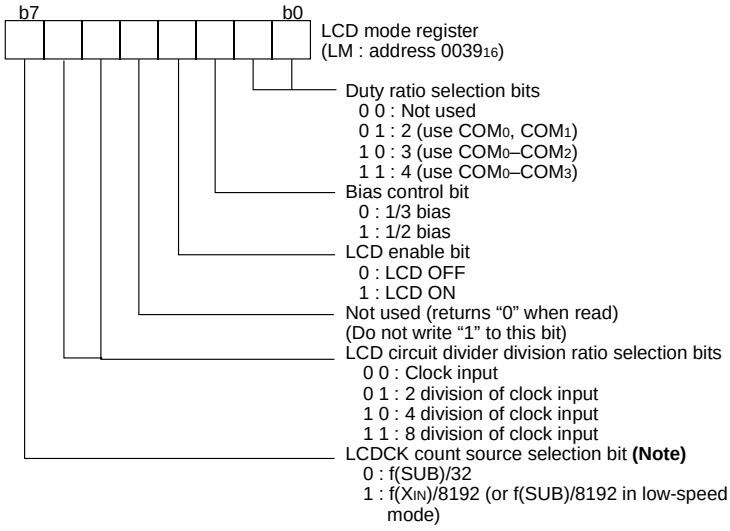
A maximum of 32 segment output pins and 4 common output pins can be used.

Up to 128 pixels can be controlled for LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 10 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
2	64 dots or 8 segment LCD 8 digits
3	96 dots or 8 segment LCD 12 digits
4	128 dots or 8 segment LCD 16 digits





Note: LCDCK is a clock for a LCD timing controller.
f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator.
Internal clock ϕ is f(SUB)/2 in the low-speed mode.

Fig. 36 Structure of segment output enable register and LCD mode register

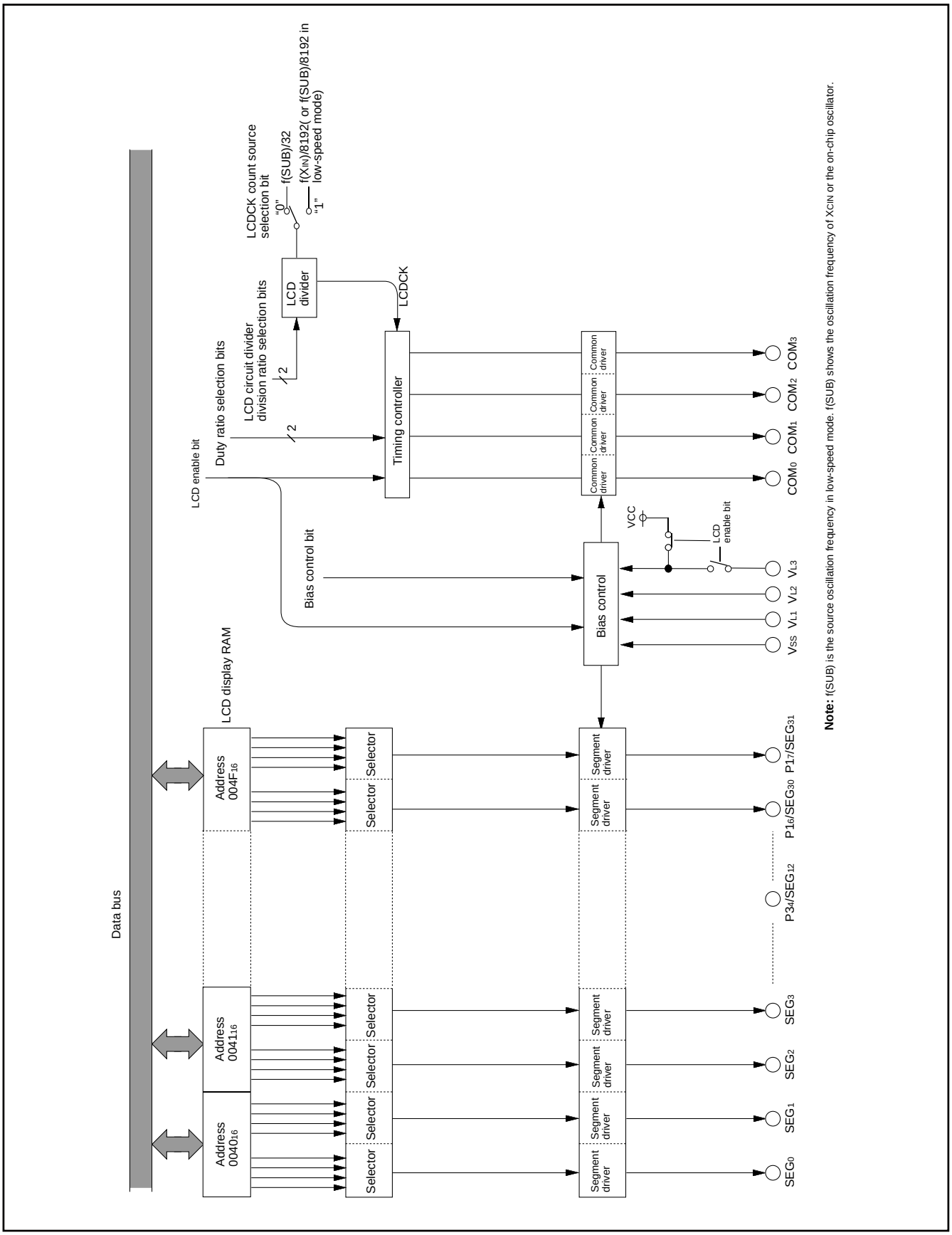


Fig. 37 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 11 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

Table 11 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note 1: V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Table 12 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
2	0	1	COM_0, COM_1 **(Note 1)**
3	1	0	COM_0–COM_2 **(Note 2)**
4	1	1	COM_0–COM_3

Notes1: COM_2 and COM_3 are open.
2: COM_3 is open.

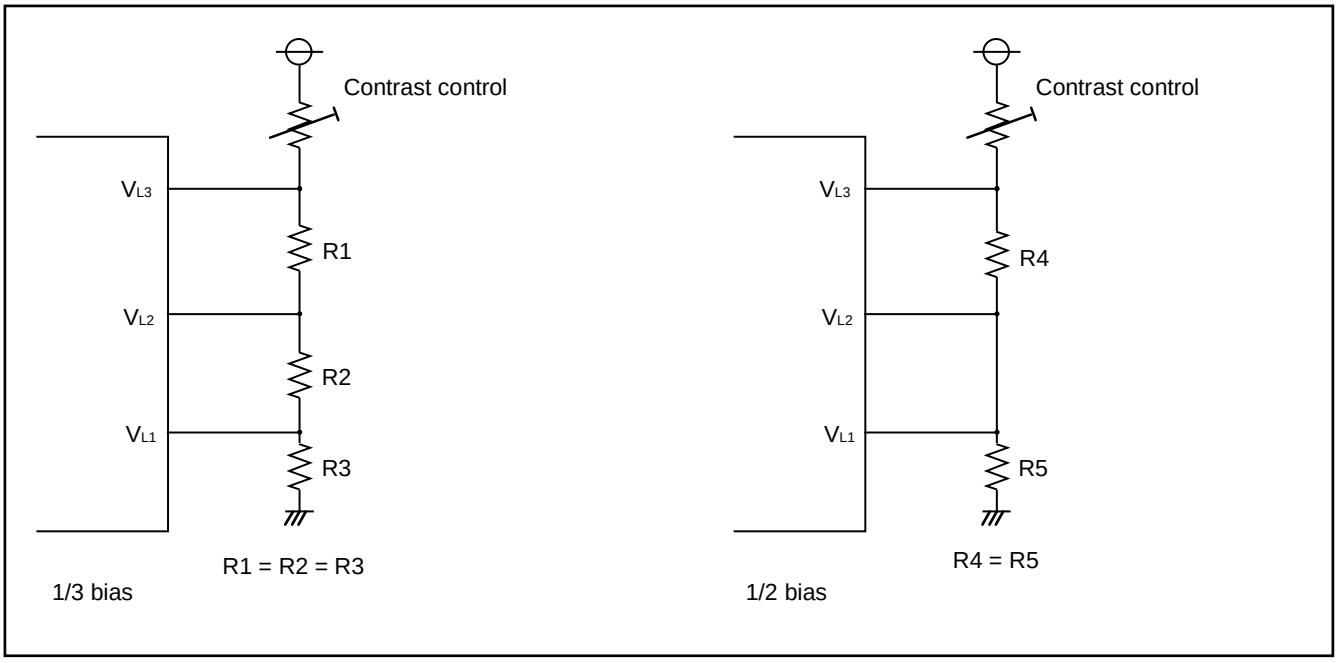


Fig. 38 Example of circuit at each bias

LCD Display RAM

Address 0040_{16} to $004F_{16}$ is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{\text{(duty ratio)}}$$

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	SEG1				SEG0			
0041_{16}	SEG3				SEG2			
0042_{16}	SEG5				SEG4			
0043_{16}	SEG7				SEG6			
0044_{16}	SEG9				SEG8			
0045_{16}	SEG11				SEG10			
0046_{16}	SEG13				SEG12			
0047_{16}	SEG15				SEG14			
0048_{16}	SEG17				SEG16			
0049_{16}	SEG19				SEG18			
$004A_{16}$	SEG21				SEG20			
$004B_{16}$	SEG23				SEG22			
$004C_{16}$	SEG25				SEG24			
$004D_{16}$	SEG27				SEG26			
$004E_{16}$	SEG29				SEG28			
$004F_{16}$	SEG31				SEG30			
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Fig. 39 LCD display RAM map

STP Instruction Execution

Execution of the STP instruction sets the LCD enable bit (bit 3 of the LCD mode register) to "0" and the LCD panel turns off.To make the LCD panel turn on after returning from the stop mode, set the LCD enable bit to "1".

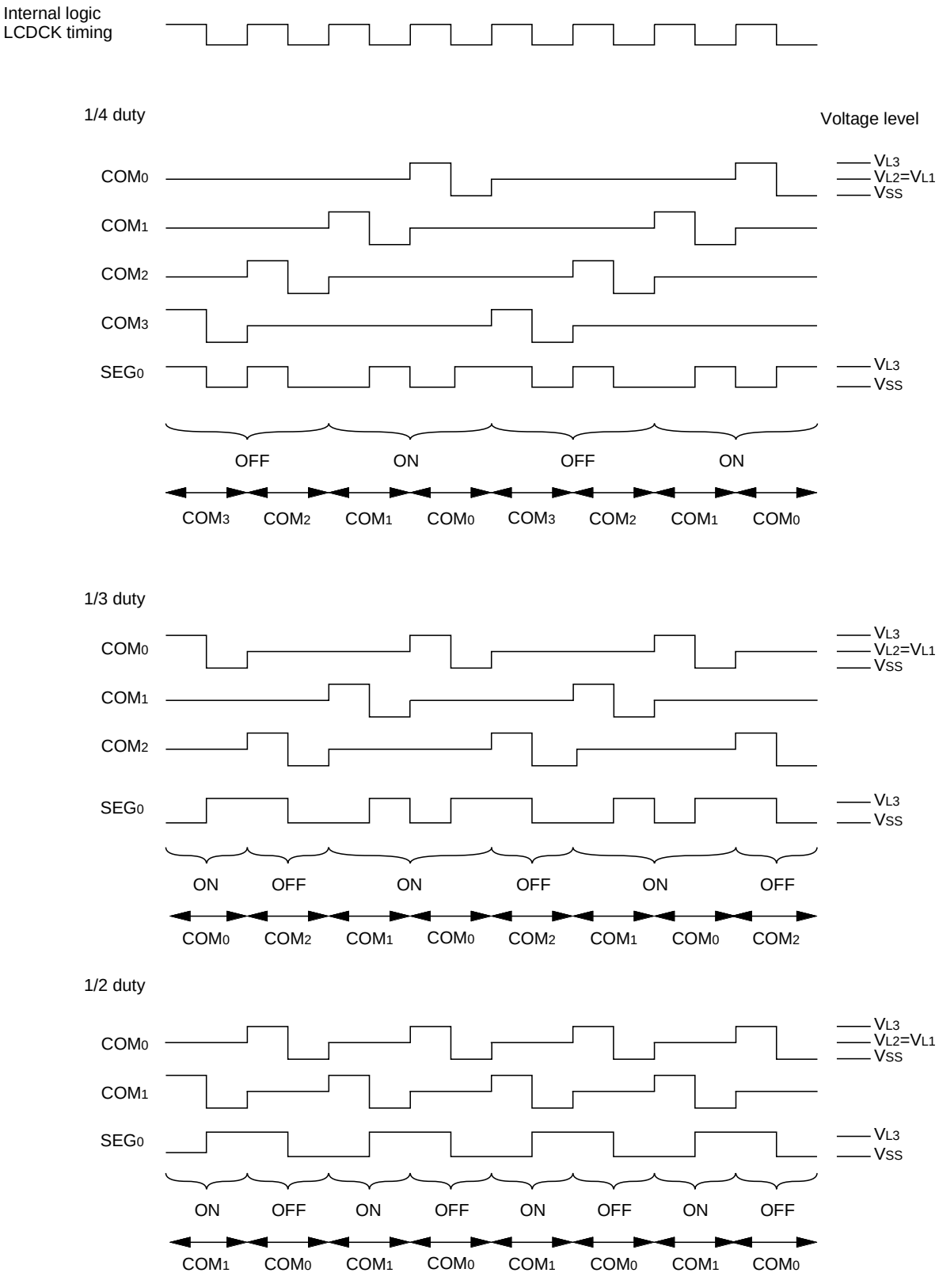


Fig. 40 LCD drive waveform (1/2 bias)

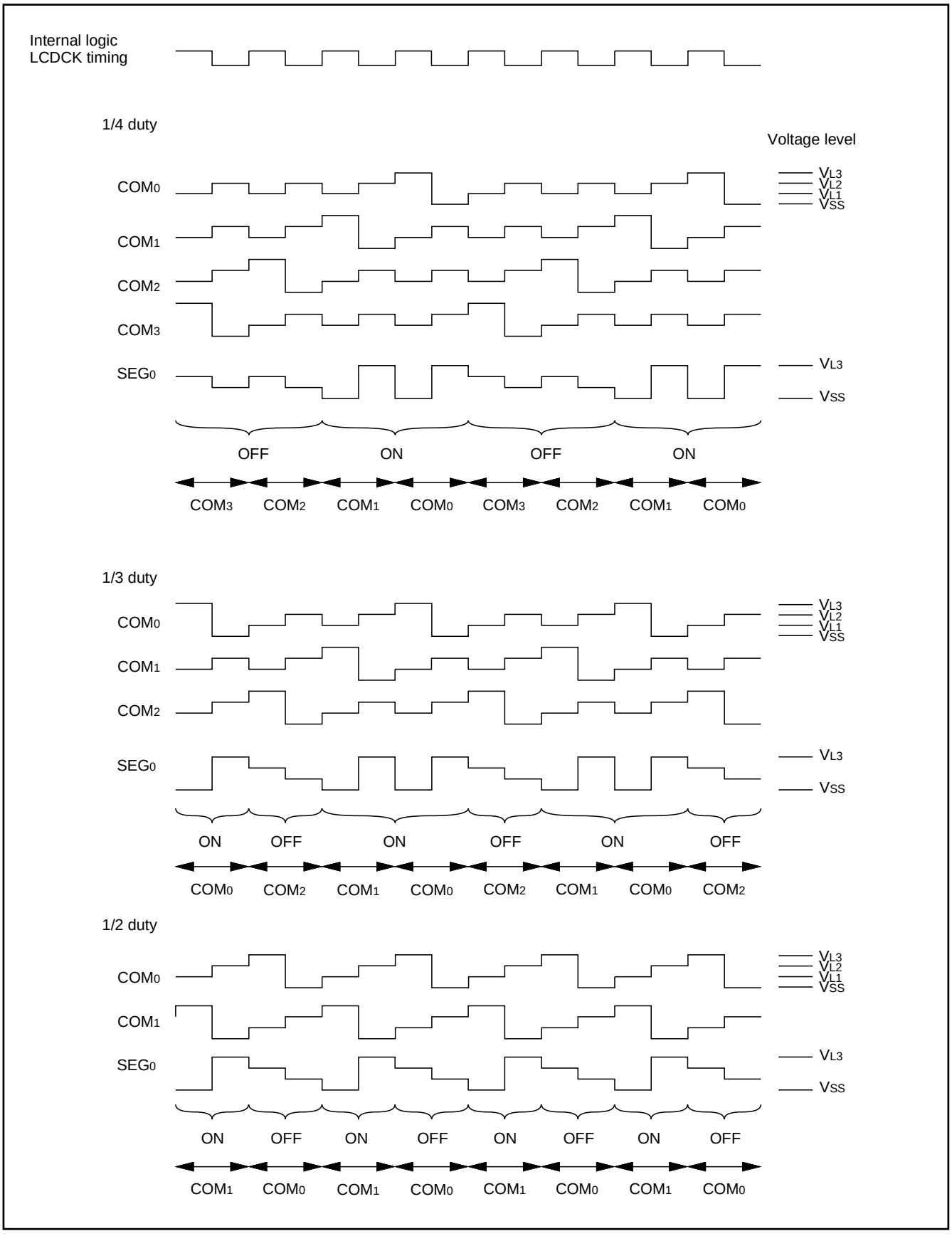


Fig. 41 LCD drive waveform (1/3 bias)

ROM CORRECTION FUNCTION

A part of program in ROM can be corrected.

Set the start address of the corrected ROM data (i.e. an Op code address of the beginning instruction) to the ROM correction address low-order and high-order registers. The program for the correction is stored in RAM for ROM correction.

When the program is being executed and the value of the program counter matches with the set address value in the the ROM correction address registers,the program is branched to the start address of RAM for ROM correction and then the correction program is executed. Use the JMP instruction (3-byte instruction) to return the main program from the correction program.

The correctable area is up to two. There are two blocks of RAM for ROM correction:

Block 1: Address $0A00_{16}$

Block 2: Address $0A20_{16}$

The ROM correction function is controlled by the ROM correction enable register.

If the ROM correction function is not used, the ROM correction vector may be used as normal RAM. When using the ROM correction vector as normal RAM, make sure to set bits 1 and 0 in the ROM correction enable register to “0” (Disable).

Notes 1: When using the ROM correction function, set the ROM correction address registers and then enable the ROM correction with the ROM correction enable register.

2: Do not set addresses other than the ROM area in the ROM correction address registers.
Do not set the same addresses in both the ROM correction address 1 registers and the ROM correction address 2 registers.

3: It is necessary to contain the process in the program to transfer the correction program from an external EEPROM and others to the RAM for ROM correction.

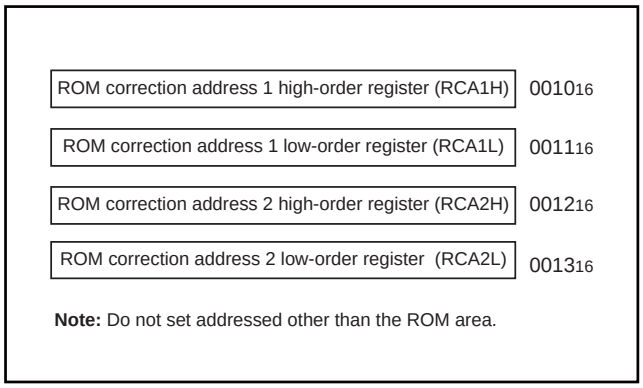


Fig. 42 ROM correction address register

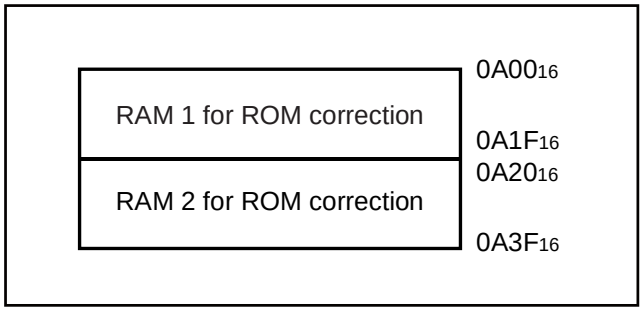


Fig. 43 RAM for ROM correction

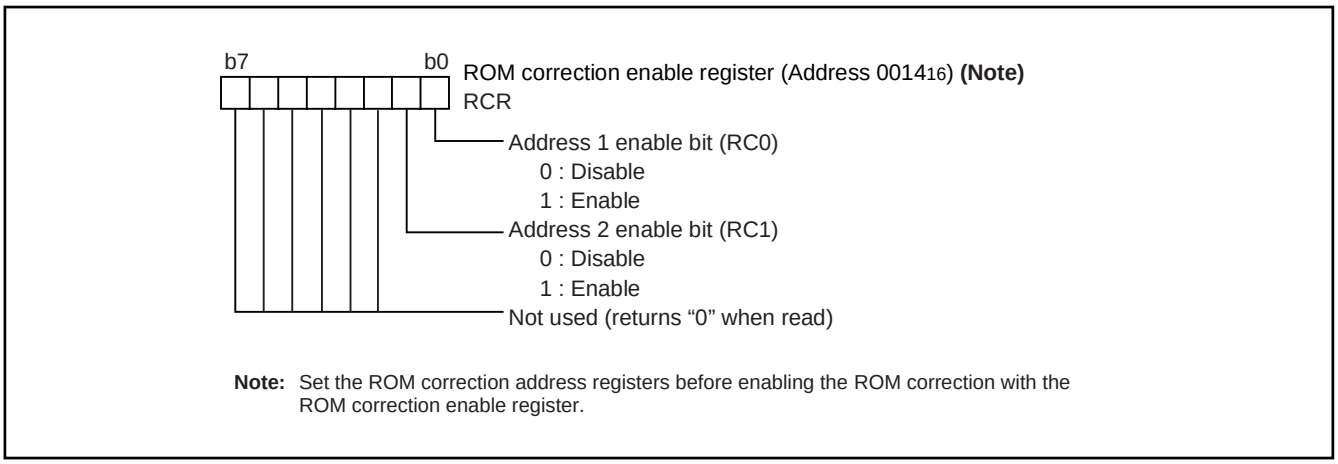


Fig. 44 Structure of ROM correction enable register

φ CLOCK SYSTEM OUTPUT FUNCTION

The internal system clock φ or XCIN frequency signal can be output from port P41 by setting the φ output control register. Set bit 1 of the port P4 direction register to "1" when outputting φ clock.

Set the bit 4 in the peripheral function expansion register to "1" when the XCIN frequency signal is output.

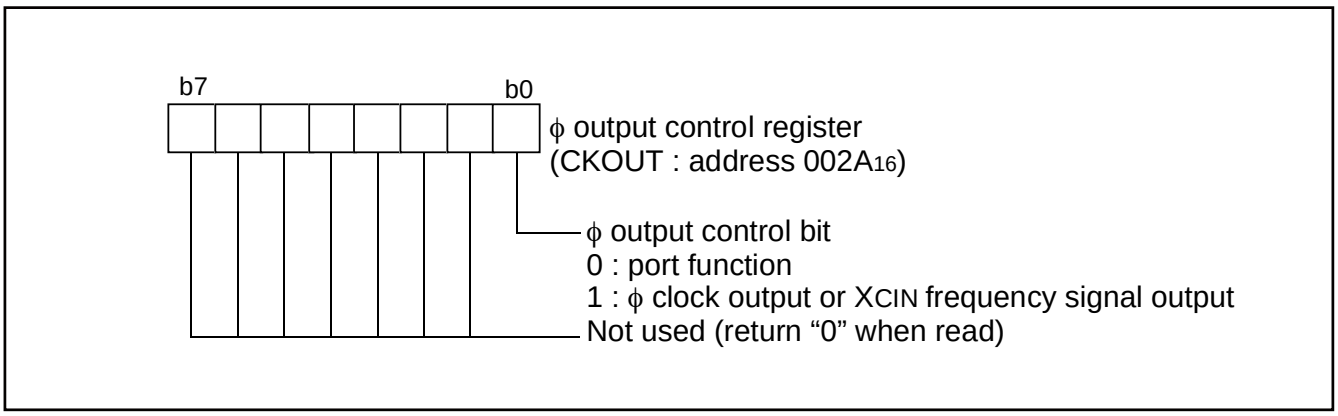


Fig. 45 Structure of φ output control register

Temporary data register

The temporary data register (addresses 002C16 to 002E16) is the 8-bit register and does not have the control function. It can be used to store data temporarily. It is initialized after reset.

RRF register

The RRF register (address 002F16)is the 8-bit register and does not have the control function. As for the value written in this register, high-order 4 bits and low-order 4 bits interchange. It is initialized after reset.

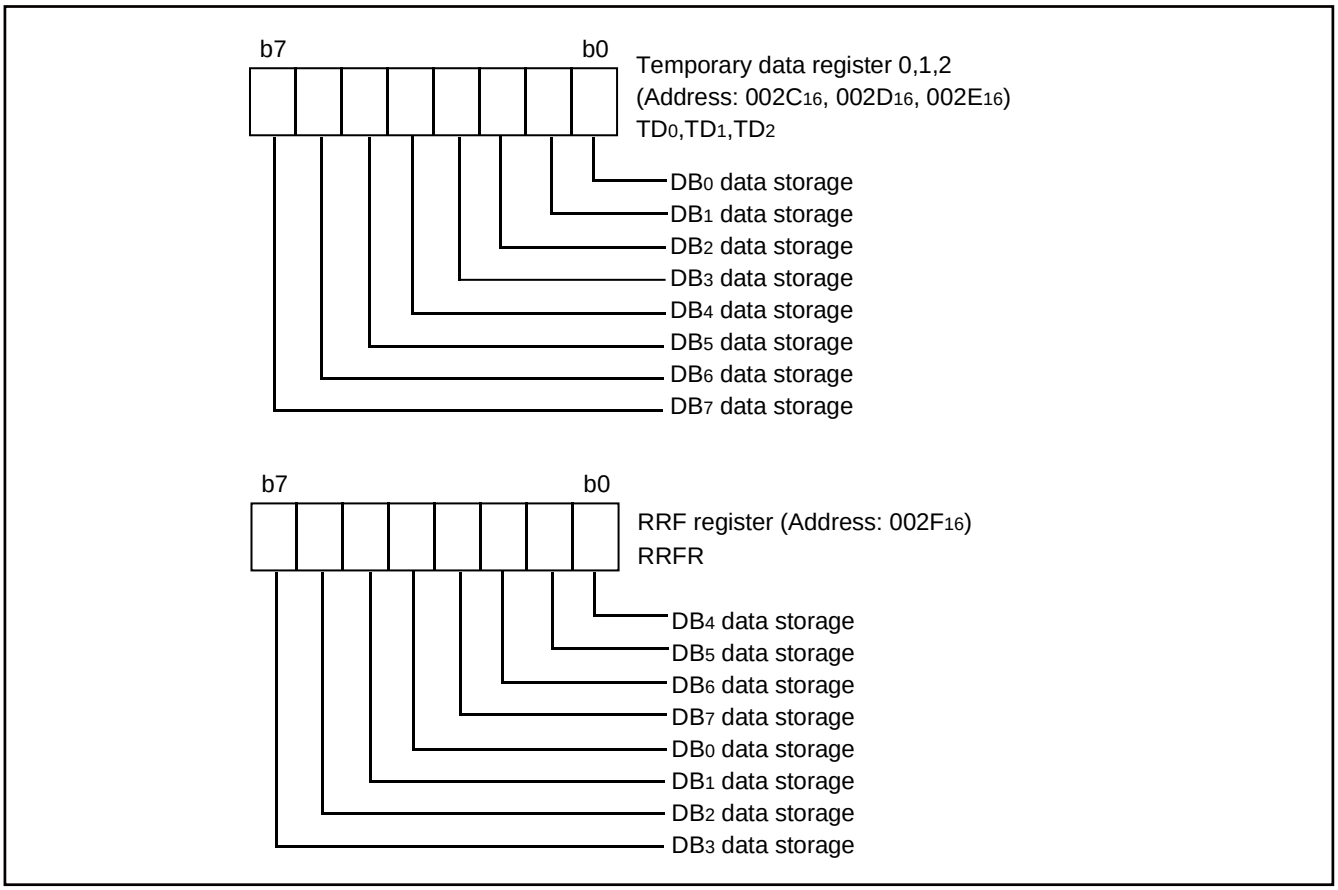


Fig. 46 Structure of temporary register, RPF register

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit counter.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register, each watchdog timer is set to "FF16." Instructions such as STA, LDM and CLB to generate the write signals can be used.
The written data in bits 0 to 5 are not valid, and the above values are set.
Bits 7 and 6 can be rewritten only once after reset.
After rewriting it is disable to write any data to this bit. These bits become "0" after reset.

Standard Operation of Watchdog Timer

The watchdog timer is in the stop state at reset and the watchdog timer starts to count down by writing an optional value in the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer. Then, reset is released after the reset release time is elapsed, the program starts from the reset vector address. Normally, writing to the watchdog timer control register before an underflow of the watchdog timer is programmed. If writing to the watchdog timer control register is not executed, the watchdog timer does not operate.
When reading the watchdog timer control register is executed, the contents of the high-order 6-bit counter and the STP instruction bit (bit 6), and the count source selection bit (bit 7) are read out.

Bit 6 of Watchdog Timer Control Register

- When bit 6 of the watchdog timer control register is "0", the MCU enters the stop mode by execution of STP instruction.
  Just after releasing the stop mode, the watchdog timer restarts counting (Note). When executing the WIT instruction, the watchdog timer does not stop.
- When bit 6 is "1", execution of STP instruction causes an internal reset. When this bit is set to "1" once, it cannot be rewritten to "0" by program. Bit 6 is "0" at reset.

The time until the underflow of the watchdog timer register after writing to the watchdog timer control register is executed is as follows (when the bit 7 of the watchdog timer control register is "0") ;

- at frequency/2/4/8 mode (f(XIN)) = 8 MHz): 32.768 ms
- at low-speed mode (f(XCIN) = 32 KHz): 8.19s

■ Note

The watchdog timer continues to count even during the wait time set by timer 1 and timer 2 to release the stop state and in the wait mode. Accordingly, do not underflow the watchdog timer in this time.

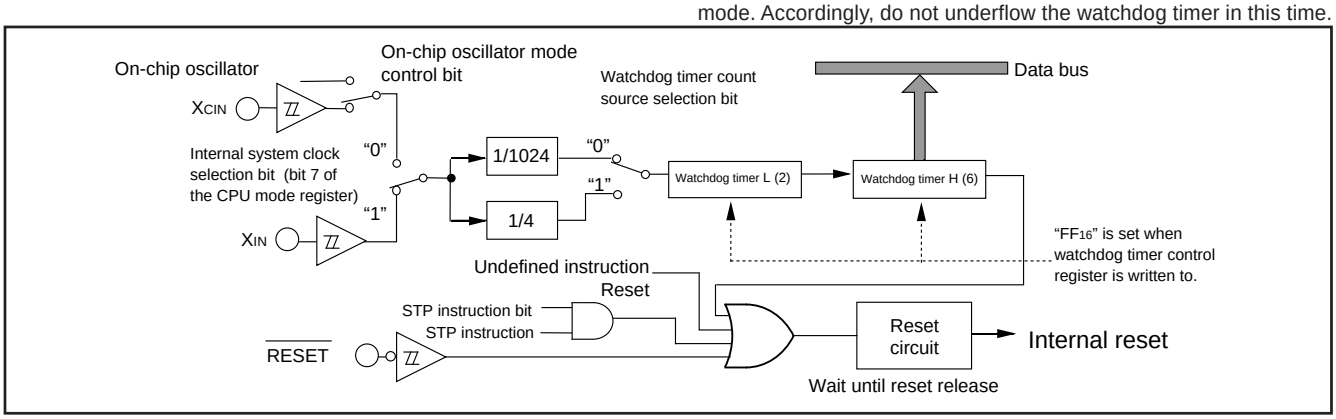


Fig. 47 Block diagram of Watchdog timer

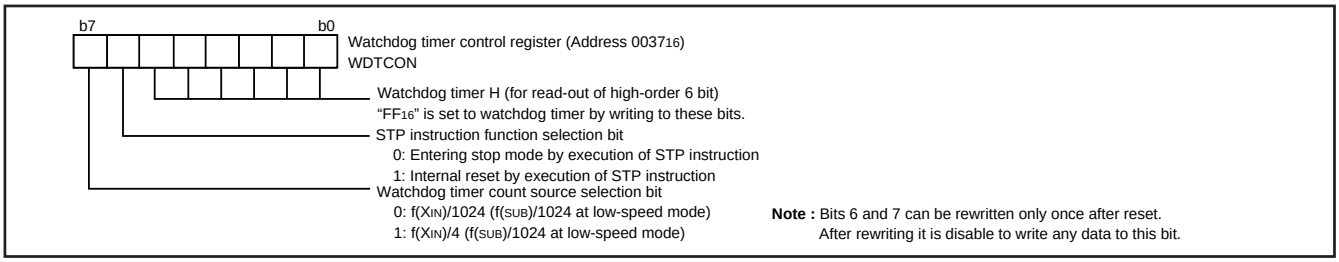


Fig. 48 Structure of Watchdog timer control register

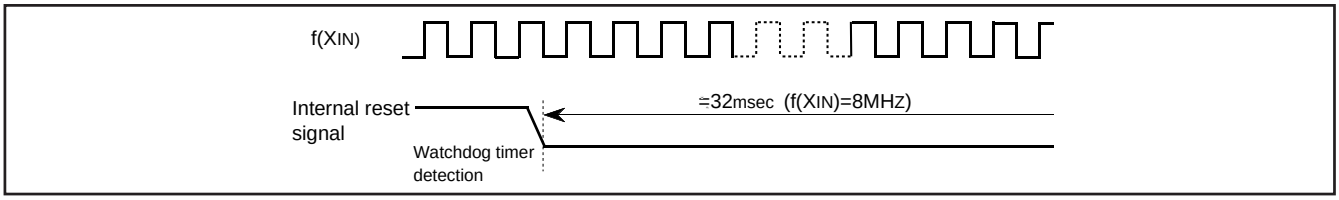


Fig. 49 Timing of reset output

PERIPHERAL FUNCTION EXTENSION REGISTER

The serial I/O transfer direction can be switched by setting the bit 0 in the peripheral function expansion register to “1”. This function is valid only when the bit 6 in the serial I/O control register is set to “1” (when the clock synchronous serial I/O is selected). P47 can be selected as the output pin of the clock synchronous serial I/O by setting the bit 1 in the peripheral function expansion register to “1”. When setting P47 to the SOUT pin, set the bit 7 in the port P4 direction register to “1”. This function is valid only when the bit 6 in the serial I/O control register to “1” (when the clock synchronous serial I/O is selected). P-channel output of TXD and SOUT can be disabled by the bits 2 and 3 in the peripheral function expansion register. Set the bit 4 in the UART control register to “1” after selecting the pin to disable the P-channel output. XCIN frequency signal can be output from the port P41 by setting the bit 4 in the peripheral function expansion register to “1”. Set the bit 0 in the ϕ output control register and the bit 1 in the port P4 direction register to “1” to output the XCIN frequency signal.

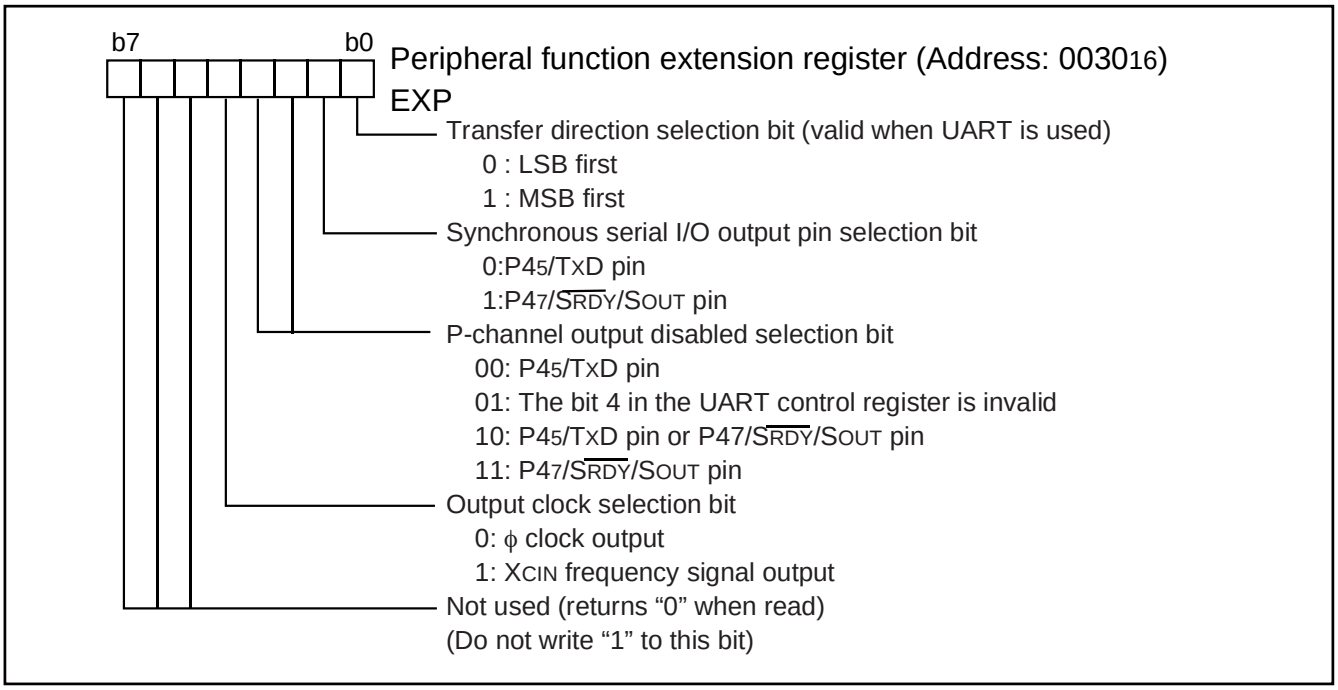


Fig. 50 Structure of peripheral function extension register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between V_{CC}(min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes V_{CC}(min.).

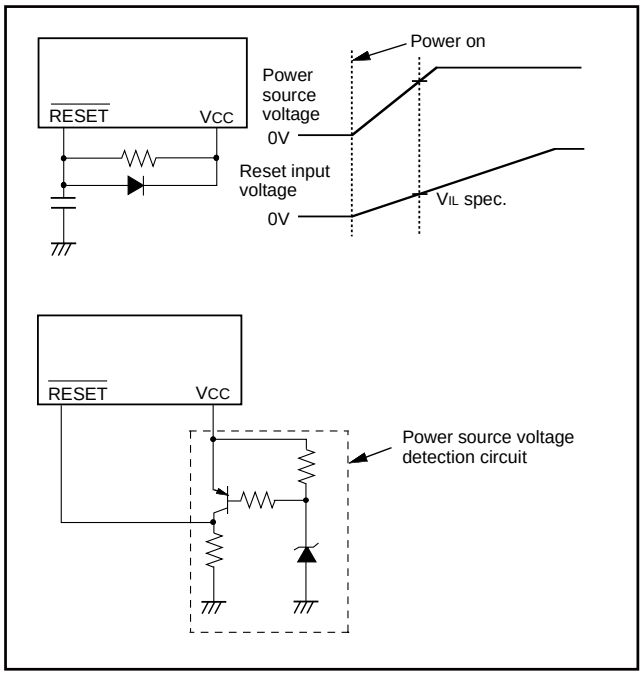
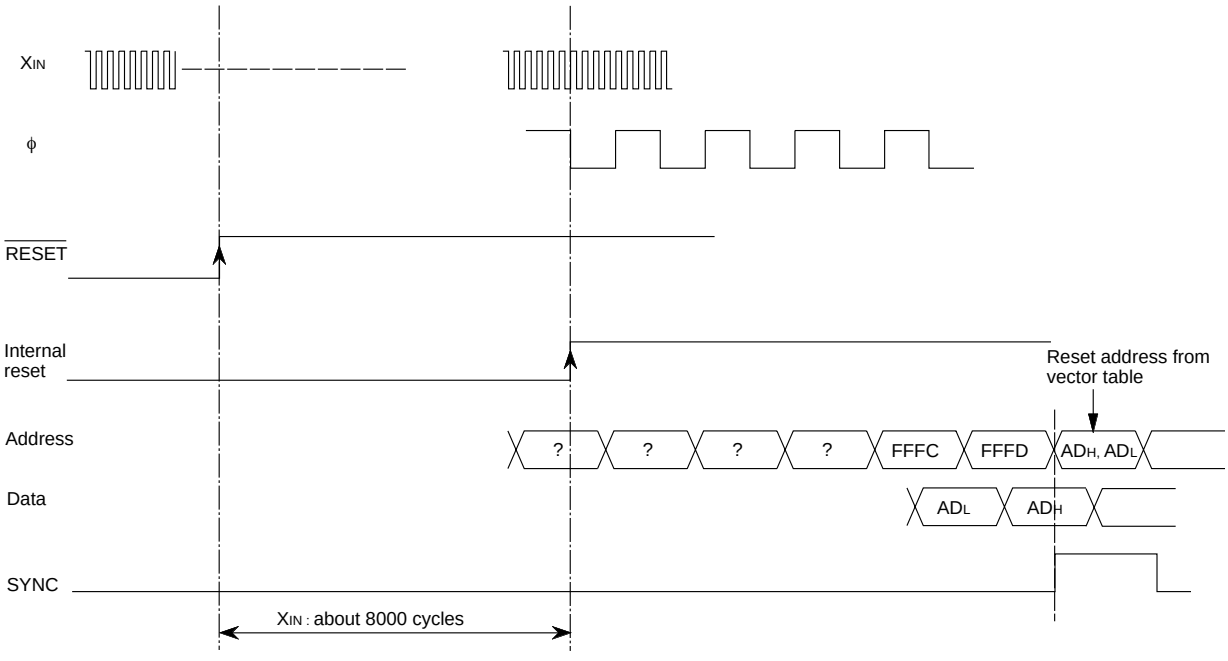


Fig. 51 Reset Circuit Example



Notes 1: The frequency relation of f(X_{IN}) and f(ϕ) is f(X_{IN}) =8•f(ϕ)
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig. 52 Reset Sequence

		Address	Register Contents
(1)	Port P0 direction register	000116	0016
(2)	Port P1 direction register	000316	0016
(3)	Port P2 direction register	000516	0016
(4)	Port P4 direction register	000916	0016
(5)	Port P5 direction register	000B16	0016
(6)	Port P6 direction register	000D16	0016
(7)	Port P7 direction register	000F16	0016
(8)	ROM correctoin enable register (RCR)	001416	0016
(9)	PULL register A	001616	0 0 0 0 1 0 1 1
(10)	PULL register B	001716	0016
(11)	Sirial I/O status register	001916	1 0 0 0 0 0 0 0
(12)	Sirial I/O control register	001A16	0016
(13)	UART control register	001B16	1 1 1 0 0 0 0 0
(14)	Timer X high-order register	002016	FF16
(15)	Timer X low-order register	002116	FF16
(16)	Timer Y high-order register	002216	FF16
(17)	Timer Y low-order register	002316	FF16
(18)	Timer 1 register	002416	FF16
(19)	Timer 2 register	002516	0116
(20)	Timer 3 register	002616	FF16
(21)	Timer X mode register	002716	0016
(22)	Timer Y mode register	002816	0016
(23)	Timer 123 mode register	002916	0016
(24)	ϕ output control register	002A16	0016
(25)	CPU mode extension register	002B16	0016
(26)	Temporary data register 0	002C16	0016
(27)	Temporary data register 1	002D16	0016
(28)	Temporary data register 2	002E16	0016
(29)	RRF register	002F16	0016
(30)	Peripheral function extension register	003016	0016
(31)	AD control register	003416	0 0 0 0 1 0 0 0
(32)	AD conversion low-order register	003616	X X 0 0 0 0 0 0
(33)	Watchdog timer control register	003716	0 0 1 1 1 1 1 1
(34)	Segment output enable register	003816	0016
(35)	LCD mode register	003916	0016
(36)	Interrupt edge selection register	003A16	0016
(37)	CPU mode register	003B16	0 1 0 0 1 0 0 0
(38)	Interrupt request register 1	003C16	0016
(39)	Interrupt request register 2	003D16	0016
(40)	Interrupt control register 1	003E16	0016
(41)	Interrupt control register 2	003F16	0016
(42)	Processor status register	(PS)	X X X X X 1 X X
(43)	Program counter	(PC_H)	Contents of address FFFD16
		(PC_L)	Contents of address FFFC16

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X: undefined

Fig. 53 Initial status of microcomputer after reset

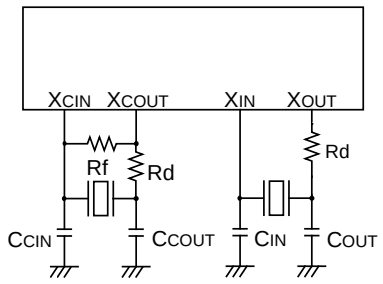
CLOCK GENERATING CIRCUIT

The 3823 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. The oscillation start voltage and the oscillation start time differ in accordance with an oscillator, a circuit constant, or temperature, etc.

When power supply voltage is low and the high frequency oscillator is used, an oscillation start will require sufficient conditions. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. (an external feed-back resistor may be needed depending on conditions.) However, an external feedback resistor is needed between XCIN and XCOUT since a resistor does not exist between them.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.



Note : Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the maker of the oscillator. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 54 Ceramic resonator circuit example

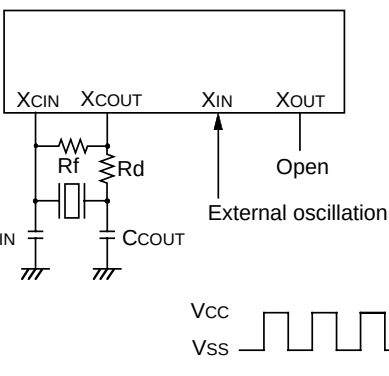


Fig. 55 External clock input circuit

Frequency Control

(1) frequency/8 Mode

The internal clock ϕ is the frequency of XIN divided by 8.
After reset, this mode is selected.

(2) frequency/4 Mode

The internal clock ϕ is the frequency of XIN divided by 4.

(3) frequency/2 Mode

The internal clock ϕ is half the frequency of XIN.

(4) Low-speed Mode

- The internal clock ϕ is the frequency of XIN or on-chip oscillation frequency divided by 2.
- A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to “1”.
  When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.
  In low speed mode, the system clock ϕ can be switched to the on-chip oscillator or XCIN. Use the on-chip oscillator control bit (bit 0 in the CPU mode expansion register) for settings. To set this bit to “0” from “1”, wait until XCIN oscillation stabilizes.

Note 1: If you switch the mode between frequency/2/4/8 mode and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).

2: In frequency/2/4/8 mode, XIN-XOUT oscillation does not stop even if the main clock (XIN-XOUT) stop bit is set to "1".

3: In low speed mode, XCIN-XCOUT oscillation does not stop even if the port XC switch bit is set to "0".

Oscillation Control

(1) Stop Mode

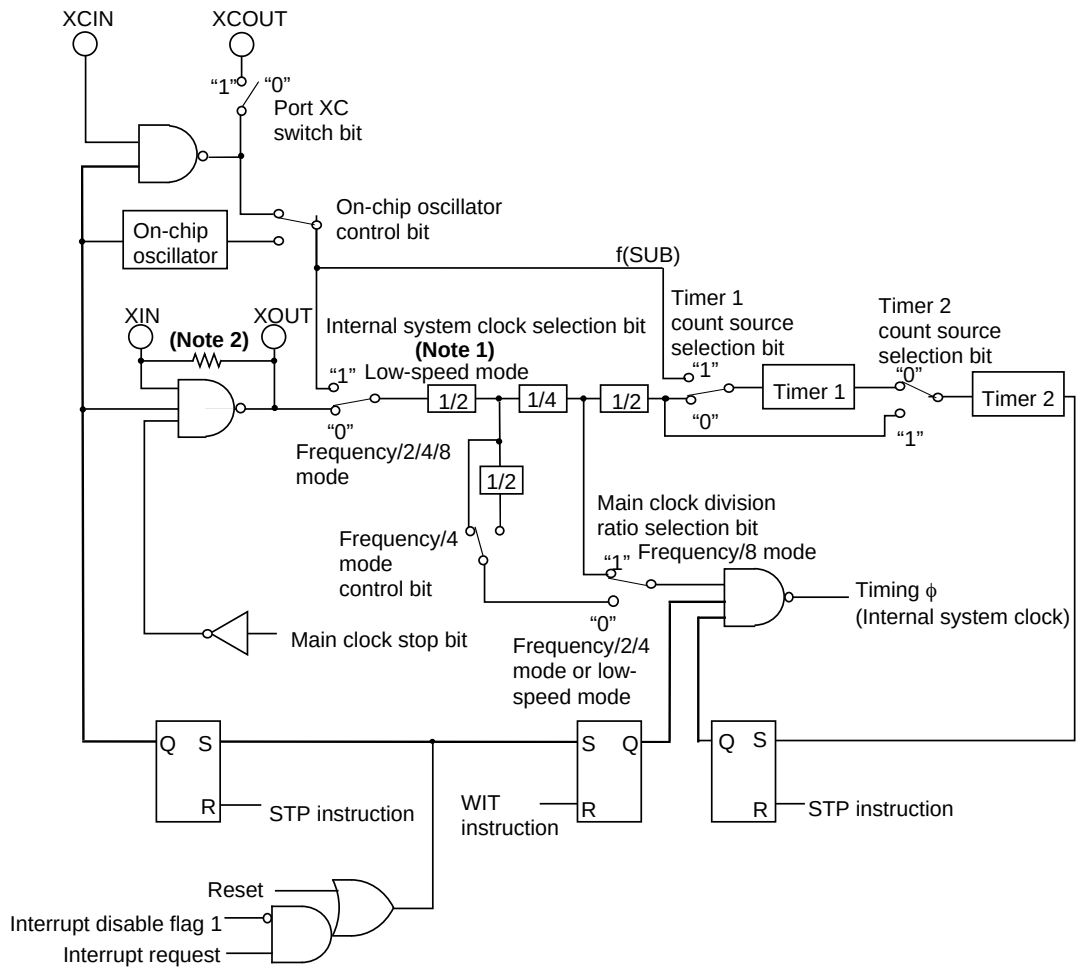
If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction. Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows timer for the clock circuit oscillation to stabilize.

Execution of the STP instruction sets the LCD enable bit (bit 3 of the LCD mode register) to "0" and the LCD panel turns off.To make the LCD panel turn on after returning from the stop mode, set the LCD enable bit to "1".

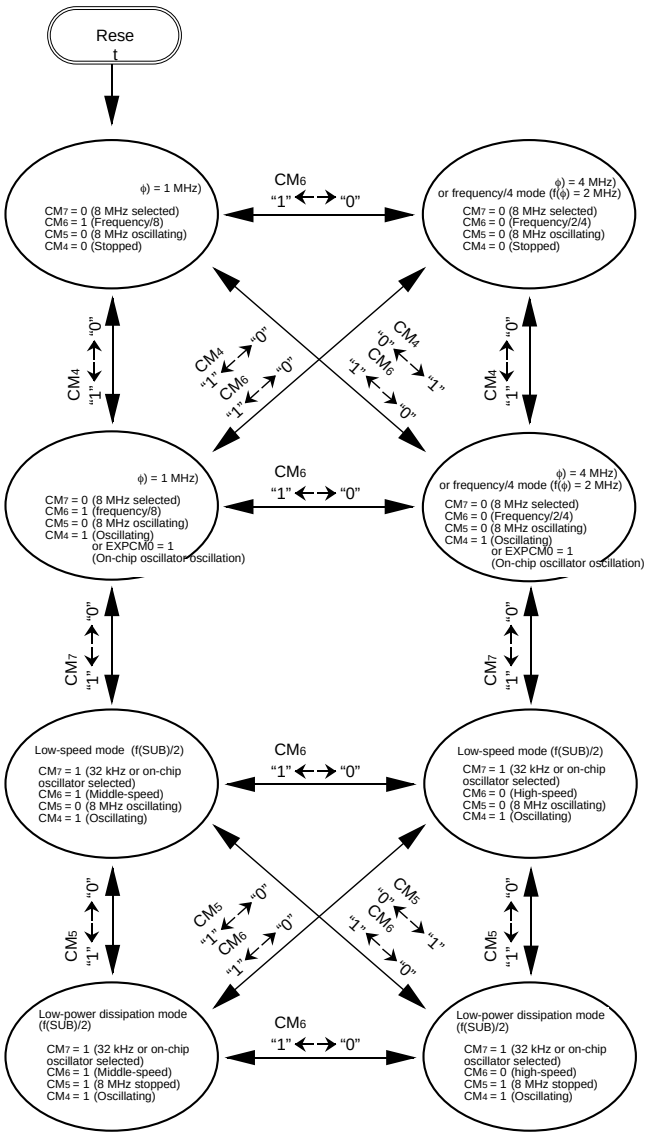
(2) Wait Mode

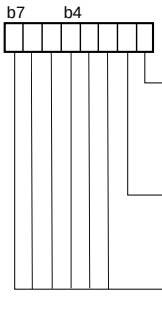
If the WIT instruction is executed, only the system clock ϕ stops at an "H" state. The states of main clock, on-chip oscillator and sub clock are the same as the state before executing the WIT instruction, and oscillation does not stop. Since supply of system clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.



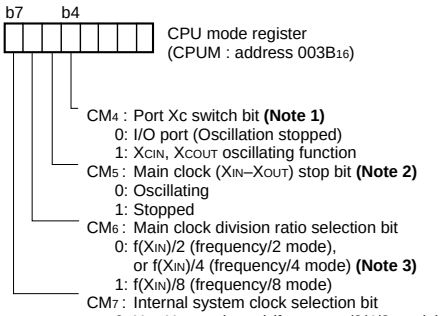
Notes 1: When using the low-speed mode, set the port XC switch bit to "1" .
2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 56 Clock generating circuit block diagram





Note 1 : The on-chip oscillator is selected for the operation clock in low-speed mode regardless of XCIN-XCOUT.
2 : Valid only when the main clock division ratio selection bit (bit 6 in the CPU mode register) is set to "0". When "1" (frequency/8 mode) is selected for the main clock division ratio selection bit or when the internal system clock selection bit is set to 1, set "0" to the frequency/4 mode control bit.



Note 1 : In low speed mode (XCIN is selected as the system clock ϕ), XCIN-XCOUT oscillation does not stop even if the port XC switch bit is set to "0".
2 : In frequency/2/4/8 mode, XIN-XOUT oscillation does not stop even if the main clock (XIN-XOUT) stop bit is set to "1".
3 : When the system clock ϕ is divided by 4 of f(XIN), set the bit 6 in the CPU mode register to "0" after setting the bit 1 in the CPU mode extension register to "1".
4 : When using the on-chip oscillator in low-speed mode, set the bit 7 in the CPU mode register to "1" after setting the bit 0 in the CPU mode extension register to "1".

Notes
1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.
3 : Timer and LCD operate in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs automatically by timer 1 and timer 2 in frequency/2/4/8 mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs automatically by timer 1 and timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to frequency/2/4/8 mode.
7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.
8 : f(SUB) is the source oscillation frequency in low-speed mode. f(SUB) shows the oscillation frequency of XCIN or the on-chip oscillator. Internal clock ϕ is f(SUB)/2 in the low-speed mode.
9 : Set the CPU mode expansion register in advance when switching to low-speed mode which uses mode divided by 4 and on-chip oscillator.
10: In low speed mode, the system clock ϕ can be switched to the on-chip oscillator or XCIN. Use the on-chip oscillator control bit (bit 0 in the CPU mode expansion register) for settings. To set this bit to "0" from "1", wait until XCIN oscillation stabilizes.

Fig. 57 State transitions of system clock

QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 13 lists the pin description (QzROM writing mode) and Figure 58 and Figure 59 show the pin connections.
Refer to Figure 60 and Figure 61 for examples of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer. Refer to the user's manual of your serial programmer for details on how to use it.

Table 13 Pin description (QzROM writing mode)

Pin	Name	I/O	Function
V_{CC}, V_{SS}	Power source	Input	• Apply 1.8 to 5.5 V to V_{CC}, and 0 V to V_{SS}.
$\overline{RESET}$	Reset input	Input	• Reset input pin for active "L". Reset occurs when $\overline{RESET}$ pin is hold at an "L" level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	Input	• Set the same termination as the single-chip mode.
X_{OUT}	Clock output	Output	
V_{REF}	Analog reference voltage	Input	• Input the reference voltage of A/D converter to V_{REF}.
AVss	Analog power source	Input	• Connect AVss to Vss.
$P0_0$ –$P0_7$ $P1_0$ –$P1_7$ $P2_0$ –$P2_7$ $P3_4$ –$P3_7$ $P4_1$–$P4_4$ $P5_0$ –$P5_7$ $P6_0$ –$P6_7$	I/O port	I/O	• Input "H" or "L" level signal or leave the pin open.
$P4_0$	V_{PP} input	Input	• QzROM programmable power source pin.
$P4_4$	ESDA input/output	I/O	• Serial data I/O pin.
$P4_2$	ESCLK input	Input	• Serial clock input pin.
$P4_3$	ESPGMB input	Input	• Read/program pulse input pin.

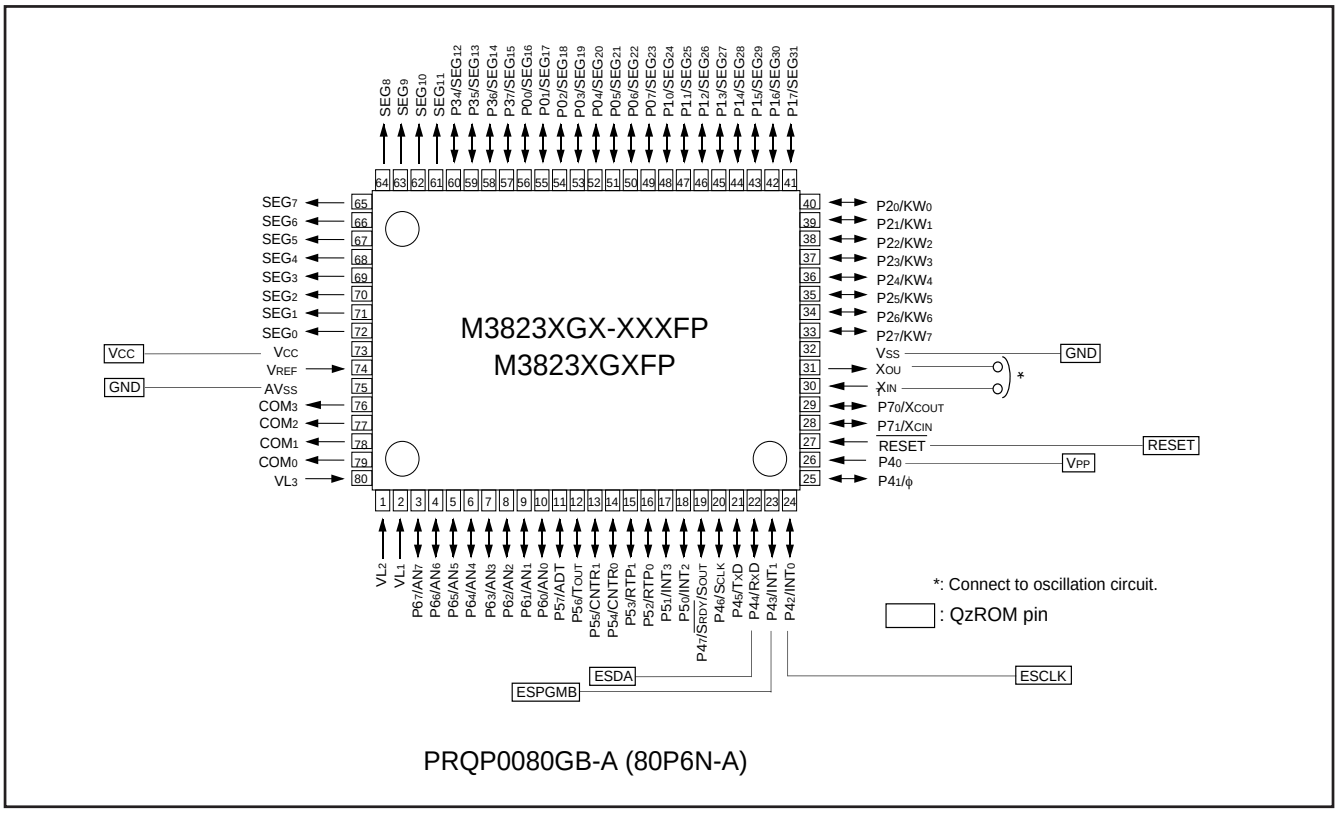


Fig. 58 Pin connection diagram (M3823XGX-XXXFP)

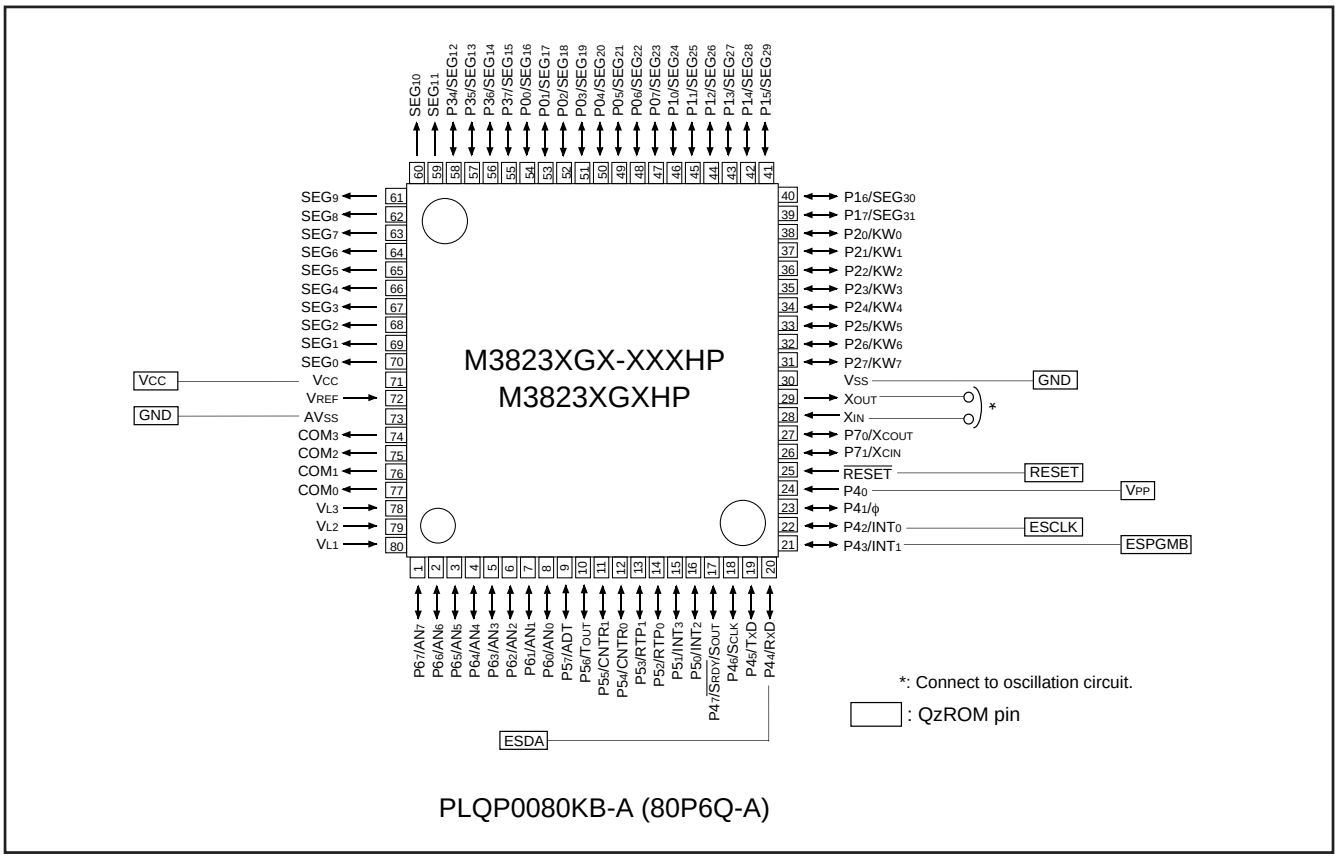
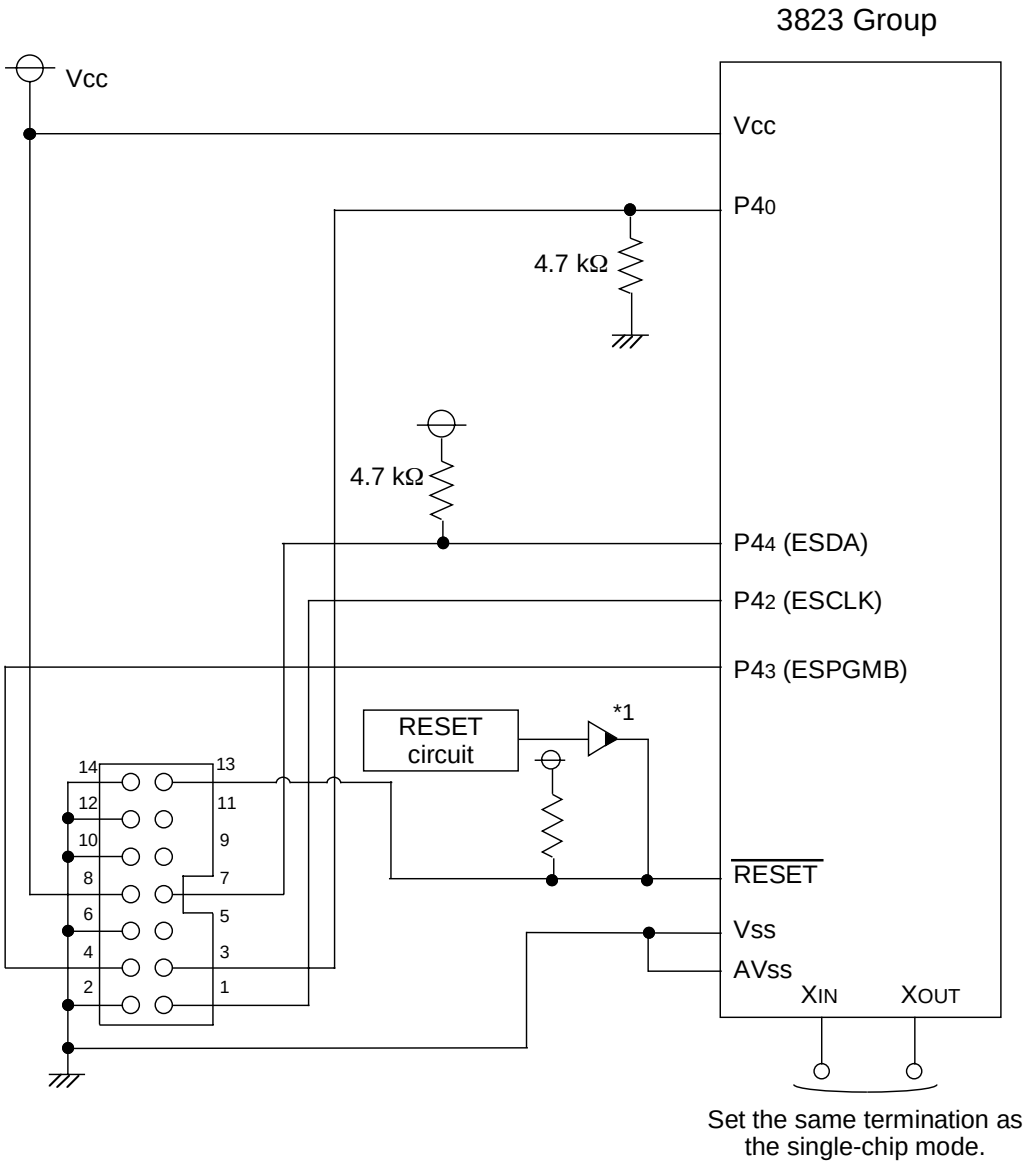


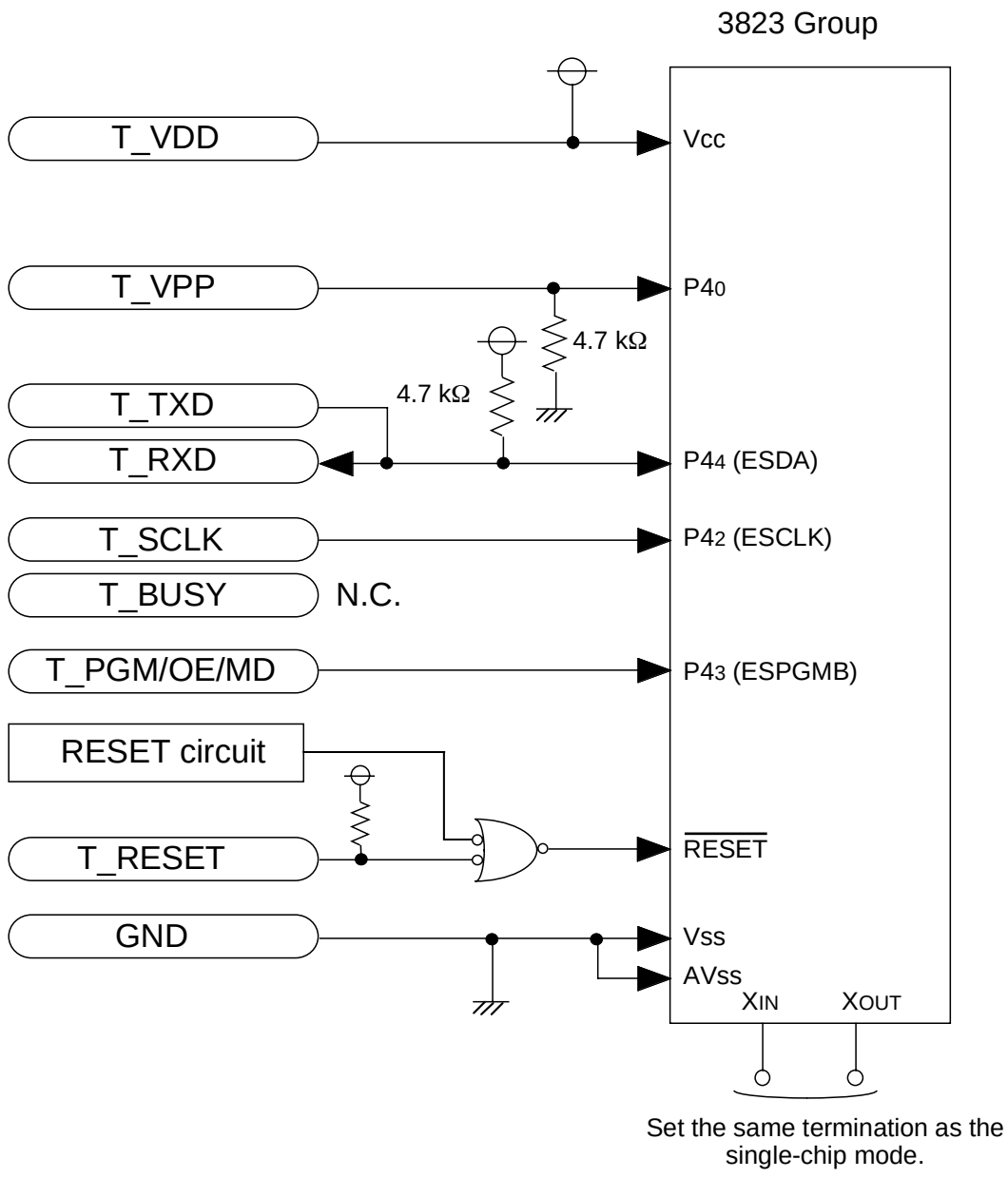
Fig. 59 Pin connection diagram (M3823XGX-XXXHP)



* 1 : Open-collector buffer

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 60 When using E8 programmer, connection example



Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 61 When using programmer of Sisei Electronics System Co., LTD, connection example

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations. Initialize these flags at the beginning of the program.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to “1”.
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A/D Converter

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough. Accordingly, set f(XIN) to at least 500kHz during A/D conversion in the middle-or high-speed mode.
Also, do not execute the STP or WIT instruction during an A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the on-chip oscillator, the minimum value of f(XIN) frequency is not limited.

LCD Drive Control Circuit

Execution of the STP instruction sets the LCD enable bit (bit 3 of the LCD mode register) to “0” and the LCD panel turns off.To make the LCD panel turn on after returning from the stop mode, set the LCD enable bit to “1”.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the XIN frequency.

Countermeasures against noise

(1) Shortest wiring length

① Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

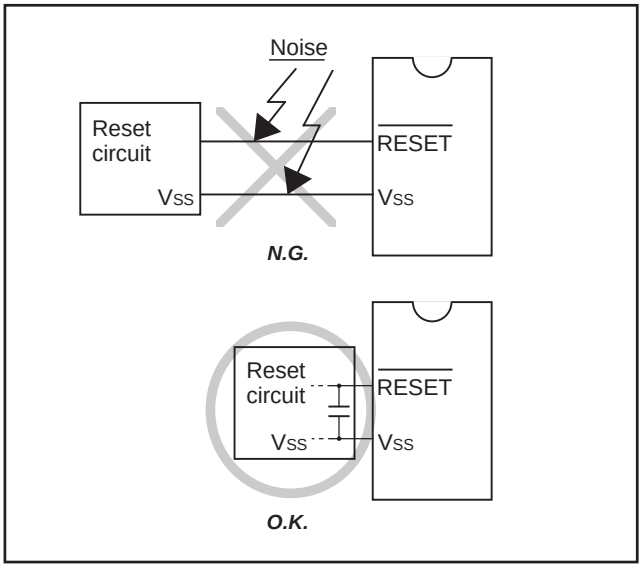


Fig. 62 Wiring for the RESET pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

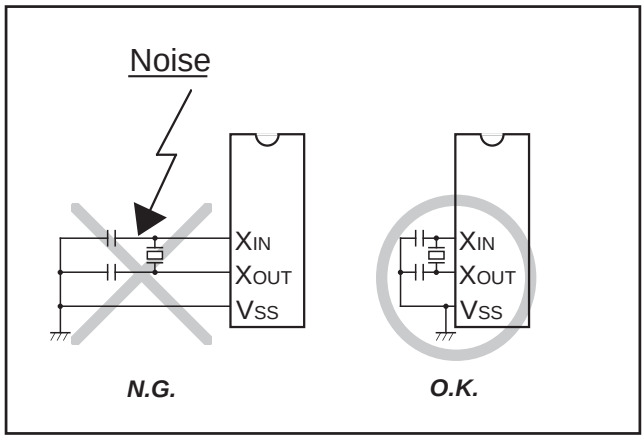


Fig. 63 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

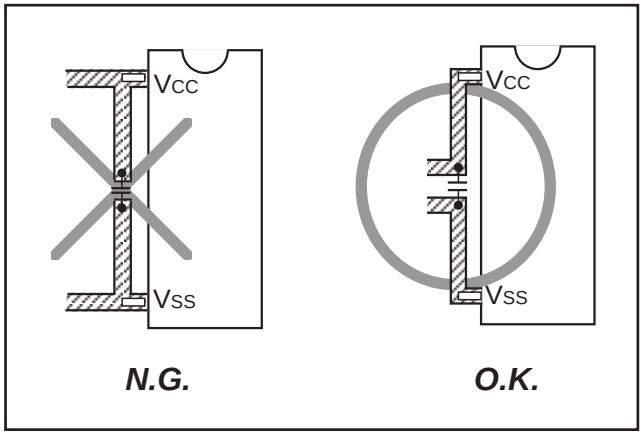


Fig. 64 Bypass capacitor across the Vss line and the Vcc line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of votage and temperature is wide.

Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

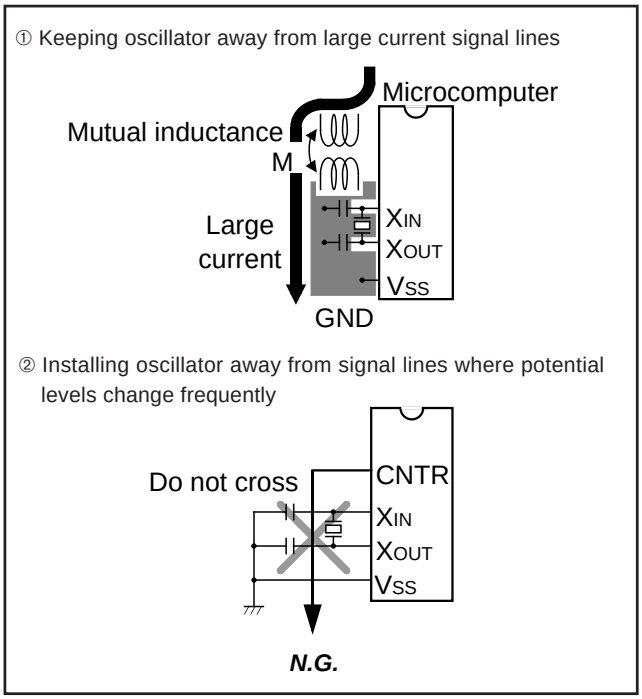


Fig. 65 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory size

When memory size differ in one group, actual values such as an electrical characteristics, A/D conversion accuracy, and the amount of -proof of noise incorrect operation may differ from the ideal values. When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to P40/(VPP) pin

When using P40/(VPP) pin as an input port, connect an approximately 5 kΩ resistor to the P40/(VPP) pin the shortest possible in series.

When not using P40/(VPP) pin, connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer.

● Reason

The P40/(VPP) pin of the QzROM version is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the VPP pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the P40/(VPP) pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

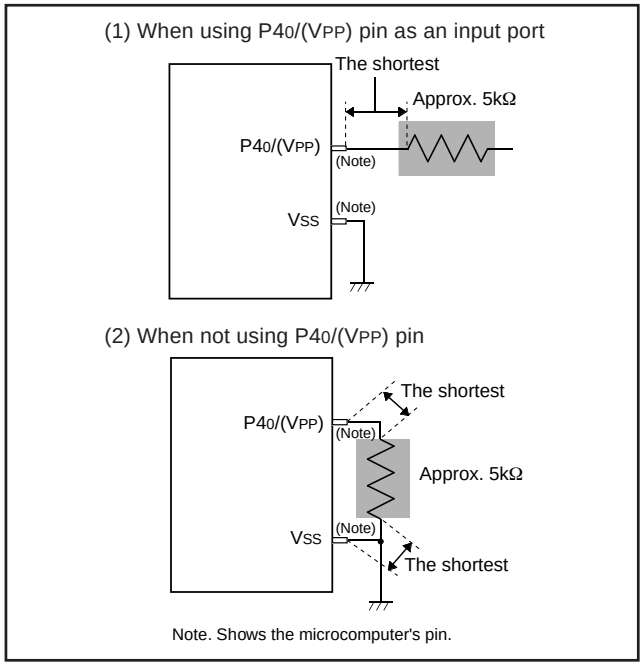


Fig. 66 Wiring for the P40/(VPP) pin

NOTES ON USE
Power Source Voltage
When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

LCD drive power supply
Power supply capacitor may be insufficient with the division resistance for LCD power supply,and the characteristic of the LCD panel.In this case,there is the method of connecting the bypass capacitor about 0.1 –0.33μF to V_{L1} –V_{L3} pins.The example of a strengthening measure of the LCD drive power supply is shown in Figure 67.

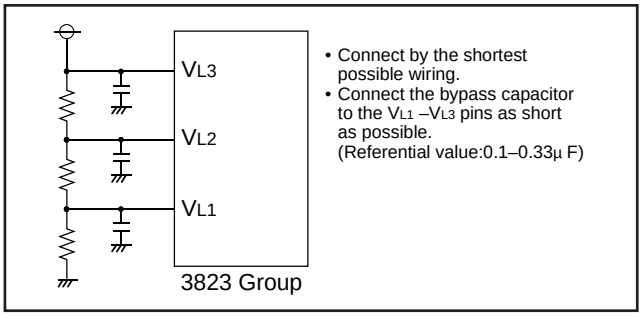


Fig. 67 Strengthening measure example of LCD drive power supply

Product shipped in blank
As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Overvoltage
Make sure that voltage exceeding the Vcc pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in figure below does not occur for pin $P4_0$ (V_{PP} power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

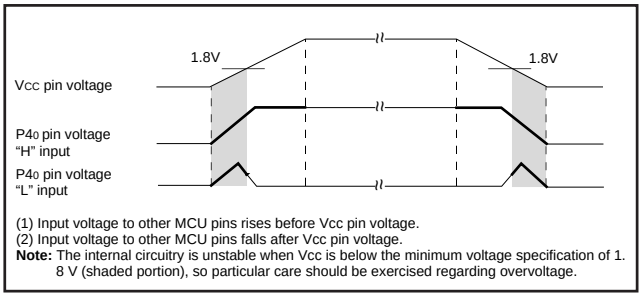


Fig. 68 Timing Diagram (Applies to section indicated by bold line.)

NOTES ON QzROM
Notes On QzROM Writing Orders
When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.
Be sure to set the ROM option ("MASK option" written in the mask file converter) setup when making the mask file by using the mask file converter MM.

Notes On ROM Code Protect (QzROM product shipped after writing)
As for the QzROM product shipped after writing, the ROM code protect is specified according to the ROM option setup data in the mask file which is submitted at ordering.
The ROM option setup data in the mask file is "00_{16}" for protect enabled or "FF_{16}" for protect disabled. Therefore, the contents of the ROM code protect address (other than the user ROM area) of the QzROM product shipped after writing is "00_{16}" or "FF_{16}".
Note that the mask file which has nothing at the ROM option data or has the data other than "00_{16}" and "FF_{16}" can not be accepted.

DATA REQUIRED FOR QzROM WRITING ORDERS
The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

ELECTRICAL CHARACTERISTICS

Table 14 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P3_4$–$P3_7$	At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{11}		–0.3 to V_{L3}	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 150	°C

Table 15 Recommended operating conditions (1)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage (**Note 1**)	Frequency/2 mode	f(X_{IN}) = 10 MHz	4.5	5.0	5.5	V
			f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
			f(X_{IN}) = 5 MHz	2.0	5.0	5.5	V
			f(X_{IN}) = 2.5 MHz	1.8	5.0	5.5	V
		Frequency/4 mode	f(X_{IN}) = 10 MHz	2.5	5.0	5.5	V
			f(X_{IN}) = 8 MHz	2.0	5.0	5.5	V
			f(X_{IN}) = 5 MHz	1.8	5.0	5.5	V
		Frequency/8 mode	f(X_{IN}) = 10 MHz	2.5	5.0	5.5	V
			f(X_{IN}) = 8 MHz	2.0	5.0	5.5	V
			f(X_{IN}) = 5 MHz	1.8	5.0	5.5	V
		Low-speed mode (OCO included)		1.8	5.0	5.5	V
V_{SS}	Power source voltage				0		V
V_{L3}	LCD power voltage			2.5		5.5	V
V_{REF}	A/D conversion reference voltage			1.8		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage AN_0–AN_7			AV_{SS}		V_{REF}	V

Note : When the A/D converter is used, refer to the recommended operating condition for A/D converter.

Table 16 Recommended operating conditions (2)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$,$P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0		0.3 V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.2 V_{CC}	V

Table 17 Recommended operating conditions (3)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			–2	mA
$I_{OH(peak)}$	"H" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.5 V ≤ V_{CC} ≤ 5.5 V)			5.0	MHz
		(4.0 V ≤ V_{CC} ≤ 4.5 V)			2 × V_{CC} – 4	MHz
		(2.0 V ≤ V_{CC} ≤ 4.0 V)			0.75 × V_{CC} + 1	MHz
		(V_{CC} ≤ 2.0 V)			6.25 × V_{CC} - 10	MHz
f(X_{IN})	Main clock input oscillation frequency (duty cycle 50%) **(Note 4)**	Frequency/2 mode (4.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		Frequency/2 mode (4.0 V ≤ V_{CC} ≤ 4.5 V)			4 × V_{CC} – 8	MHz
		Frequency/2 mode (2.0 V ≤ V_{CC} ≤ 4.0 V)			1.5 × V_{CC} + 2	MHz
		Frequency/2 mode (1.8 V ≤ V_{CC} ≤ 2.0 V)			12.5 × V_{CC} - 20	MHz
		Frequency/4 mode (2.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		Frequency/4 mode (2.0 V ≤ V_{CC} ≤ 2.5 V)			4 × V_{CC}	MHz
		Frequency/4 mode (1.8 V ≤ V_{CC} ≤ 2.0 V)			15 × V_{CC} – 22	MHz
		Frequency/8 mode (2.5 V ≤ V_{CC} ≤ 5.5 V)			10.0	MHz
		Frequency/8 mode (2.0 V ≤ V_{CC} ≤ 2.5 V)			4 × V_{CC}	MHz
		Frequency/8 mode (1.8 V ≤ V_{CC} ≤ 2.0 V)			15 × V_{CC} – 22	MHz
f(X_{CIN})	Sub-clock input oscillation frequency (duty cycle 50%) **(Note 5)**			32.768	80	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the A/D converter is used, refer to the recommended operating condition for A/D converter.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 18 Electrical characteristics (1)
(V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_3, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.0 V to 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
		V_{CC} = 5 V, V_I = V_{CC} Pull-downs "on"	30	70	140	µA
		V_{CC} = 3 V, V_I = V_{CC} Pull-downs "on"	6.0	25	45	µA
I_{IH}	"H" input current $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$,$P4_0$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
		V_{CC} = 3 V, V_I = V_{SS} Pull-ups "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
V_{RAM}	RAM hold voltage	When clock is stopped	1.8		5.5	V

Note: When "1" is set to the port X_C switch bit (bit 4 at address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

Table 19 Electrical characteristics (2)

(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	Frequency/2 mode	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		4.3	8.6	mA
				f(X_{IN}) = 8 MHz		3.7	7.4	mA
				f(X_{IN}) = 4 MHz		2.5	5.0	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 4 MHz		0.8	1.6	mA
				f(X_{IN}) = 2 MHz		0.4	0.8	mA
		Frequency/4 mode	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		2.9	5.8	mA
				f(X_{IN}) = 8 MHz		2.5	5.0	mA
				f(X_{IN}) = 4 MHz		1.7	3.4	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 10 MHz		1.0	2.0	mA
				f(X_{IN}) = 8 MHz		0.8	1.6	mA
				f(X_{IN}) = 4 MHz		0.5	1.0	mA
				f(X_{IN}) = 2 MHz		0.3	0.6	mA
		Frequency/8 mode	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		2.2	4.4	mA
				f(X_{IN}) = 8 MHz		1.9	3.8	mA
				f(X_{IN}) = 4 MHz		1.4	2.8	mA
				f(X_{IN}) = 2 MHz		1.0	2.0	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 10 MHz		0.7	1.4	mA
				f(X_{IN}) = 8 MHz		0.6	1.2	mA
				f(X_{IN}) = 4 MHz		0.4	0.8	mA
				f(X_{IN}) = 2 MHz		0.2	0.4	mA
		Frequency/2/4/8 mode In WIT state	V_{CC} = 5.0 V	f(X_{IN}) = 10 MHz		1.35	2.7	mA
				f(X_{IN}) = 8 MHz		1.2	2.4	mA
				f(X_{IN}) = 4 MHz		0.9	1.8	mA
				f(X_{IN}) = 2 MHz		0.8	1.6	mA
			V_{CC} = 2.5 V	f(X_{IN}) = 10 MHz		0.35	0.7	mA
				f(X_{IN}) = 8 MHz		0.3	0.6	mA
				f(X_{IN}) = 4 MHz		0.2	0.4	mA
				f(X_{IN}) = 2 MHz		0.15	0.3	mA
		Low-speed mode f(X_{IN}) = stopped	V_{CC} = 5.0 V	f(X_{CIN}) = 32 kHz		13	26	µA
				On-chip oscillator		80	240	µA
			V_{CC} = 2.5 V	f(X_{CIN}) = 32 kHz		7	14	µA
				On-chip oscillator		14	42	µA
		Low-speed mode f(X_{IN}) = stopped In WIT state	V_{CC} = 5.0 V	f(X_{CIN}) = 32 kHz		5.5	11	µA
				On-chip oscillator		20	60	µA
			V_{CC} = 2.5 V	f(X_{CIN}) = 32 kHz		3.5	7	µA
				On-chip oscillator		3.5	10	µA
		Current increased at A/D converter operating		V_{CC} = 5 V, all modes		500		µA
				V_{CC} = 2.5 V, all modes		50		µA
		All oscillation stopped Ta = 25 °C, Output transistors “off” (in STP state)				0.1	1.0	µA
		All oscillation stopped Ta = 85 °C, Output transistors “off” (in STP state)					10	µA
R_{OCO}	On-chip oscillator oscillatoin	V_{CC} = 2.5 V, Ta = 25 °C				80		kHz

Table 20 A/D converter characteristics (1) (in 8 bit A/D mode)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
ABS	Absolute accuracy (excluding quantization error)	ADL2 = “0”, ADL1 = “0”, CPUM7 = “0” 2.2 V ≤ V_{CC} = V_{REF} ≤ 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±2	LSB
		ADL2 = “0”, ADL1 = “0”, CPUM7 = “0” 2.0 V ≤ V_{CC} = V_{REF} < 2.2 V f(X_{IN}) = 4.4 MHz			±3	LSB
		ADL2 = “0”, ADL1 = “1”, CPUM7 = “0” V_{CC} = V_{REF} = 4.0 to 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±3	LSB
		ADL2 = “1”, ADL1 = “0”, CPUM7 = “1” and EXPCM0 = “1” V_{CC} = V_{REF} = 1.8 to 2.2 V			±4	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz (ADL2 = “0”, ADL1 = “0”, CPUM7 = “0”)			TC(X_{IN})×100	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Table 21 A/D converter characteristics (2) (in 10 bit A/D mode)
(V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				10	Bits
ABS	Absolute accuracy (excluding quantization error)	ADL2 = “0”, ADL1 = “0”, CPUM7 = “0” 2.2 V ≤ V_{CC} = V_{REF} ≤ 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±4	LSB
		ADL2 = “0”, ADL1 = “1”, CPUM7 = “0” V_{CC} = V_{REF} = 4.0 to 5.5 V f(X_{IN}) = 2 × V_{CC} MHz ≤ 10 MHz			±4	LSB
		ADL2 = “1”, ADL1 = “0”, CPUM7 = “1” and EXPCM0 = “1” V_{CC} = V_{REF} = 1.8 to 2.2 V			±4	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz (ADL2 = “0”, ADL1 = “0”, CPUM7 = “0”)			TC(X_{IN})×100	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Table 22 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	4.0 ≤ Vcc < 4.5 V	1000/(4 × V_{CC}–8)			ns
		4.5 ≤ Vcc ≤ 5.5 V	100			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	4.0 ≤ Vcc < 4.5 V	45			ns
		4.5 ≤ Vcc ≤ 5.5 V	40			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	4.0 ≤ Vcc < 4.5 V	45			ns
		4.5 ≤ Vcc ≤ 5.5 V	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	4.0 ≤ Vcc < 4.5 V	1000/(2 × V_{CC}–4)			ns
		4.5 ≤ Vcc ≤ 5.5 V	200			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	4.0 ≤ Vcc < 4.5 V	105			ns
		4.5 ≤ Vcc ≤ 5.5 V	85			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	4.0 ≤ Vcc < 4.5 V	105			ns
		4.5 ≤ Vcc ≤ 5.5 V	85			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width		80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width		80			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**		800			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**		370			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**		370			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time		220			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time		100			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this limits value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 23 Timing requirements (2)

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	2.0 ≤ Vcc ≤ 4.0 V	125			ns
		Vcc < 2.0 V	1000/(10 × V_{CC}–12)			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	2.0 ≤ Vcc ≤ 4.0 V	50			ns
		Vcc < 2.0 V	70			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	2.0 ≤ Vcc ≤ 4.0 V	50			ns
		Vcc < 2.0 V	70			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	2.0 ≤ Vcc ≤ 4.0 V	1000/V_{CC}			ns
		Vcc < 2.0 V	1000/(5 × V_{CC}–8)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width		$t_{c(CNTR)}$/2–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width		$t_{c(CNTR)}$/2–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width		230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width		230			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**		2000			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**		950			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**		950			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time		400			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time		200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this limits value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 24 Switching characteristics (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note)**			140	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns

Note : When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.

Table 25 Switching characteristics (2)

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–100			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–100			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note)**			350	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			100	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			100	ns

Note : When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.

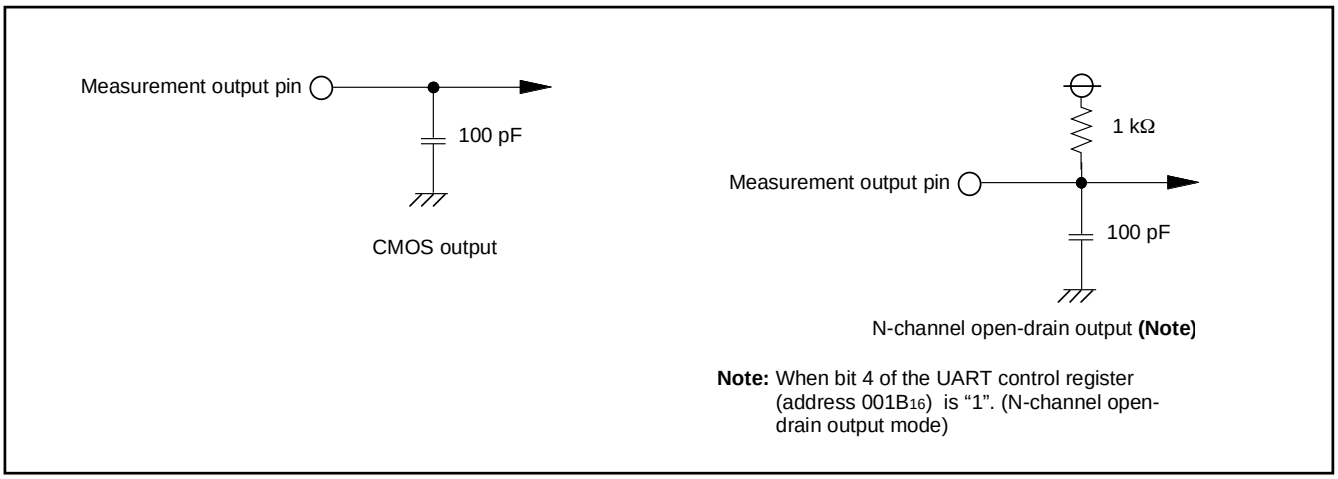


Fig. 69 Circuit for measuring output switching characteristics

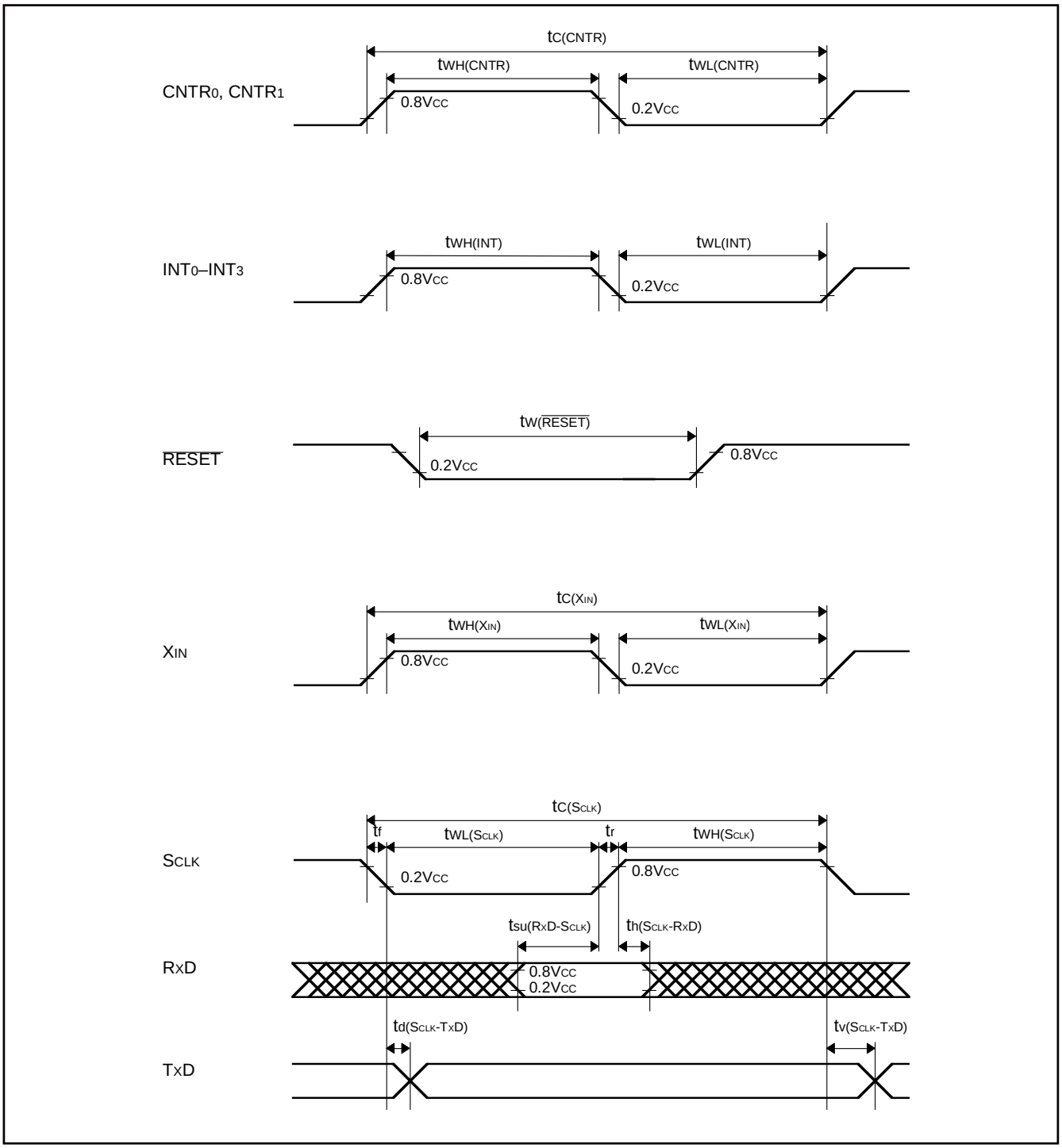
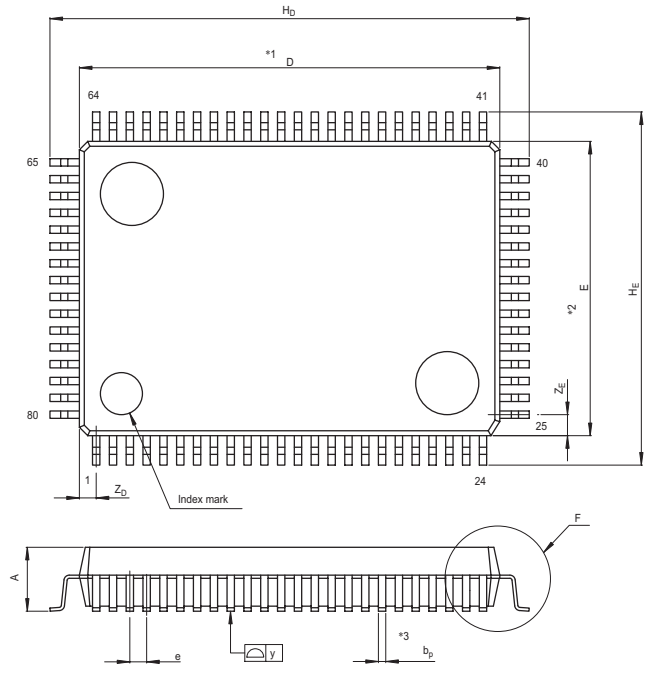


Fig. 70 Timing diagram

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

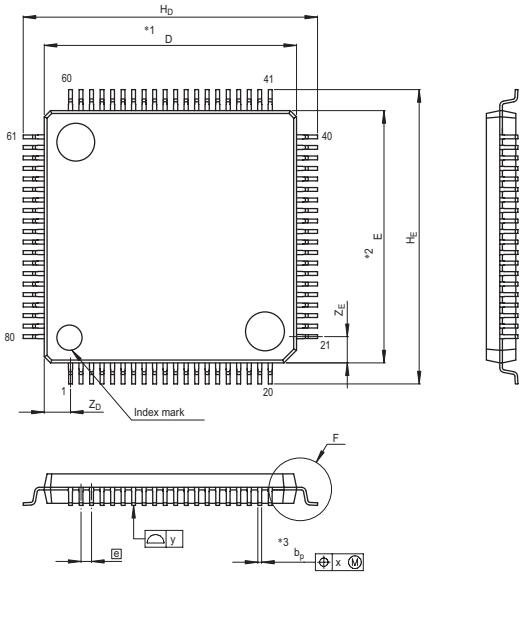
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x20-0.80	PRQP0080GB-A	80P6N-A	1.6g

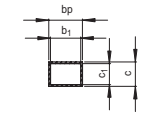


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

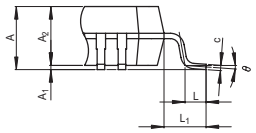
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.65	0.8	0.95
y	—	—	0.10
Z_D	—	0.8	—
Z_E	—	1.0	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	3823 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.00	05/13/05		First edition
2.00	05/07/07	6 8 9 14 40 49 52 54 55 60	Table 3 is partly revised Fig.5 is partly added Table 4 is revised “ROM Code Protect Address” is added Fig.10 is revised “STP instruction Execution” is revised “Oscillation Control” (1) Stop Mode is partly revised “LCD drive Control Circuit” is revised “(6) Wiring to P40/(V_{PP}) pin” is revised Fig.59 is revised Fig.60 is partly deleted “NOTES ON QzROM” is added Table 18 is partly added
2.01	05/11/08	6 61 65-66	Table 3 is partly revised Table 19, 20 are partly revised PACKAGE OUTLINE revised
2.02	07/06/19	– 6 8 9 10 15 22 23-27 46 48 51 52 53 54 55-58 58 59 63 66	“RENESAS TECHNICAL UPDATE” reflected: TN-740-A111A/E Table 3: Function except a port function; •Serial I/O function pins → •Serial interface function pins Fig. 5 M38234G4, M38235G6: Under development → Mass production Note deleted Table 4: Under development deleted FUNCTIONAL DESCRIPTION CENTRAL PROCESSING UNIT (CPU): Description added Fig. 11: Note added CPU mode extension register ($002B_{16}$) → CPU mode expansion register Peripheral function extension register (0030_{16}) → Peripheral function expansion register Table 8: AV_{SS} added, Note revised INTERRUPTS: Description revised, Fig. 18-20 added ROM CORRECTION FUNCTION: Description added Initial Value of Watchdog Timer: Description added Standard Operation of Watchdog Timer: A part of description deleted Bit 6 and bit 7 of Watchdog Timer Control Register: added and revised Fig. 48 revised, Note added Fig. 53: Port P0 direction register (0000_{16}) → (0001_{16}) Frequency Control: Description revised Fig. 56: revised Fig. 57: revised QzROM Writing Mode: added Processor Status Register: added Overvoltage: Description revised and Fig. 68 added Table 15 V_{CC}: Frequency/4 mode → Frequency/8 mode V_{REF}: Limits Min. 2.0 → 1.8 Table 18: V_{RAM} added

Rev.	Date	Description	
		Page	Summary
2.02	07/06/19	67 72	Table 19 ROCO: Ta = 25 °C added Note added

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.0

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View M38239GCFP#U0 on WIN SOURCE
- Renesas Electronics America Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management