



**THE DATASHEET OF
TPS62140ARGTT**



TPS6214x 3-V to 17-V 2-A Step-Down Converter in 3 x 3 QFN Package

1 Features

- DCS-Control™ Topology
- Input Voltage Range: 3 V to 17 V
- Up to 2-A Output Current
- Adjustable Output Voltage from 0.9 V to 6 V
- Pin-Selectable Output Voltage (Nominal, +5%)
- Programmable Soft Start and Tracking
- Seamless Power-Save Mode Transition
- Quiescent Current of 17 μ A (Typical)
- Selectable Operating Frequency
- Power-Good Output
- 100% Duty-Cycle Mode
- Short-Circuit Protection
- Over Temperature Protection
- Pin to Pin Compatible with [TPS62130](#) and [TPS62150](#)
- Available in a 3-mm x 3-mm, VQFN-16 Package

2 Applications

- Standard 12-V Rail Supplies
- POL Supply From Single or Multiple Li-Ion Battery
- Solid-State Disk Drives
- Embedded Systems
- LDO Replacement
- Mobile PCs, Tablet, Modems, Cameras
- Server, Microserver
- Data Terminal, Point of Sales (ePOS)

3 Description

The TPS6214x family is an easy-to-use synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response by use of the DCS-Control™ topology.

With their wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other batteries, as well as from 12-V intermediate power rails. It supports up to 2 A of continuous output current at output voltages between 0.9 V and 6 V (with 100% duty-cycle mode). The output voltage start-up ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the Enable (EN) and open-drain Power Good (PG) pins.

In Power Save Mode, the devices draw quiescent current of about 17 μ A from VIN. Power Save Mode, entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In Shutdown Mode, the device is turned off and current consumption is less than 2 μ A.

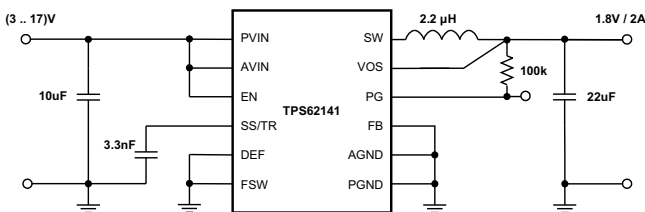
The device, available in adjustable and fixed output voltage versions, is packaged in a 16-pin VQFN package measuring 3 mm x 3 mm (RGT).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6214x	VQFN (16)	3.00 mm x 3.00 mm

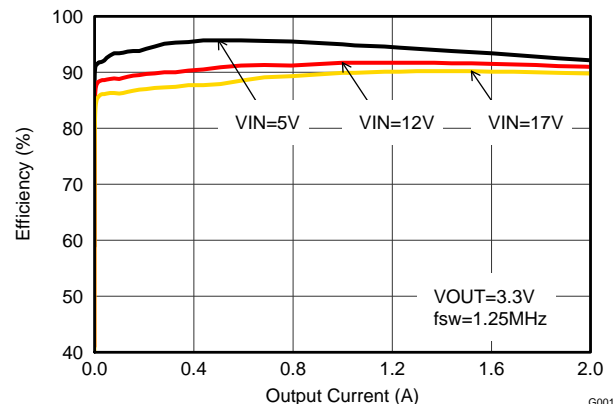
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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Efficiency vs Output Current



G001



Table of Contents

1 Features	1	9.1 Application Information.....	13
2 Applications	1	9.2 Typical Application	13
3 Description	1	9.3 System Examples	25
4 Revision History	2	10 Power Supply Recommendations	28
5 Device Comparison Table	4	11 Layout	29
6 Pin Configuration and Functions	4	11.1 Layout Guidelines	29
7 Specifications	5	11.2 Layout Example	29
7.1 Absolute Maximum Ratings	5	11.3 Thermal Considerations	30
7.2 ESD Ratings.....	5	12 Device and Documentation Support	31
7.3 Recommended Operating Conditions.....	5	12.1 Device Support.....	31
7.4 Thermal Information	5	12.2 Documentation Support	31
7.5 Electrical Characteristics.....	6	12.3 Related Links	31
7.6 Typical Characteristics	7	12.4 Receiving Notification of Documentation Updates	31
8 Detailed Description	8	12.5 Community Resources.....	32
8.1 Overview	8	12.6 Trademarks	32
8.2 Functional Block Diagrams	8	12.7 Electrostatic Discharge Caution.....	32
8.3 Feature Description.....	9	12.8 Glossary	32
8.4 Device Functional Modes.....	11	13 Mechanical, Packaging, and Orderable Information	32
9 Application and Implementation	13		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2015) to Revision E	Page
• Added "Pin to Pin Compatible with TPS62130 and TPS62150" to <i>Features</i> list	1
• Changed the T _J MAX value From: 125°C To: 150°C in the <i>Absolute Maximum Rating</i>	5
• Changed the <i>Thermal Information</i> values	5
• Changed (T _J = -40°C to 85°C) To: (T _J = -40°C to 125°C) in the <i>Electrical Characteristics</i> conditions	6
• Added a test condition for IQ at TA = -40°C to +85°C in the <i>Electrical Characteristics</i>	6
• Added Table 1 and Table 2	10
• Added indicators (C1, C3, and C5) for capacitances to Figure 7	13
• Added Switching Frequency graphs for 1.0-V, 1.8-V, and 5.0-V applications (Figure 24 through Figure 31).....	20
• Changed Layout Example	29

Changes from Revision C (August 2015) to Revision D	Page
• Changed V _{TH_PG} Falling (%V _{OUT}) specification MAX value from "93%" to "94%" in the <i>Electrical Characteristics</i>	6

Changes from Revision B (June 2013) to Revision C	Page
• Added <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

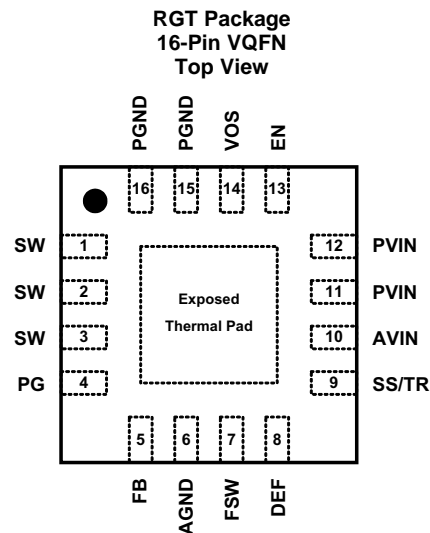
Changes from Revision A (October 2012) to Revision B	Page
• Added new device version TPS62140A to the data sheet.....	1
• Added text to Power Good section regarding the TPS62140A function	10
• Added pin option to the footnote for Pin-Selectable Output (DEF) section.....	10
• Added text to Frequency Selection (FSW) section regarding pin control.....	11
• Added text to Tracking Function section for clarification.....	17
• Added application example with regard to new version TPS62140A.....	25

Changes from Original (November 2011) to Revision A	Page
• Changed the description of the AGND pin, and added Note 3.	4
• Added values to the Initial output voltage accuracy for $T_A = -10^{\circ}\text{C}$ to 85°C	6
• Added text to the Power-Save Mode Operation section following Equation 1	11
• Changed the Layout Considerations section.....	29
• Changed Layout Example	29

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	Power Good Logic Level (EN=Low)
TPS62140	adjustable	High Impedance
TPS62140A	adjustable	Low
TPS62141	1.8 V	High Impedance
TPS62142	3.3 V	High Impedance
TPS62143	5.0 V	High Impedance

6 Pin Configuration and Functions



Pin Functions

PIN ⁽¹⁾		I/O	DESCRIPTION
NO.	NAME		
1,2,3	SW	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
4	PG	O	Output power good (High = V_{OUT} ready, Low = V_{OUT} below nominal regulation) ; open drain (requires pull-up resistor)
5	FB	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
6	AGND		Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
7	FSW	I	Switching Frequency Select (Low \approx 2.5MHz, High \approx 1.25MHz ⁽²⁾ for typical operation) ⁽³⁾
8	DEF	I	Output Voltage Scaling (Low = nominal, High = nominal + 5%) ⁽³⁾
9	SS/TR	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
10	AVIN	I	Supply voltage for control circuitry. Connect to same source as PVIN.
11,12	PVIN	I	Supply voltage for power stage. Connect to same source as AVIN.
13	EN	I	Enable input (High = enabled, Low = disabled) ⁽³⁾
14	VOS	I	Output voltage sense pin and connection for the control loop circuitry.
15,16	PGND		Power Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
	Exposed Thermal Pad		Must be connected to AGND (pin 6), PGND (pin 15,16) and common ground plane. See the Layout Example . Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see the [Detailed Description](#) and [Application and Implementation](#) sections.

(2) Connect FSW to VOUT or PG in this case.

(3) An internal pull-down resistor keeps the logic level low, if pin is floating.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage ⁽²⁾	AVIN, PVIN	-0.3	20	V
	EN, SS/TR	-0.3	V _{IN} +0.3	
	SW	-0.3	V _{IN} +0.3	V
	DEF, FSW, FB, PG, VOS	-0.3	7	V
Power-good sink current	PG		10	mA
Temperature	Operating junction temperature, T _J	-40	150	°C
	Storage temperature, T _{stg}	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge ⁽¹⁾	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽³⁾	±500	

- (1) ESD testing is performed according to the respective JESD22 JEDEC standard.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V _{IN} (at AVIN and PVIN)			3	17	V
Operating junction temperature, T _J		-40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS6214x	UNIT
		RGT 16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	45	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	53.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	17.4	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	4.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

 over operating junction temperature ($T_J = -40^\circ\text{C}$ to 125°C), typical values at $V_{IN} = 12\text{V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY							
V_{IN}	Input voltage range ⁽¹⁾		3		17	V	
I_Q	Operating quiescent current	EN = High, $I_{OUT} = 0\text{ mA}$, device not switching		17	30	μA	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		17	25		
I_{SD}	Shutdown current ⁽²⁾	EN = Low		1.5	25	μA	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1.5	4		
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage (PWM mode operation)	2.6	2.7	2.8	V	
		Hysteresis		200		mV	
T_{SD}	Thermal shutdown temperature			160		$^\circ\text{C}$	
	Thermal shutdown hysteresis			20			
CONTROL (EN, DEF, FSW, SS/TR, PG)							
V_H	High level input threshold voltage (EN, DEF, FSW)		0.9	0.65		V	
V_L	Low level input threshold voltage (EN, DEF, FSW)			0.45	0.3	V	
I_{LKG}	Input leakage current (EN, DEF, FSW)	EN = V_{IN} or GND; DEF, FSW = V_{OUT} or GND		0.01	1	μA	
V_{TH_PG}	Power-good threshold voltage	Rising (% V_{OUT})	92%	95%	98%		
		Falling (% V_{OUT})	87%	90%	94%		
V_{OL_PG}	Power-good output low voltage	$I_{PG} = -2\text{ mA}$		0.07	0.3	V	
I_{LKG_PG}	Input leakage current (PG)	$V_{PG} = 1.8\text{ V}$		1	400	nA	
$I_{SS/TR}$	SS/TR pin source current		2.3	2.5	2.7	μA	
POWER SWITCH							
$r_{DS(on)}$	High-side MOSFET ON-resistance	$V_{IN} \geq 6\text{ V}$		90	170	$\text{m}\Omega$	
		$V_{IN} = 3\text{ V}$		120			
	Low-side MOSFET ON-resistance	$V_{IN} \geq 6\text{ V}$		40	70	$\text{m}\Omega$	
		$V_{IN} = 3\text{ V}$		50			
I_{LIMF}	High-side MOSFET forward current limit ⁽³⁾	$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$	2.45	3	3.5	A	
OUTPUT							
I_{LKG_FB}	Input leakage current (FB)	TPS62140, $V_{FB} = 0.8\text{ V}$		1	100	nA	
V_{OUT}	Output voltage range (TPS62140)	$V_{IN} \geq V_{OUT}$	0.9		6.0	V	
	DEF (output voltage programming)	DEF = 0 (GND)		V_{OUT}			
		DEF = 1 (V_{OUT})		$V_{OUT} + 5\%$			
	Initial output voltage accuracy ⁽⁴⁾	PWM mode operation, $V_{IN} \geq V_{OUT} + 1\text{ V}$		785.6	800	814.4	mV
		PWM mode operation, $V_{IN} \geq V_{OUT} + 1\text{ V}$, $T_A = -10^\circ\text{C}$ to 85°C		788.0	800	812.8	
		Power-save mode operation, $C_{OUT} = 22\mu\text{F}$		781.6	800	822.4	
	Load regulation ⁽⁵⁾	$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, PWM mode operation		0.05		%/A	
Line regulation ⁽⁵⁾	$3\text{ V} \leq V_{IN} \leq 17\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ A}$, PWM mode operation		0.02		%/V		

(1) The device is still functional down to undervoltage lockout (see parameter V_{UVLO}).

(2) Current into AVIN + PVIN pins

(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see [Current Limit and Short Circuit Protection](#) section).

(4) This is the accuracy provided at the FB pin for the adjustable V_{OUT} version (line and load regulation effects are not included). For the fixed-voltage versions the (internal) resistive divider is included.

(5) Line and load regulation depend on external component selection and layout (see [Figure 22](#) and [Figure 23](#)).

7.6 Typical Characteristics

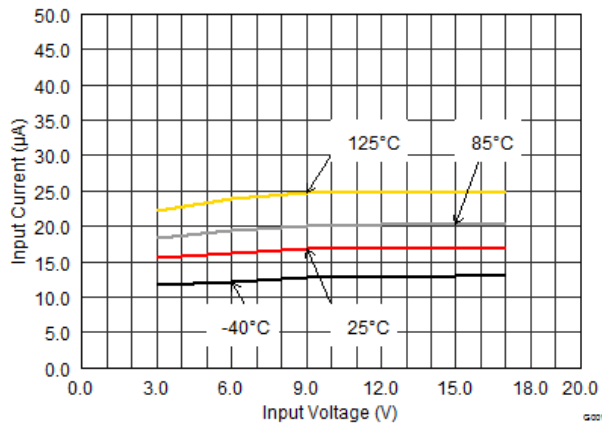


Figure 1. Quiescent Current

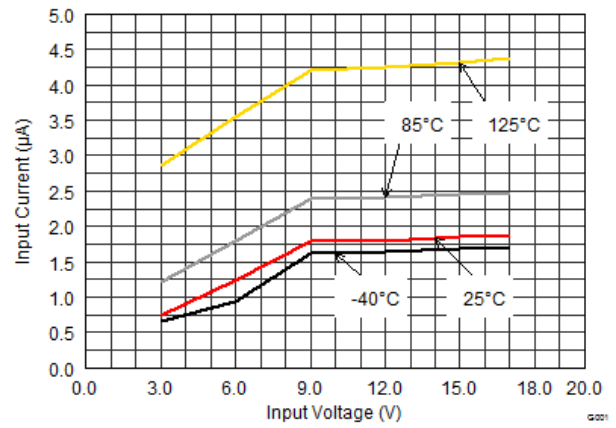


Figure 2. Shutdown Current

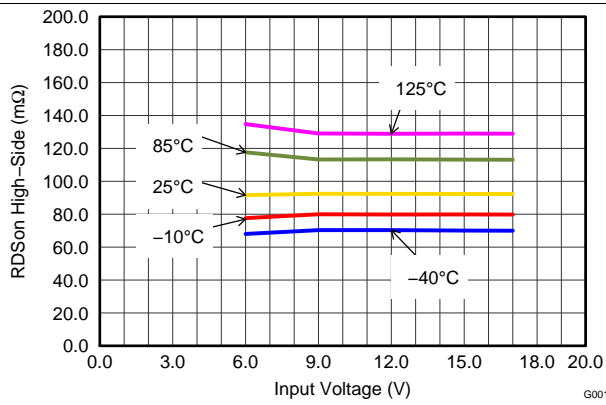


Figure 3. High-Side Switch Resistance

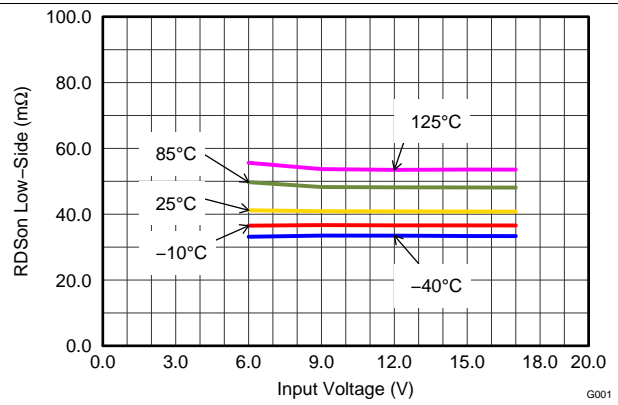


Figure 4. Low-Side Switch Resistance

8 Detailed Description

8.1 Overview

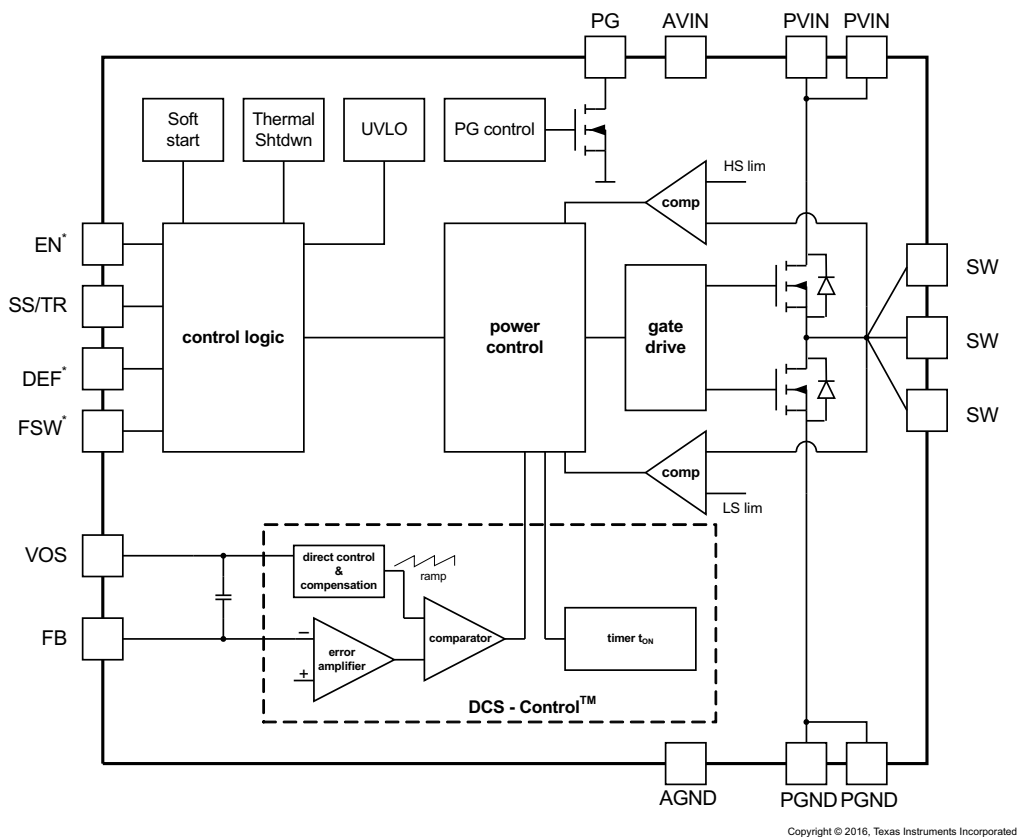
The TPS6214x synchronous switched-mode power converters are based on DCS-Control™ (Direct Control with Seamless Transition into Power-Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an ac loop directly associated with the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

The DCS-Control™ topology supports Pulse Width Modulation (PWM) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz or 1.25MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode, the switching frequency decreases linearly with the load current. Because DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

Fixed output-voltage versions provide the smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 2 A.

The TPS6214x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

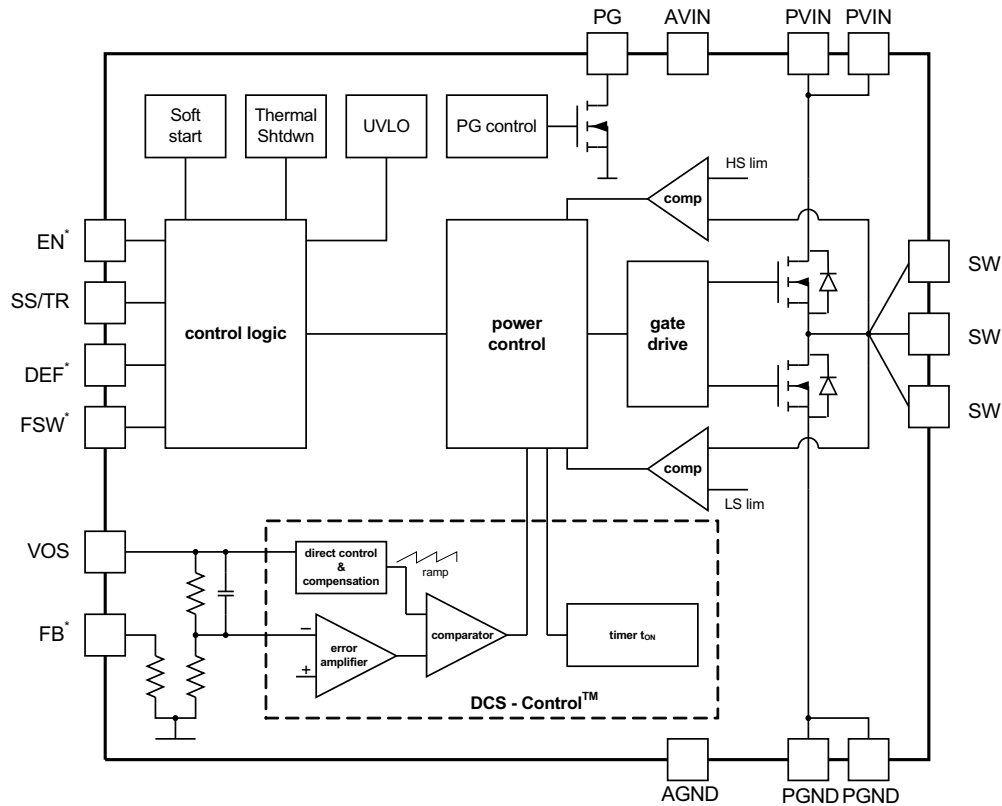
8.2 Functional Block Diagrams



* This pin is connected to a pull down resistor internally (see [Feature Description](#) section)

Figure 5. TPS62140 and TPS62140A (Adjustable Output Voltage)

Functional Block Diagrams (continued)



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* This pin is connected to a pull down resistor internally (see [Feature Description](#) section)

Figure 6. TPS62141/2/3 (Fixed Output Voltage)

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to High or Low. An internal pull-down resistor of about 400kΩ is connected and keeps EN logic low, if Low is set initially and then the pin gets floating. It is disconnected if the pin is set High

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Soft-Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output-voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs, and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See [Figure 40](#) and [Figure 41](#) for typical start-up operation.

Feature Description (continued)

Using a very small capacitor (or leaving SS/TR pin un-connected) provides fastest startup behavior. There is no theoretical limit for the longest startup time. The TPS6214x can start into a pre-biased output. During monotonic pre-biased startup, both the power MOSFETs are not allowed to turn on until the devices internal ramp sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5 V, a reduced current limit of typically 1.6 A is set internally. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage follows this voltage in both directions, up and down (see [Application and Implementation](#)).

8.3.3 Power Good (PG)

The TPS6214x has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic-low level. With TPS62140 it is high-impedance when the device is turned off due to EN, UVLO, or thermal shutdown. TPS62140A features PG=Low in this case and can be used to actively discharge Vout (see [Figure 47](#)). VIN must remain present for the PG pin to stay Low. See [SLVA644](#) for application details. If not used, the PG pin should be connected to GND but may be left floating.

Table 1. Power Good Pin Logic Table (TPS62140)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{SD}$	√	
Power Supply Removal	$V_{IN} < 0.7\text{ V}$	√	

Table 2. Power Good Pin Logic Table (TPS62140A)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\text{ V}$	√	

8.3.4 Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6214x devices can be increased by 5% above the nominal voltage by setting the DEF pin to High ⁽¹⁾. When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6214x can be found in [SLVA489](#). A pull down resistor of about 400 kΩ is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

(1) Maximum allowed voltage is 7 V. Therefore, it is recommended to connect it to VOUT or PG, not VIN.

8.3.5 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High. It is mandatory to start with FSW=Low to limit inrush current, which can be done by connecting to VOUT or PG. Running with lower frequency a higher efficiency, but also a higher output voltage ripple, is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typ.). To get low ripple and full output current at the lower switching frequency, it's recommended to use an inductor of at least 2.2uH. The switching frequency can be changed during operation, if needed. A pull down resistor of about 400kOhm is internally connected to the pin, acting the same way as at the DEF pin (see above).

8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents incorrect operation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ.), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes high-impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

8.4 Device Functional Modes

8.4.1 Pulse-Width Modulation (PWM) Operation

The TPS6214x operates with pulse-width modulation in continuous-conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN} , V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor ripple current. To maintain high efficiency at light loads, the device enters power-save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor ripple current.

8.4.2 Power Save Mode Operation

The TPS6214x enters its built-in power-save mode seamlessly if the load current decreases. This secures a high efficiency in light-load operation. The device remains in power-save mode as long as the inductor current is discontinuous.

In power-save mode, the switching frequency decreases linearly with the load current, maintaining high efficiency. The transition into and out of power-save mode happens within the entire regulation scheme and is seamless in both directions.

TPS6214x includes a fixed-on-time circuit. An estimate for this on-time, in steady-state operation with FSW=Low, is:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \quad (1)$$

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such case. Using t_{ON} , the typical peak inductor current in Power Save Mode can be approximated by:

Device Functional Modes (continued)

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \quad (2)$$

When V_{IN} decreases to typically 15% above V_{OUT} , the TPS6214x does not enter power-save mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by $D = V_{out}/V_{in}$ and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty-cycle operation, turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input-to-output voltage differences, e.g., for longest operation time of battery-powered applications. In 100% duty-cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} (R_{DS(on)} + R_L)$$

where

- I_{OUT} is the output current.
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET.
- R_L is the DC resistance of the inductor used.

(3)

8.4.4 Current Limit and Short Circuit Protection

The TPS6214x devices are protected against heavy load and short-circuit events. If a short circuit is detected (V_{OUT} drops below 0.5 V), the current limit is reduced to 1.6 A, typically. If the output voltage rises above 0.5 V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot through current, then the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 2.4A. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current-limit threshold.

The output current of the device is limited by the current limit (see [Electrical Characteristics](#)). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in the [Electrical Characteristics](#)
- L is the inductor value
- V_L is the voltage across the inductor ($V_{IN} - V_{OUT}$)
- t_{PD} is the internal propagation delay

(4)

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (5)$$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62140 is a switched mode step-down converter, able to convert a 3 V to 17 V input voltage into a 0.9 V to 6 V output voltage, providing up to 2 A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitor, only the TPS62140 (TPS62140A) with an adjustable output voltage needs an additional resistive divider to set the output voltage level.

9.2 Typical Application

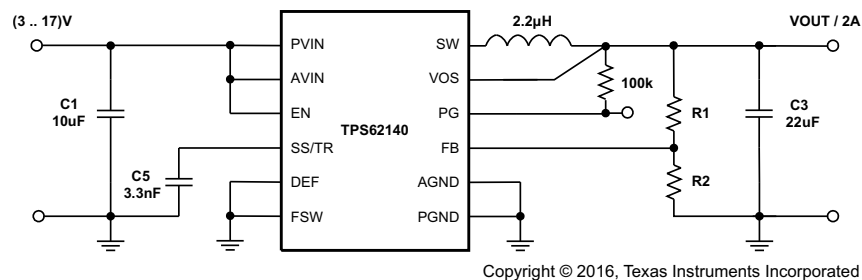


Figure 7. 3.3V/2A Step-Down Converter

9.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions. Using the FSW pin, the design can be optimized for highest efficiency or smallest solution size and lowest output voltage ripple. For highest efficiency set FSW = High and the device operates at the lower switching frequency. For smallest solution size and lowest output voltage ripple set FSW = Low and the device operates with higher switching frequency. The typical values for all measurements are $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$ and $T = 25^\circ\text{C}$, using the external components of [Table 3](#).

9.2.2 Detailed Design Procedure

The component selection used for measurements is given as follows:

Table 3. List of Components⁽¹⁾

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17-V, 2-A step-down converter, QFN	TPS62140RGT, Texas Instruments
L1	2.2- μH , 3.1-A, 0.165 in \times 0.165 in	XFL4020-222MEB, Coilcraft
C1	10- μF , 25-V, ceramic, 1210	Standard
C3	22- μF , 6.3-V, ceramic, 0805	Standard
C5	3300-pF, 25-V, ceramic, 0603	
R1	Dependent on Vout	
R2	Dependent on Vout	
R3	100-k Ω , chip, 0603, 1/16W, 1%	Standard

(1) See [Third-Party Products](#) Disclaimer

9.2.2.1 Programming the Output Voltage

While the output voltage of the TPS62140 (TPS62140A) is adjustable, the TPS62141/2/3 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from [Equation 6](#). It is recommended to choose resistor values which allow a current of at least 2 μ A, meaning the value of R2 should not exceed 400 k Ω . Lower resistor values are recommended for highest accuracy and most-robust design. For applications requiring lowest current consumption, the use of fixed output-voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (6)$$

In case the FB pin is opened, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

9.2.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6214X is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered in conjunction, creating a double pole, responsible for the corner frequency of the converter (see [Output Filter and Loop Stability](#) section). [Table 4](#) can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application. See [SLVA463](#) for details.

Table 4. Recommended LC Output Filter Combinations⁽¹⁾

	4.7 μ F	10 μ F	22 μ F	47 μ F	100 μ F	200 μ F	400 μ F
0.47 μ H							
1 μ H			√	√	√	√	
2.2 μ H		√	√ ⁽²⁾	√	√	√	
3.3 μ H		√	√	√	√		
4.7 μ H							

(1) The values in the table are nominal values. The effective capacitance was considered to vary by +20% and -50%.

(2) This LC combination is the standard value and recommended for most applications.

TPS6214X can be run with an inductor as low as 1 μ H or 2.2 μ H. FSW should be set Low in this case. However, for applications running with the low-frequency setting (FSW = High) or with low input voltages, 3.3 μ H is recommended.

9.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the inductor selected must be rated for appropriate saturation current and DC resistance (DCR). [Equation 7](#) and [Equation 8](#) calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right)$$

where

- $I_L(\max)$ is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- $L(\min)$ is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency

(8)

Calculating the maximum inductor current using the actual operating conditions gives the minimum required inductor saturation current. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6214x and are recommended for use:

Table 5. List of Inductors

TYPE	INDUCTANCE (μH)	CURRENT (A) ⁽¹⁾	DIMENSIONS [L x B x H] (mm)	MANUFACTURER ⁽²⁾
XFL4020-222ME_	2.2 μH , $\pm 20\%$	3.5	4 x 4 x 2.1	Coilcraft
XFL4020-332ME_	3.3 μH , $\pm 20\%$	2.9	4 x 4 x 2.1	Coilcraft
IHLP1212BZ-11	2.2 μH , $\pm 20\%$	3.0	3 x 3.6 x 2	Vishay
IHLP1616AB-11	2.2 μH , $\pm 20\%$	2.75	4.05 x 4.45 x 1.2	Vishay
DEM4518C 1235AS-H-3R3M	3.3 μH , $\pm 20\%$	2.5	4.5 x 4.7 x 1.9	Toko

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

(2) See [Third-Party Products](#) Disclaimer

The inductor value also determines the load current at which the power-save mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L$$

(9)

Using [Equation 8](#), this current level can be adjusted by changing the inductor value.

9.2.2.2.2 Capacitor Selection

9.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22 μF . The architecture of the TPS6214X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output-voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value can have some advantages, like smaller voltage ripple and a tighter DC output accuracy in power-save mode (see [SLVA463](#)).

Note: In power-save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.2.2 Input Capacitor

For most applications, 10 μF is sufficient and is recommended, though a larger value reduces input-current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it is recommended to place a capacitance of 0.1 μF from AVIN to AGND, to avoid potential noise coupling.

9.2.2.2.3 Soft-Start Capacitor

A capacitance connected between the SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant-current source provides 2.5 μA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu\text{A}}{1.25\text{V}} \quad [\text{F}]$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin
 - t_{SS} is the desired soft-start ramp time (s).
- (10)

NOTE

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.3 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin tracks the SS/TR pin voltage as described in [Equation 11](#) and shown in [Figure 8](#).

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \quad (11)$$

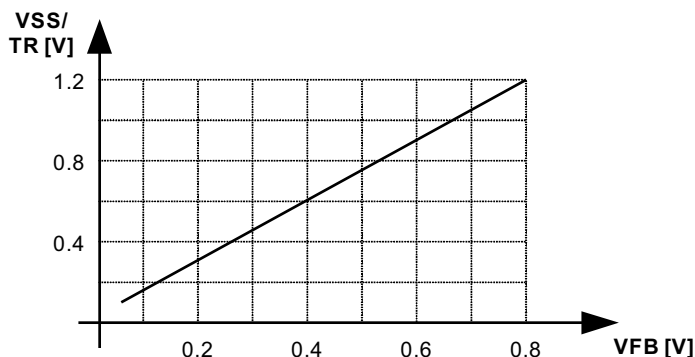
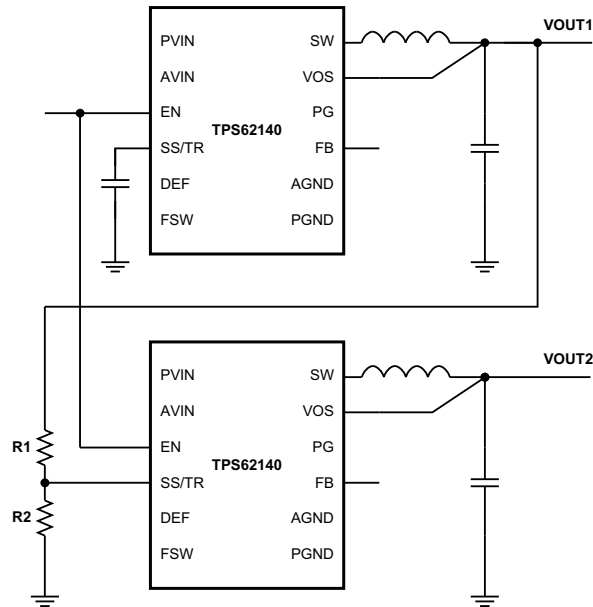


Figure 8. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is $V_{IN}+0.3V$.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. Figure 9 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.



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Figure 9. Sequence for Ratiometric and Simultaneous Startup

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. A ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 10 calculates the soft-start time, though the SS/TR current must be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

9.2.2.4 Output Filter and Loop Stability

The devices of the TPS6214x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with [Equation 12](#):

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (12)$$

Proven nominal values for inductance and ceramic capacitance are given in [Table 4](#) and are recommended for use. Different values may work, but care must be taken on the loop stability, which is affected. More information including a detailed L-C stability matrix can be found in [SLVA463](#).

The TPS6214x devices, both fixed and adjustable versions, include an internal 25 pF feed-forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equations [Equation 13](#) and [Equation 14](#):

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25 pF} \quad (13)$$

$$f_{pole} = \frac{1}{2\pi \cdot 25 pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \quad (14)$$

Though the TPS6214x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power-save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability vs transient response can be found in [SLVA289](#) and [SLVA466](#).

9.2.3 Application Curves

$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, (unless otherwise noted)

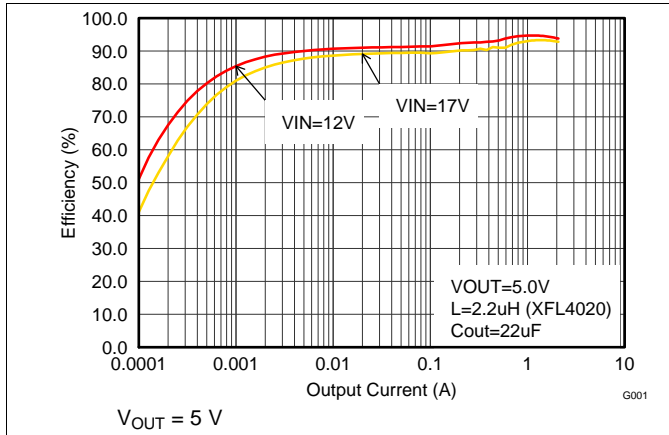


Figure 10. Efficiency With 1.25 MHz

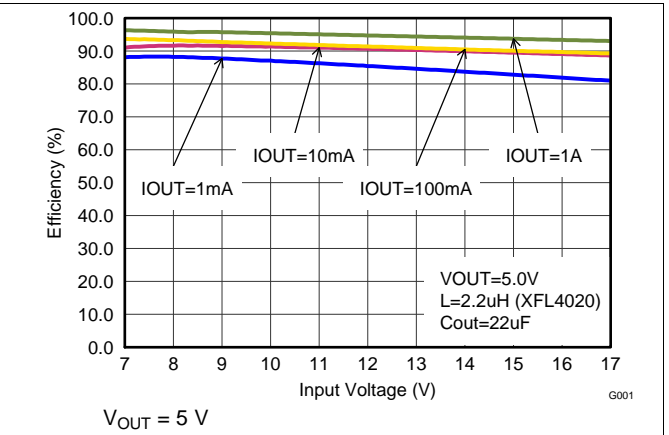


Figure 11. Efficiency With 1.25 MHz

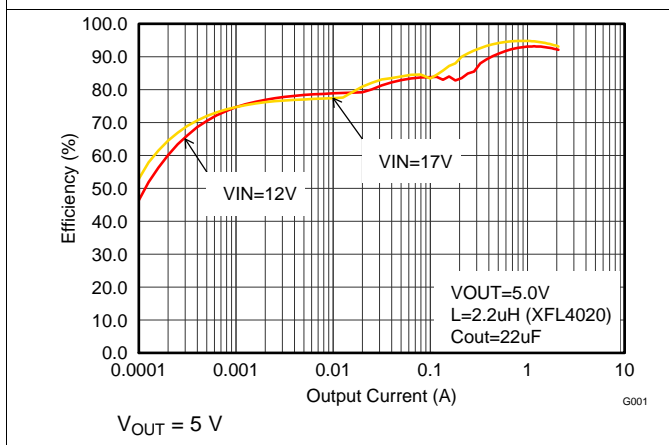


Figure 12. Efficiency With 2.5 MHz

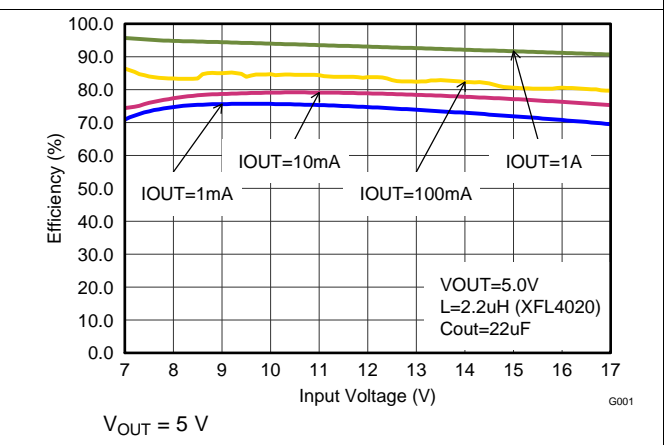


Figure 13. Efficiency With 2.5 MHz

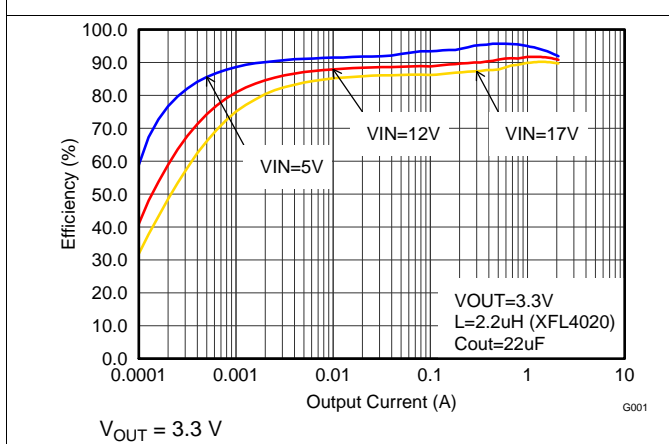


Figure 14. Efficiency With 1.25 MHz

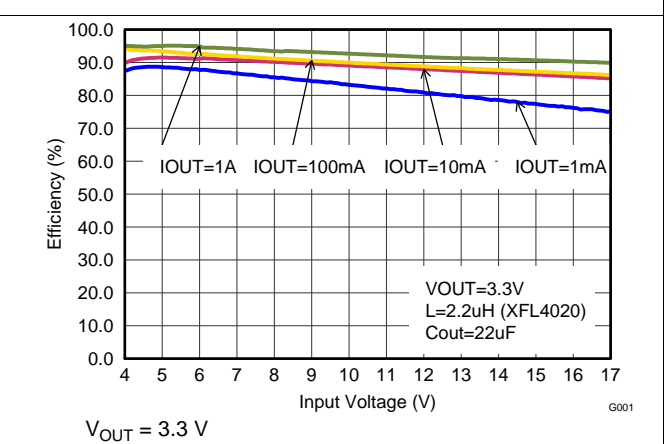


Figure 15. Efficiency With 1.25 MHz

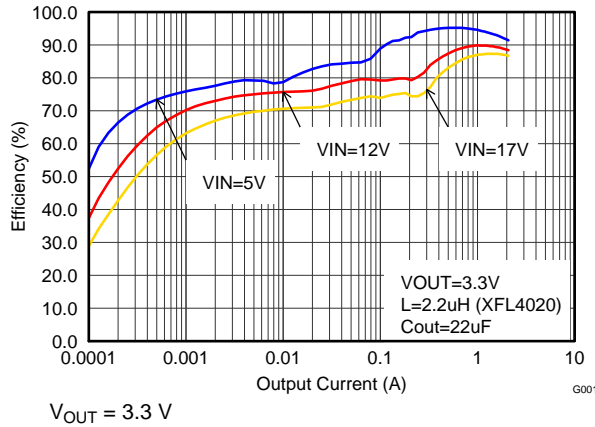


Figure 16. Efficiency With 2.5 MHz,

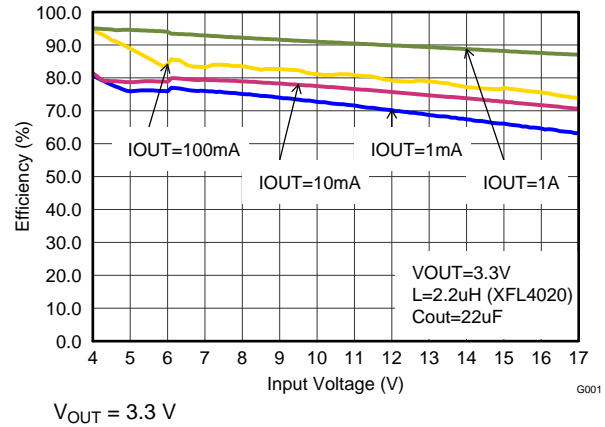


Figure 17. Efficiency With 2.5 MHz

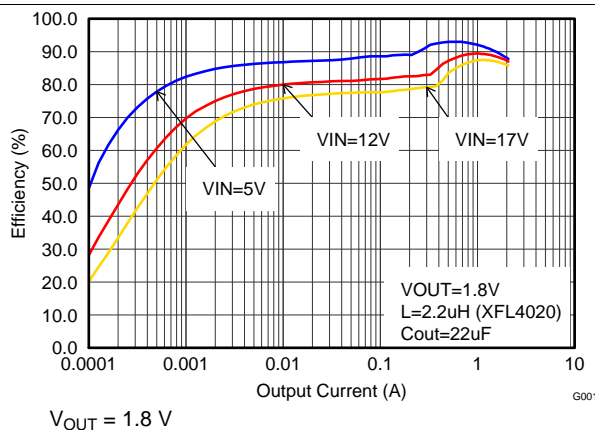


Figure 18. Efficiency With 1.25 MHz

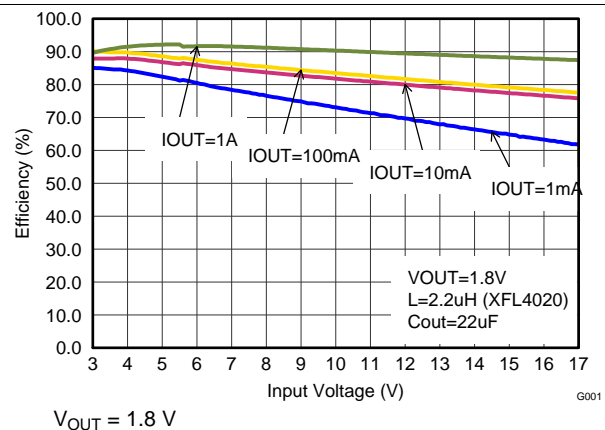


Figure 19. Efficiency With 1.25 MHz

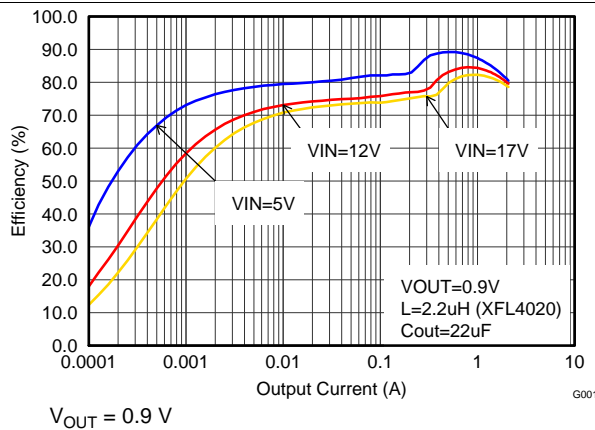


Figure 20. Efficiency With 1.25 MHz

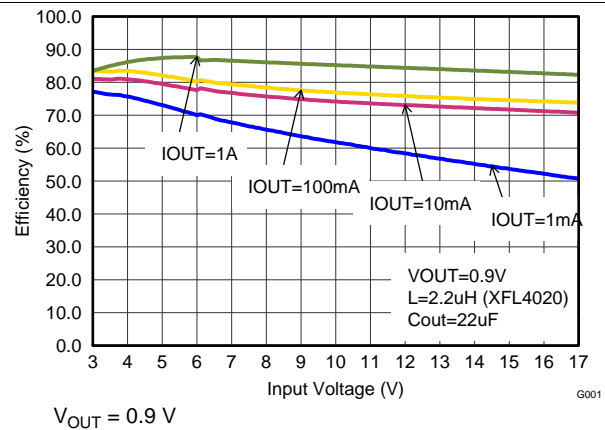


Figure 21. Efficiency With 1.25 MHz

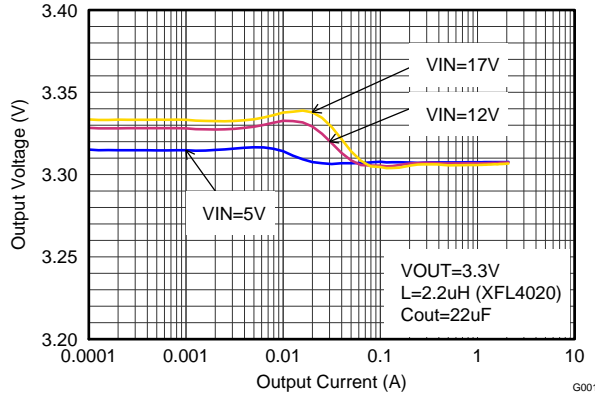


Figure 22. Output Voltage Accuracy (Load Regulation)

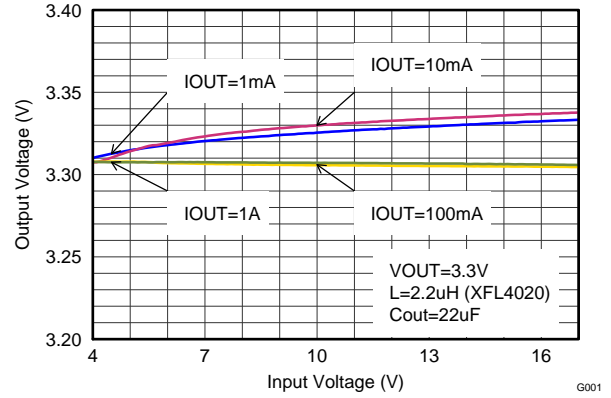


Figure 23. Output Voltage Accuracy (Line Regulation)

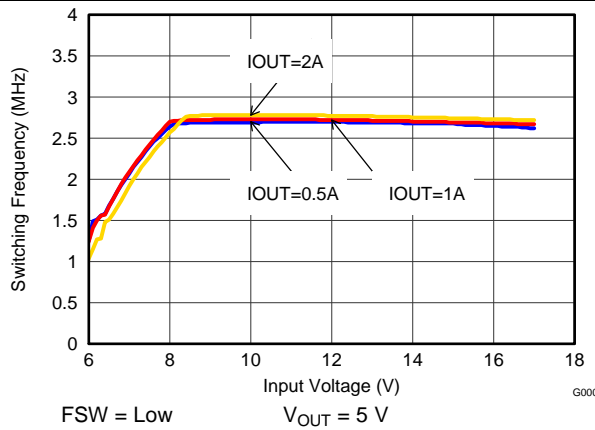


Figure 24. Switching Frequency vs Input Voltage

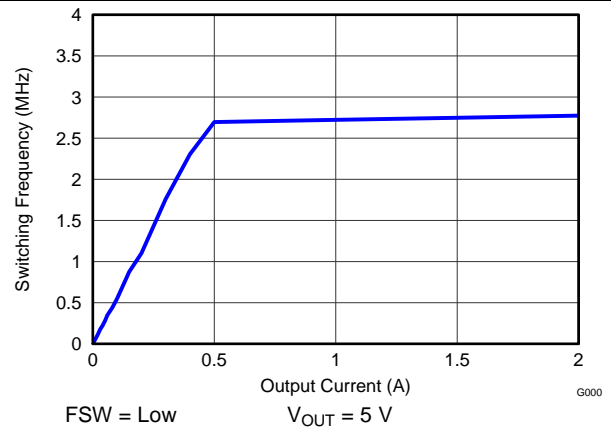


Figure 25. Switching Frequency vs Output Current

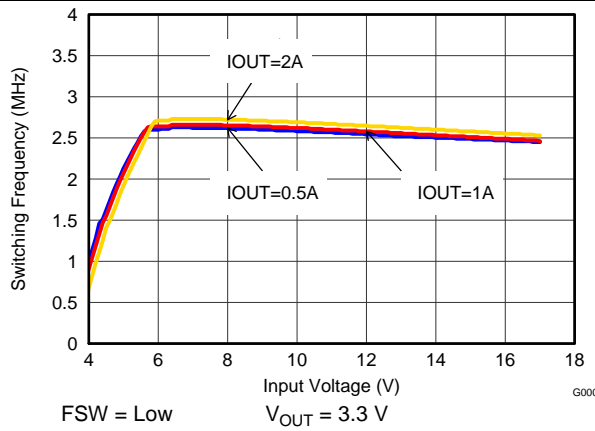


Figure 26. Switching Frequency vs Input Voltage

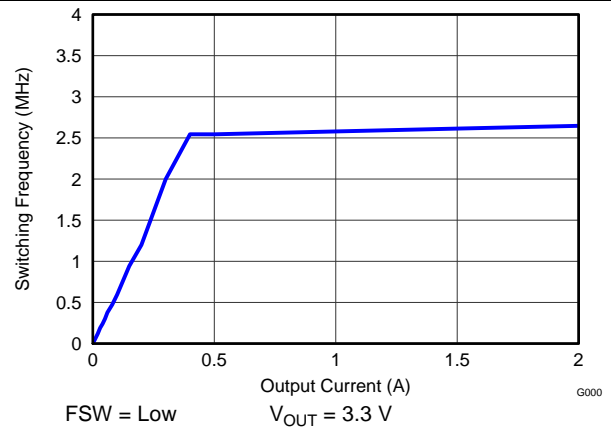


Figure 27. Switching Frequency vs Output Current

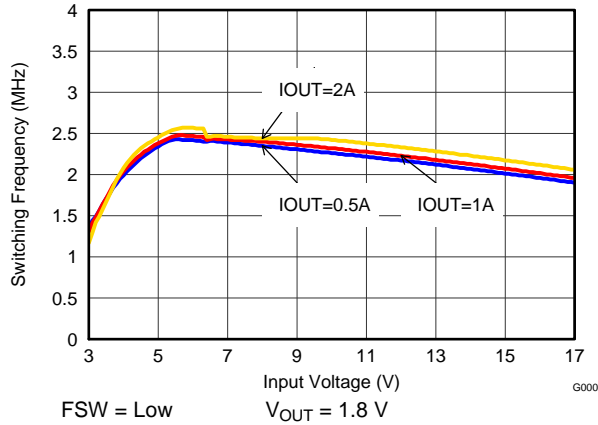


Figure 28. Switching Frequency vs Input Voltage

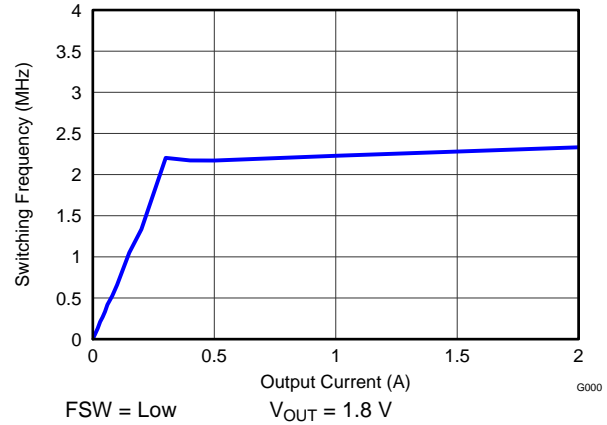


Figure 29. Switching Frequency vs Output Current

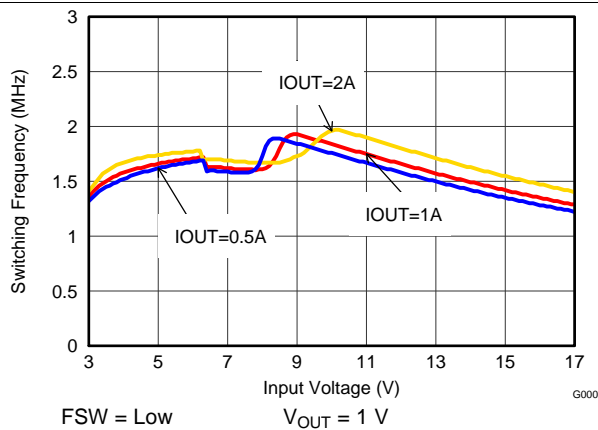


Figure 30. Switching Frequency vs Input Voltage

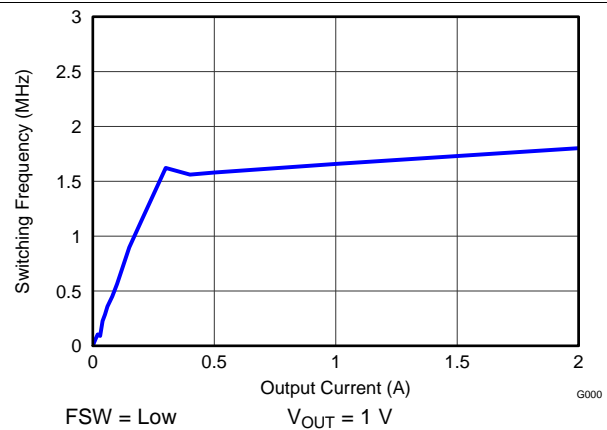


Figure 31. Switching Frequency vs Output Current

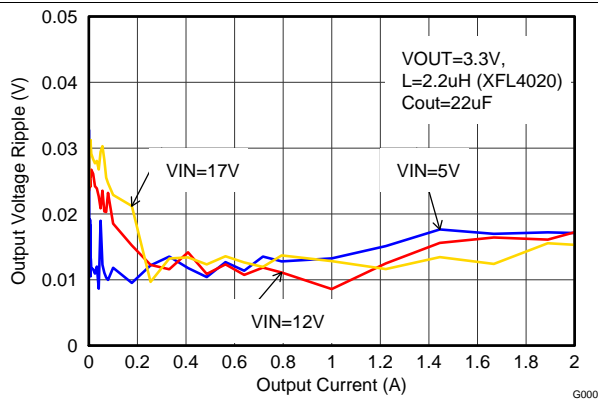


Figure 32. Output Voltage Ripple

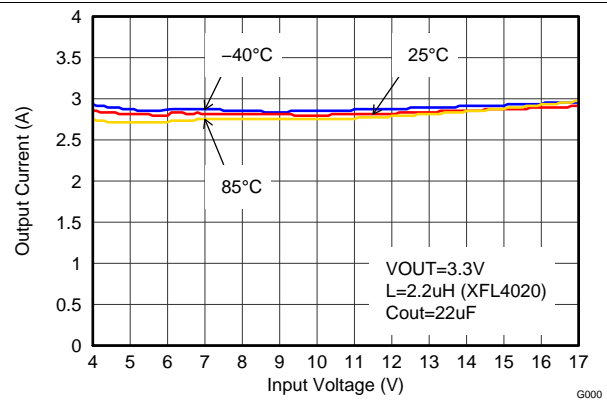


Figure 33. Maximum Output Current

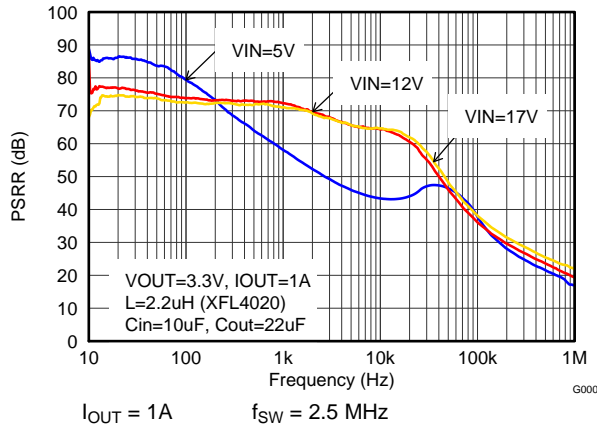


Figure 34. Power-Supply Rejection Ratio

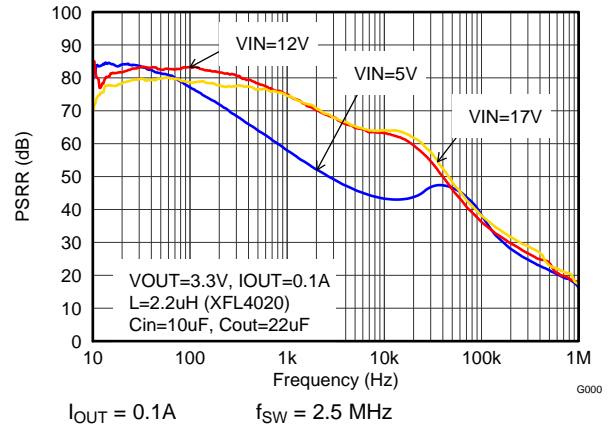
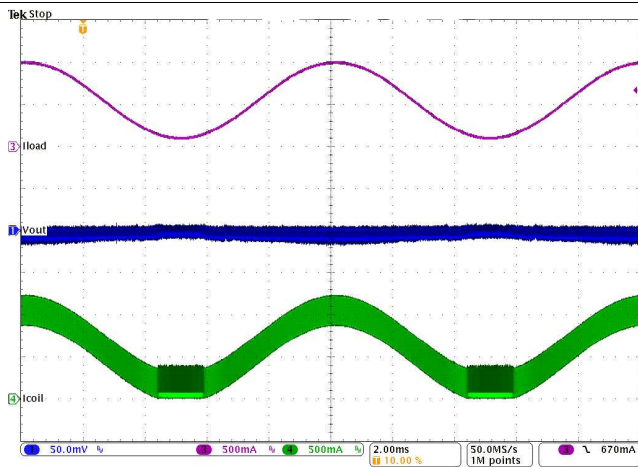
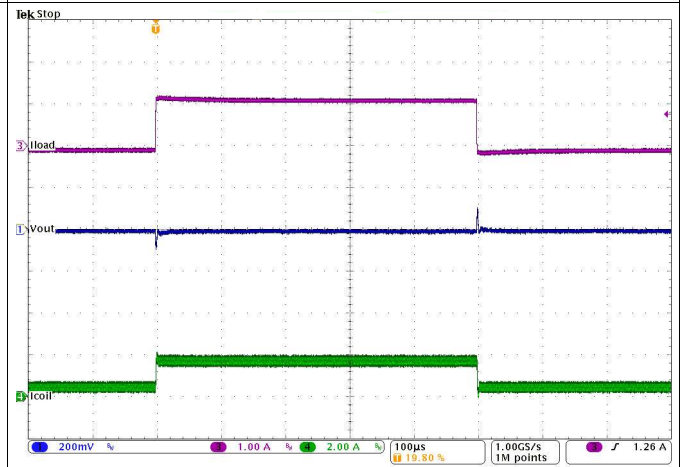


Figure 35. Power-Supply Rejection Ratio



$V_{IN} = 12\text{ V}$ $V_{OUT} = 3.3\text{ V}$ With 50 mV/div

Figure 36. PWM-PSM-Transition



$I_{OUT} = 0.5\text{ to }2\text{ to }0.5\text{ A}$ $V_{IN} = 12\text{ V}$ $V_{OUT} = 3.3\text{ V}$

Figure 37. Load Transient Response

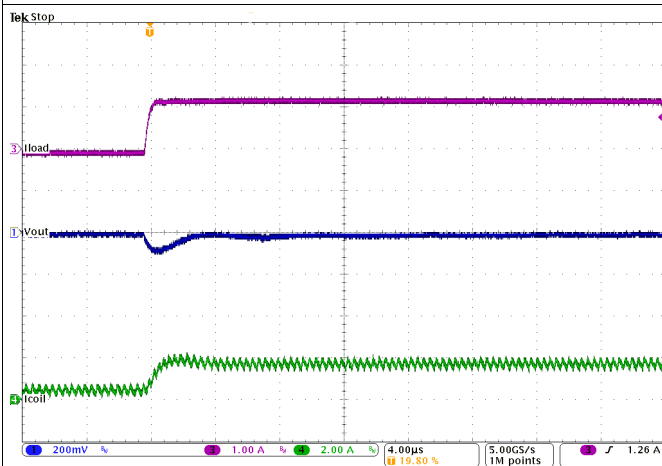
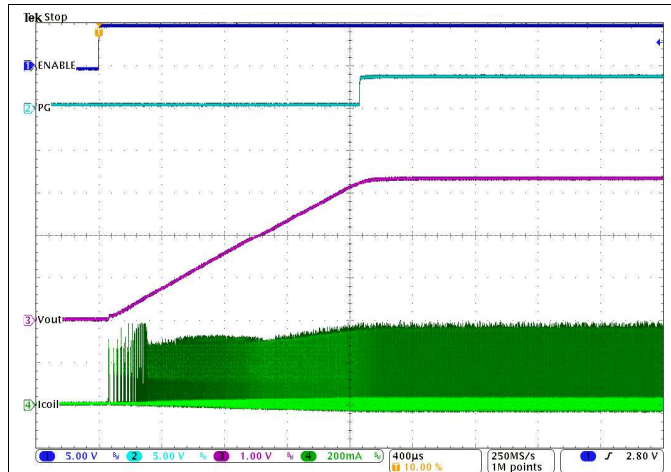


Figure 38. Line Transient Response of Figure 37, Rising Edge

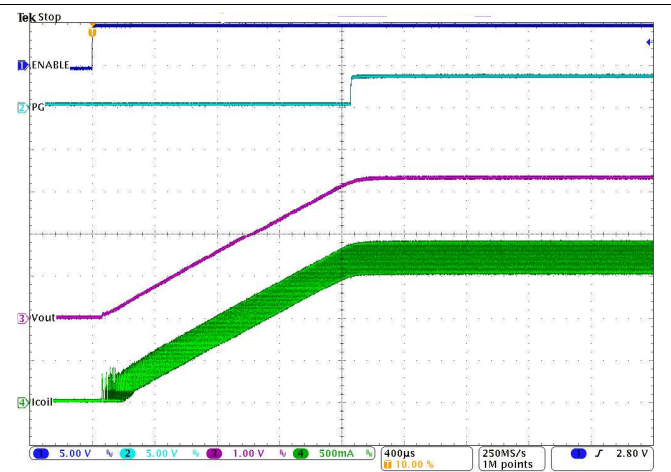


Figure 39. Line Transient Response of Figure 37, Falling Edge



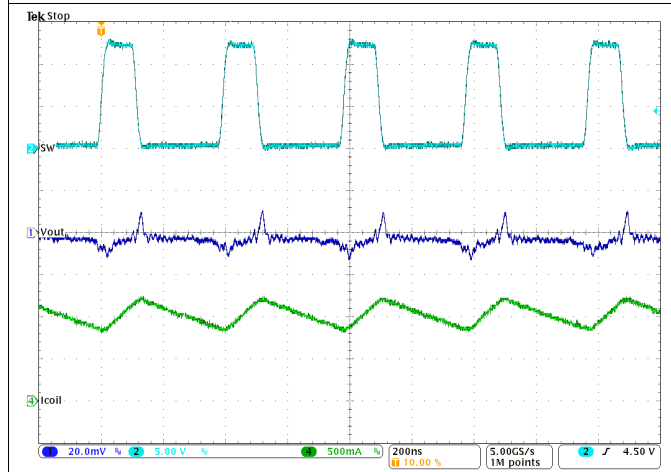
$V_{IN} = 12\text{ V}$ $V_{OUT} = 3.3\text{ V}$

Figure 40. Start-Up Into 100 mA



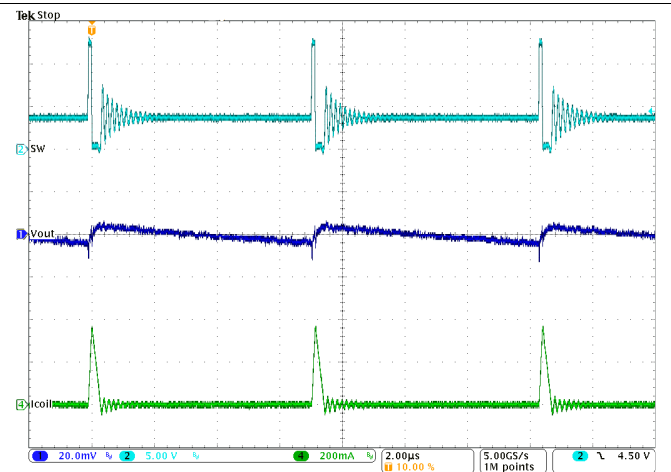
$V_{IN} = 12\text{ V}$ $V_{OUT} = 3.3\text{ V}$

Figure 41. Start-Up into 2 A



$I_{OUT} = 1\text{ A}$

Figure 42. Typical Operation in PWM Mode



$I_{OUT} = 10\text{ A}$

Figure 43. Typical Operation in Power-Save Mode

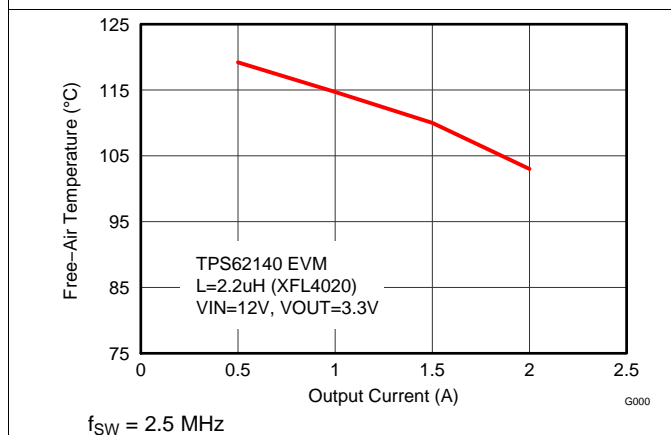


Figure 44. Maximum Ambient Temperature

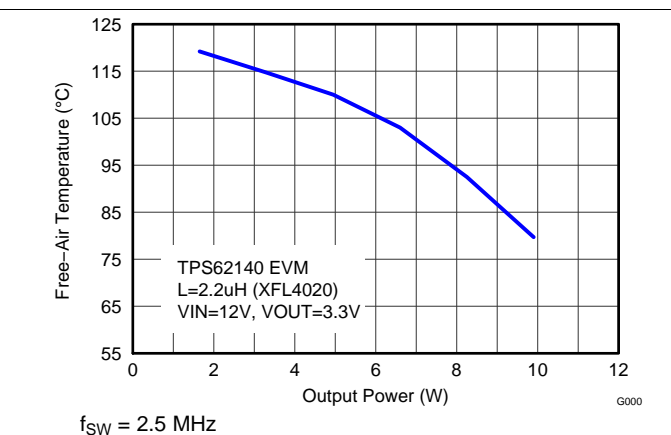
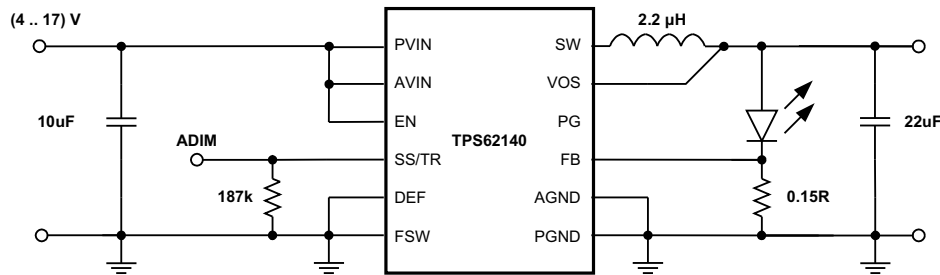


Figure 45. Maximum Ambient Temperature

9.3 System Examples

9.3.1 LED Power Supply

The TPS62140 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Because this pin provides 2.5 μA , the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62140. Figure 46 shows an application circuit, tested with analog dimming:



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Figure 46. Single Power LED Supply

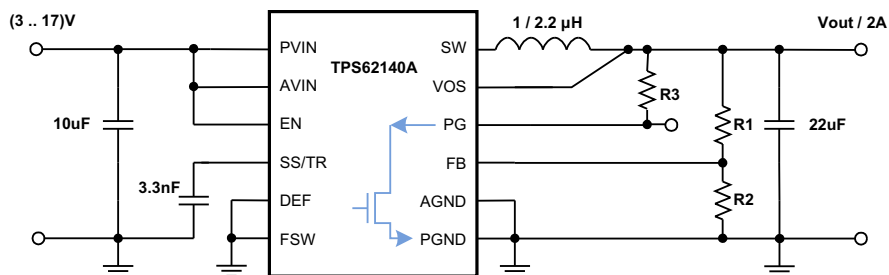
The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \cdot 2.5\mu\text{A} \cdot R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage must be rated according to the forward voltage needed by the LED used. More information is available in the application note SLVA451.

9.3.2 Active Output Discharge

The TPS62140A pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to Vout through a resistor can be used to discharge Vout in those cases (see Figure 47). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10mA.



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Figure 47. Discharge Vout through PG Pin With TPS62140A

System Examples (continued)

9.3.3 Inverting Power Supply

The TPS6214x can be used as inverting power supply by rearranging external circuitry as shown in Figure 48. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17V (see Equation 16).

$$V_{IN} + |V_{OUT}| \leq V_{INmax} \quad (16)$$

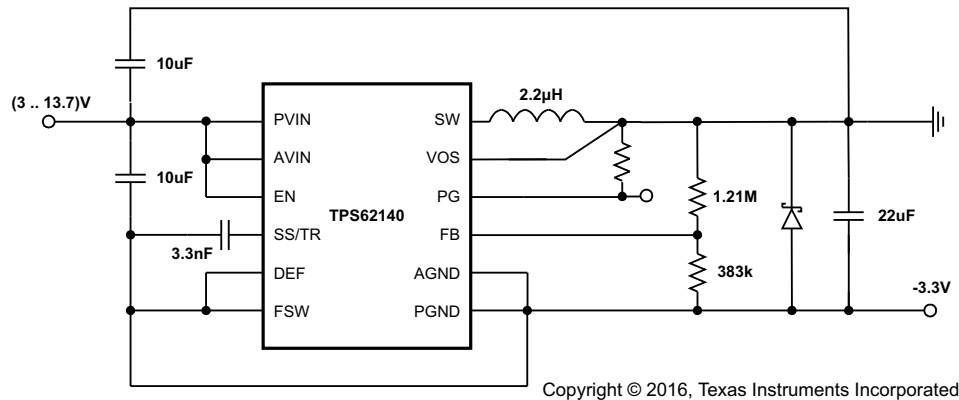


Figure 48. -3.3V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22µF is recommended. A detailed design example is given in [SLVA469](#).

9.3.4 Various Output Voltages

The following example circuits show how to use the various devices and configure the external circuitry to furnish different output voltages at 2A.

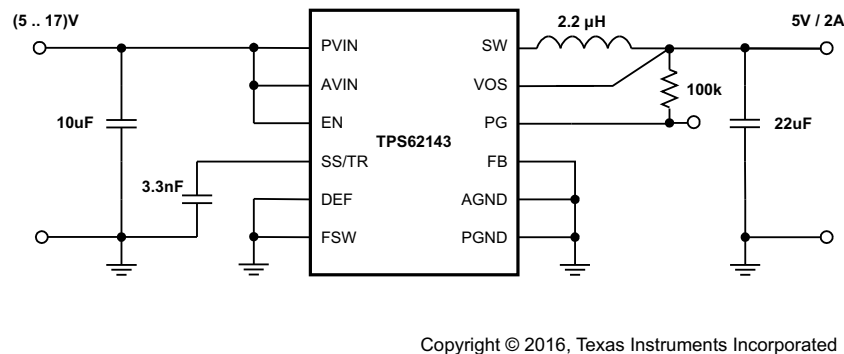
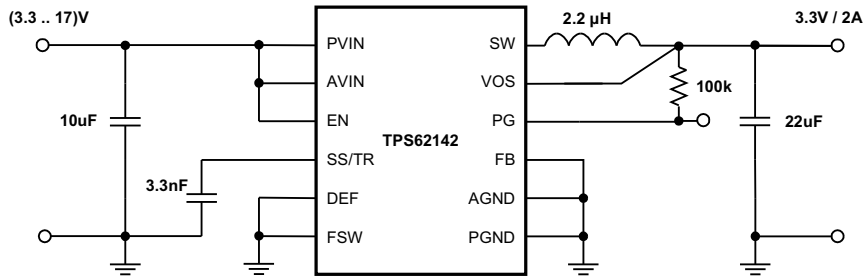


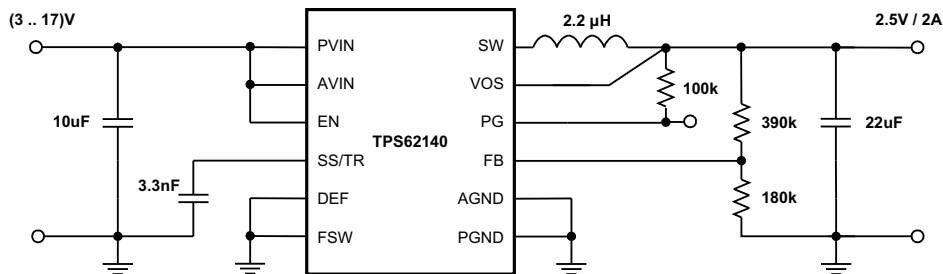
Figure 49. 5-V/2-A Power Supply

System Examples (continued)



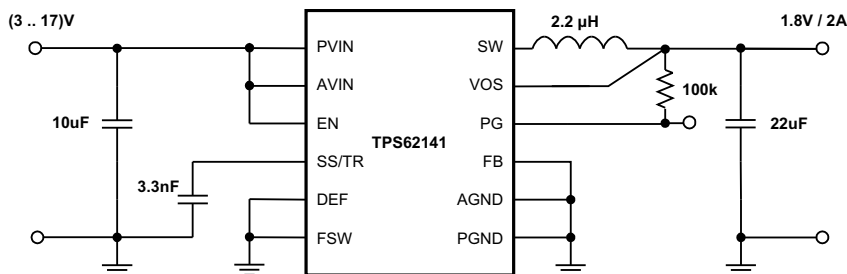
Copyright © 2016, Texas Instruments Incorporated

Figure 50. 3.3-V/2-A Power Supply



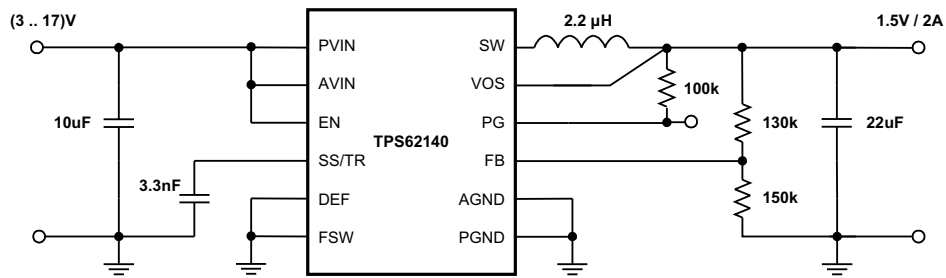
Copyright © 2016, Texas Instruments Incorporated

Figure 51. 2.5-V/2-A Power Supply

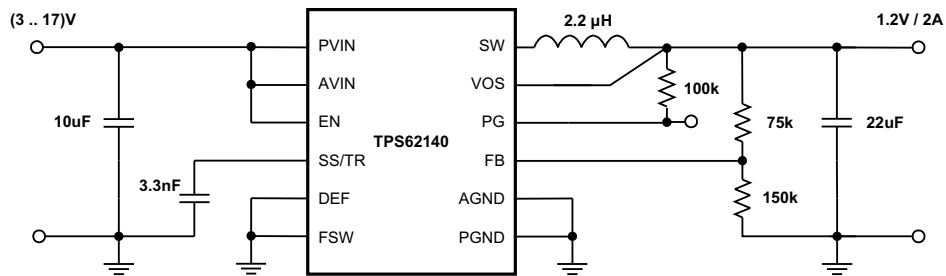


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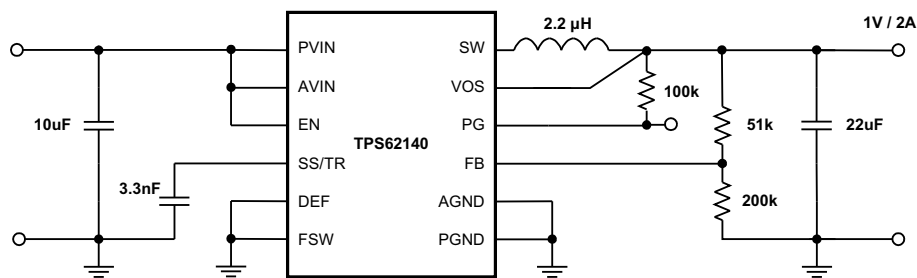
Figure 52. 1.8-V/2-A Power Supply

System Examples (continued)


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Figure 53. 1.5-V/2-A Power Supply


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Figure 54. 1.2-V/2-A Power Supply


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Figure 55. 1-V/2-A Power Supply

10 Power Supply Recommendations

The TPS6214X are designed to operate from a 3-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched-mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6214x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

See [Figure 56](#) for the recommended layout of the TPS6214x, which is designed for common external ground connections. Therefore both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to VOUT at the output capacitor. To avoid noise coupling into the VOS line, this connection should be separated from the VOUT power line/plane as shown in [Layout Example](#).

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (that is, SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, [SLVU437](#). Additionally, the EVM Gerber data are available for download here, [SLVC394](#).

11.2 Layout Example

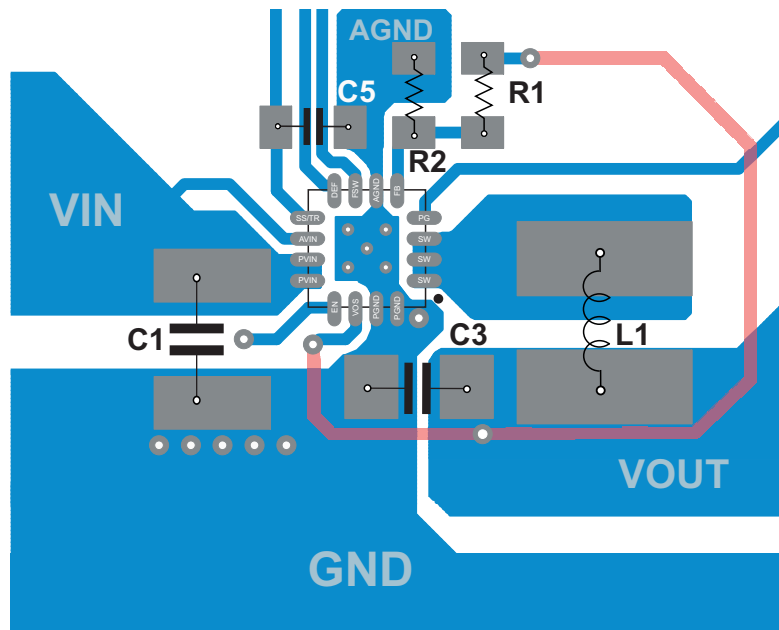


Figure 56. Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note ([SZZA017](#)), and ([SPRA953](#)).

The TPS6214X is designed for a maximum operating junction temperature (T_J) of 125°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Since the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get improved thermal behavior, it is recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short-circuit or overload conditions are present, the device is protected by limiting internal power dissipation. Experimental data, taken from the TPS62140 EVM, shows the maximum ambient temperature (without additional cooling like airflow or heat sink), that can be allowed to limit the junction temperature to at most 125°C (see [Figure 44](#)).

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Users Guide, [SLVU437](#)
- EVM Gerber Data, [SLVC394](#)
- Thermal Characteristics Application Note, [SZZA017](#) and [SPRA953](#)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62140	Click here	Click here	Click here	Click here	Click here
TPS62140A	Click here	Click here	Click here	Click here	Click here
TPS62141	Click here	Click here	Click here	Click here	Click here
TPS62142	Click here	Click here	Click here	Click here	Click here
TPS62143	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62140ARGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA7I	Samples
TPS62140ARGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA7I	Samples
TPS62140RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTZ	Samples
TPS62140RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTZ	Samples
TPS62141RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWA	Samples
TPS62141RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWA	Samples
TPS62142RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWB	Samples
TPS62142RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWB	Samples
TPS62143RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWC	Samples
TPS62143RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

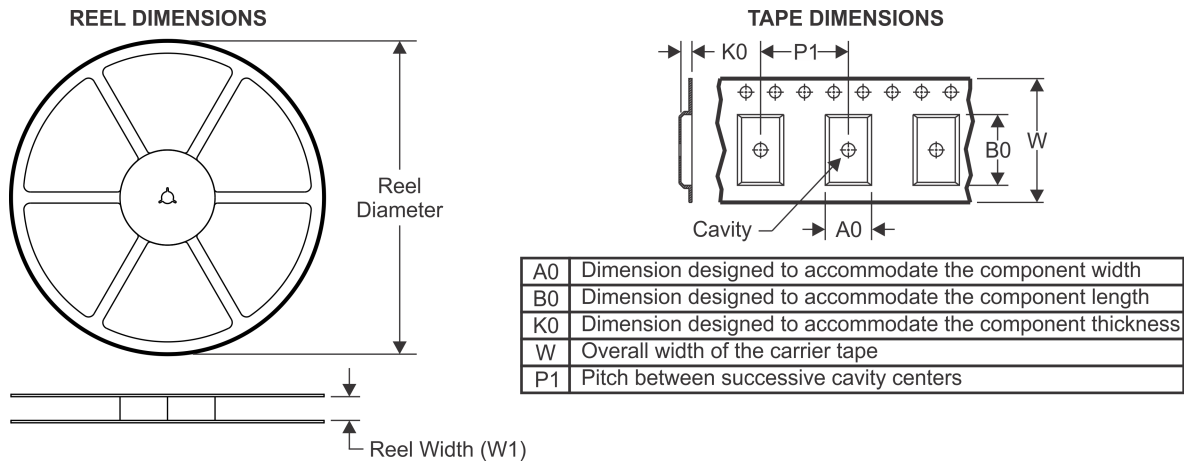
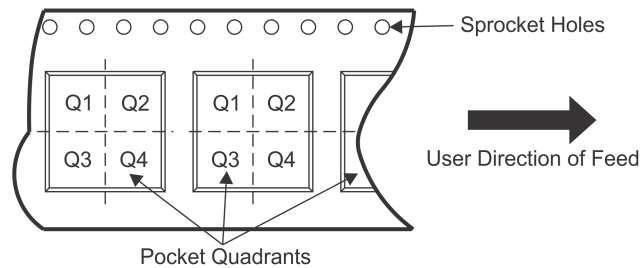
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

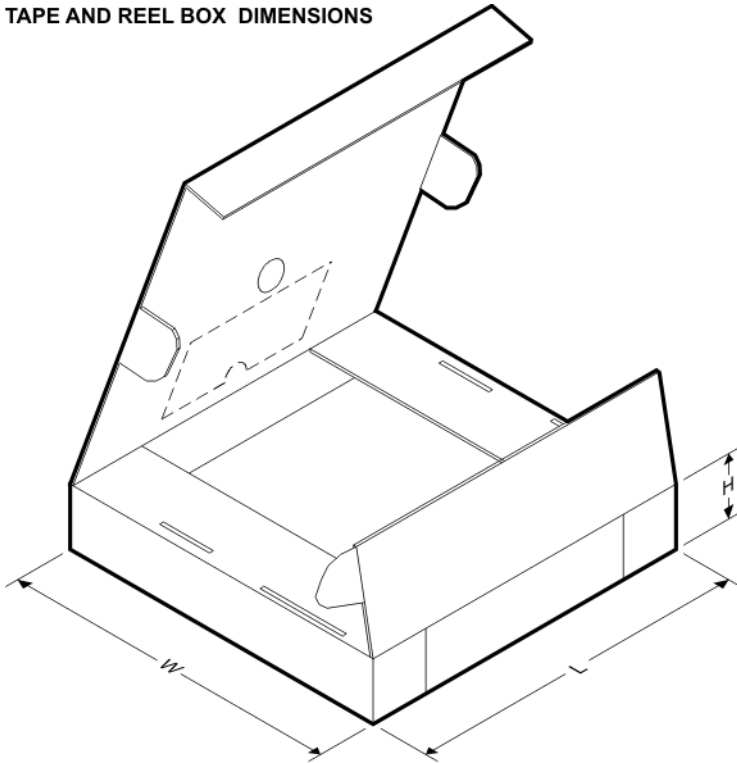
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62140ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

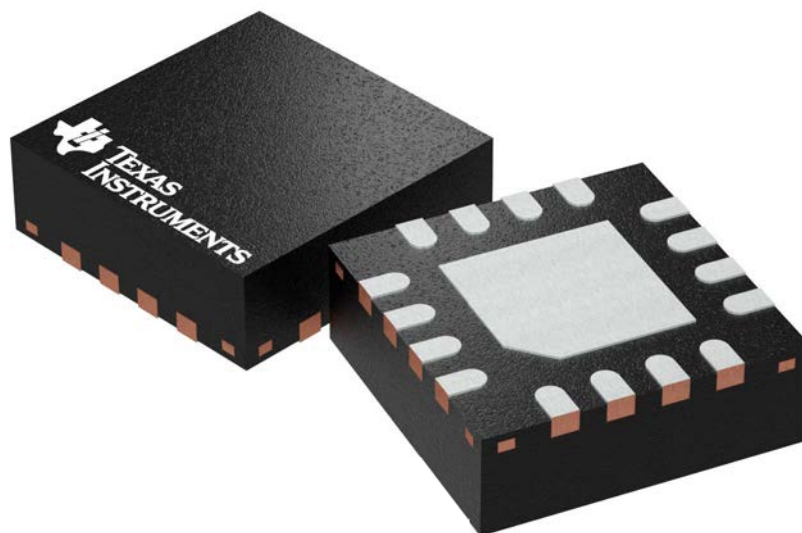
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62140ARGTR	VQFN	RGT	16	3000	552.0	367.0	36.0
TPS62140ARGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62140RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62140RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62141RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62141RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62142RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62142RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62143RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62143RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16

GENERIC PACKAGE VIEW

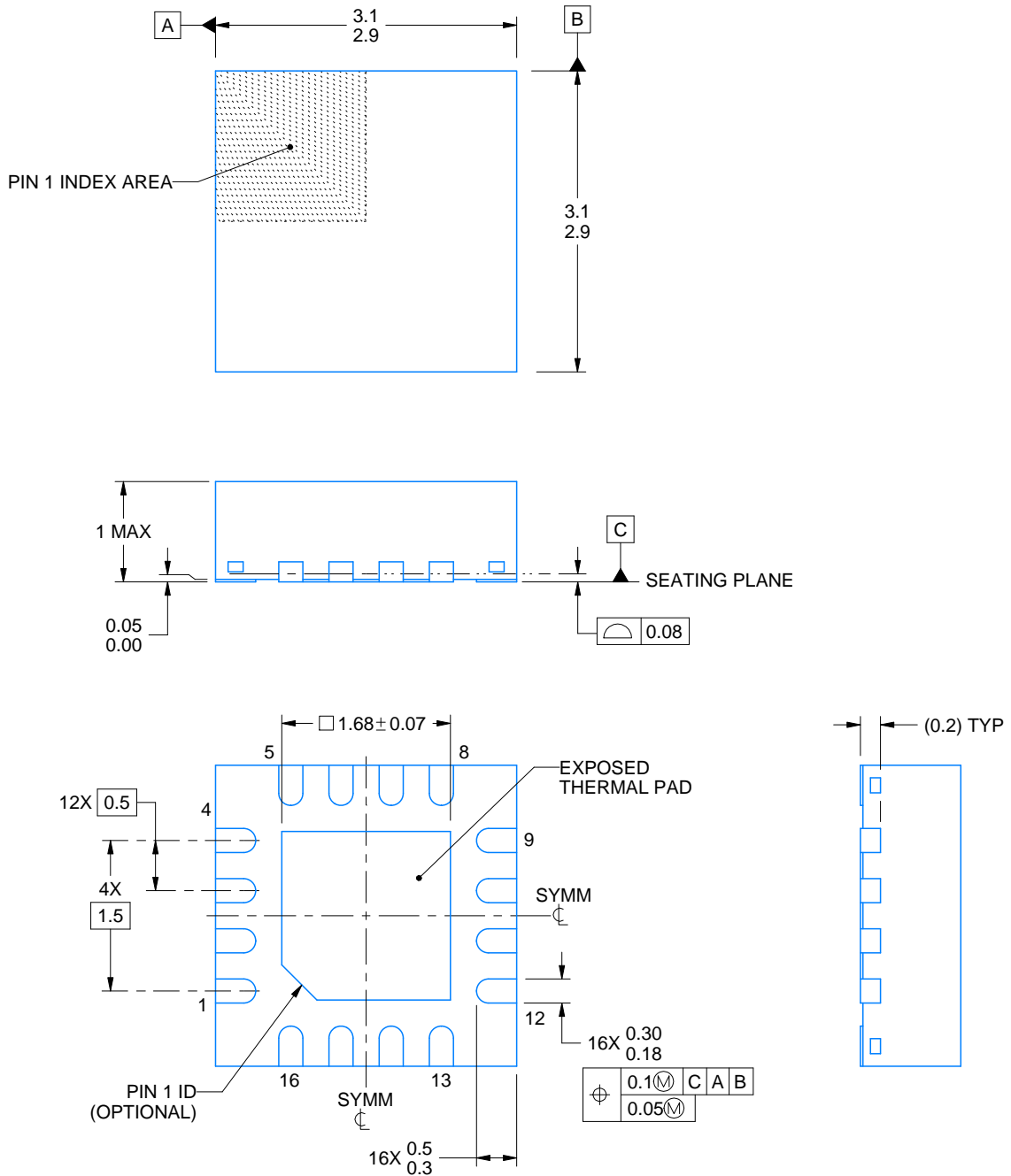
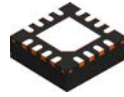
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



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NOTES:

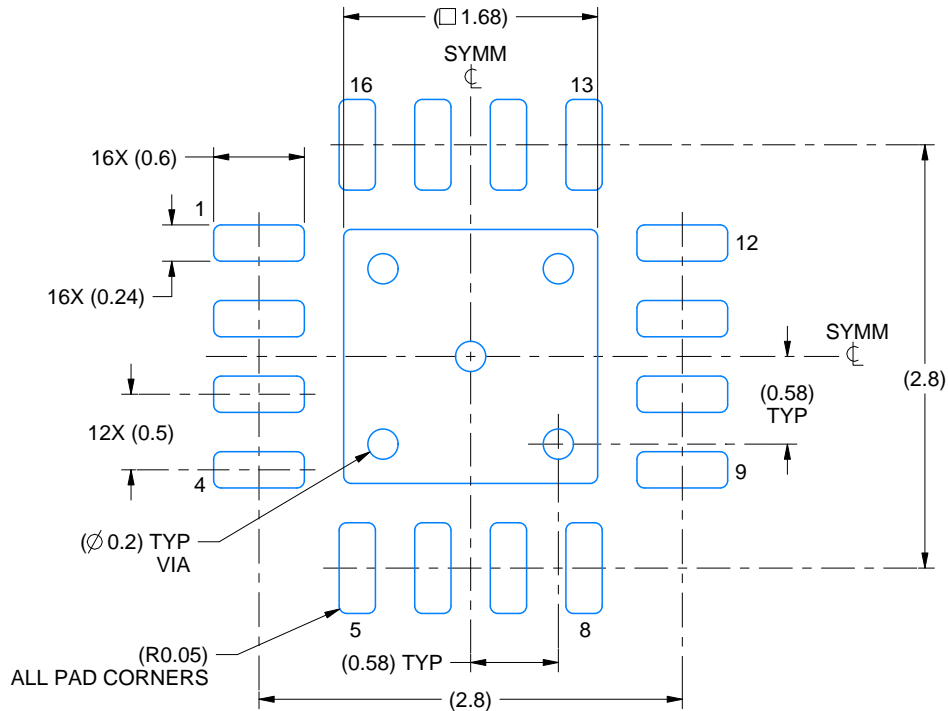
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

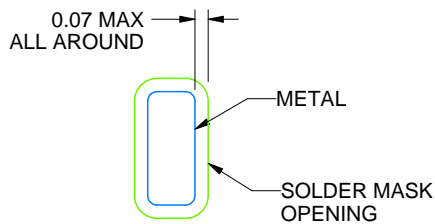
RGT0016C

VQFN - 1 mm max height

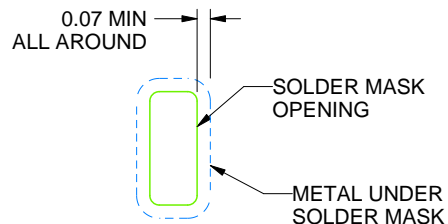
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

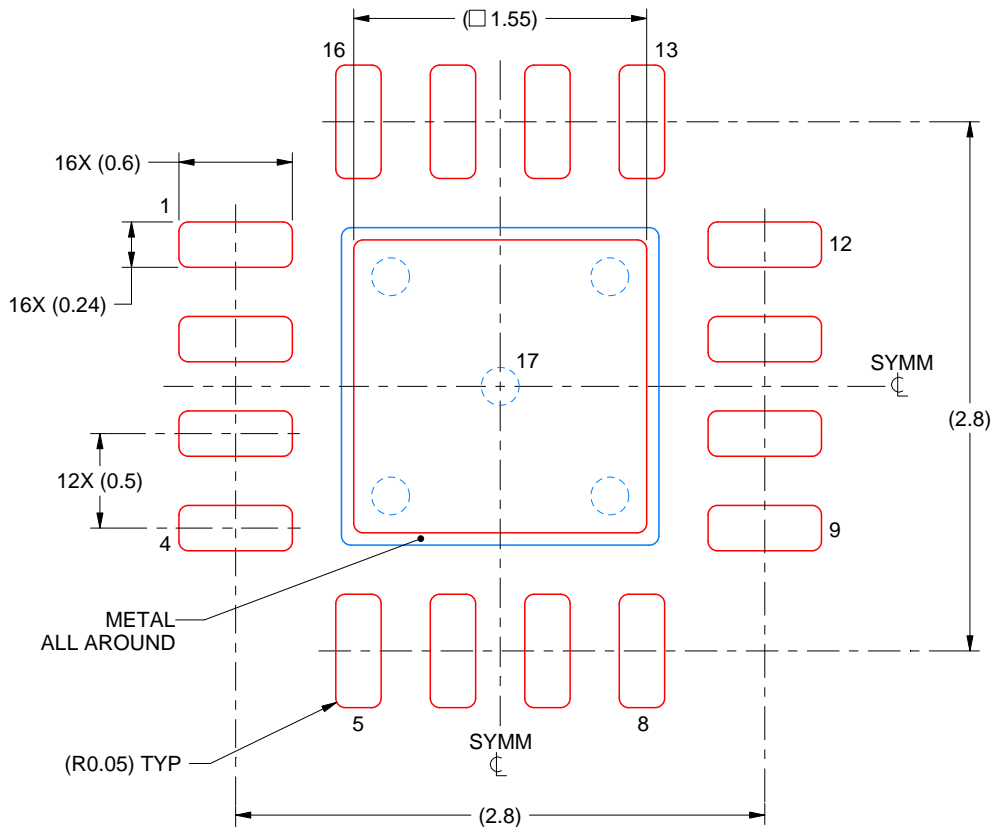
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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-  Excess Inventory Management