



# THE DATASHEET OF STL42P4LLF6



## P-channel 40 V, 0.0155 $\Omega$ typ., 42 A, STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

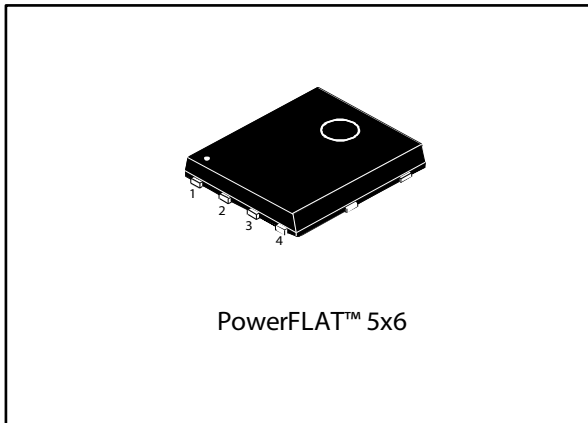
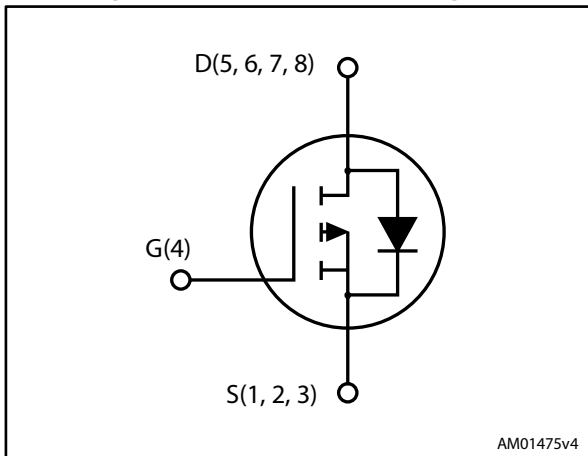


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL42P4LLF6	40 V	0.018 $\Omega$	42 A	75 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.


-  For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL42P4LLF6	42P4LLF6	PowerFLAT™ 5x6	Tape and reel

**Contents**

**1 Electrical ratings ..... 3**

**2 Electrical characteristics ..... 4**

    2.1 Electrical characteristics (curves)..... 6

**3 Test circuits ..... 8**

**4 Package mechanical data ..... 9**

    4.1 PowerFLAT™ 5x6 type R package information ..... 9

    4.2 PowerFLAT™ 5x6 packing information..... 11

**5 Revision history ..... 13**

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	42	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	29	A
$I_D^{(1)(3)}$	Drain current (pulsed)	168	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	7.5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	40	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	75	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Maximum junction temperature	175	$^\circ\text{C}$

**Notes:**

<sup>(1)</sup>The value is limited by  $R_{thj-case}$ .

<sup>(2)</sup>The value is limited by  $R_{thj-pcb}$ .

<sup>(3)</sup>Pulse width is limited by safe operating area.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.00	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	$^\circ\text{C/W}$

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu, steady state



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$		0.0105	0.018	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 5\text{ A}$		0.021	0.026	

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	2850	-	pF
$C_{oss}$	Output capacitance		-	270	-	pF
$C_{riss}$	Reverse transfer capacitance		-	180	-	pF
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 10\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 14: "Gate charge test circuit"</a> )	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	9.4	-	nC
$Q_{gd}$	Gate-drain charge		-	7.3	-	nC
$R_G$	Gate input resistance	$I_D = 0\text{ A}$ , gate DC bias = $0\text{ V}$ , $f = 1\text{ MHz}$ , magnitude of alternative signal = $20\text{ mV}$	-	1.4	-	$\Omega$

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 5\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Switching times test circuit for resistive load"</a> )	-	43	-	ns
$t_r$	Rise time		-	47	-	ns
$t_{d(off)}$	Turn-off-delay time		-	148	-	ns
$t_f$	Fall time		-	19	-	ns



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 5 \text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 32 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	26		ns
$Q_{rr}$	Reverse recovery charge		-	21		nC
$I_{RRM}$	Reverse recovery current		-	1.7		A

**Notes:**

<sup>(1)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2.1 Electrical characteristics (curves)

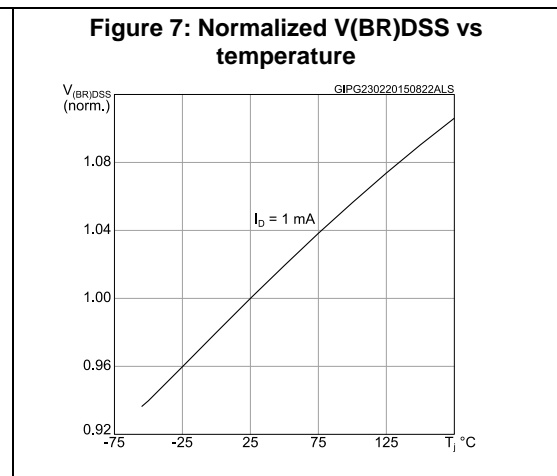
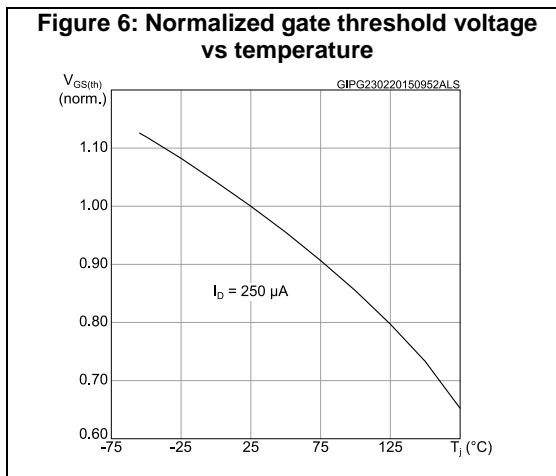
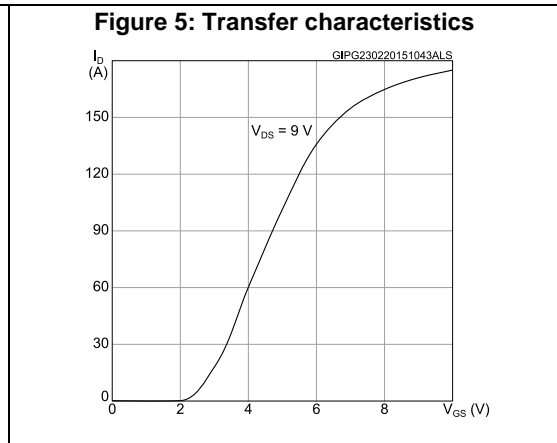
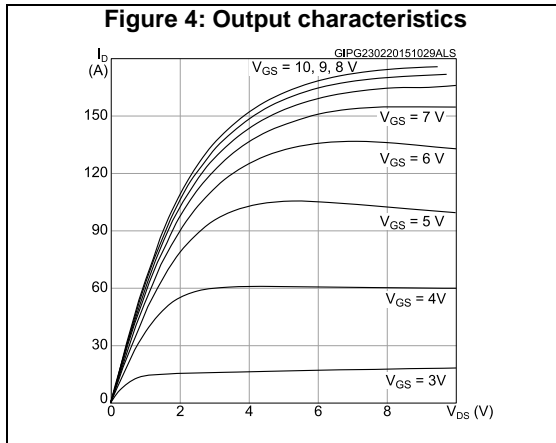
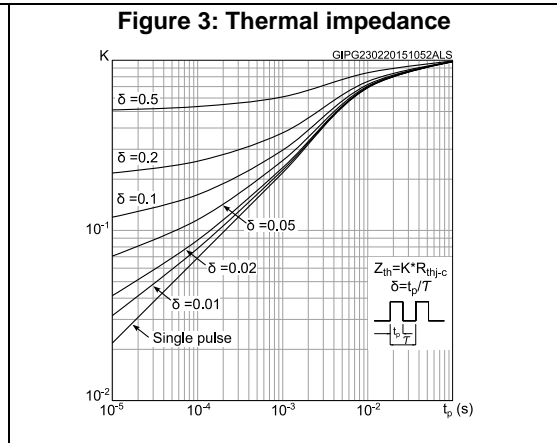
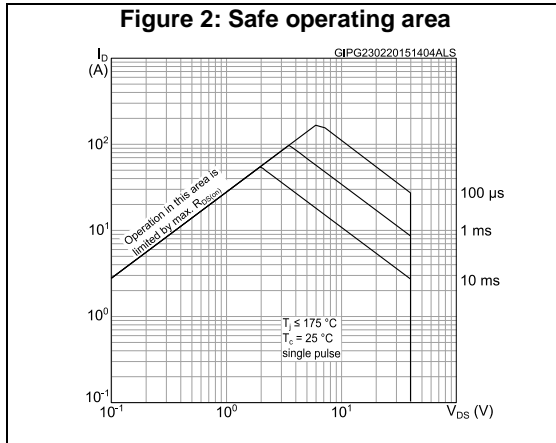


Figure 8: Static drain-source on-resistance

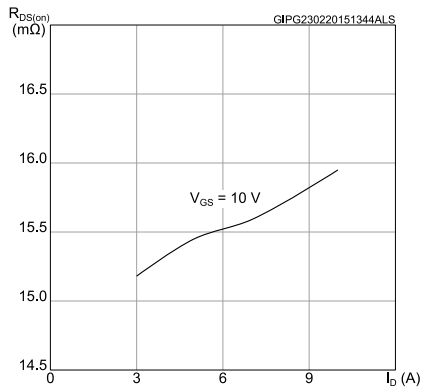


Figure 9: Normalized on-resistance vs. temperature

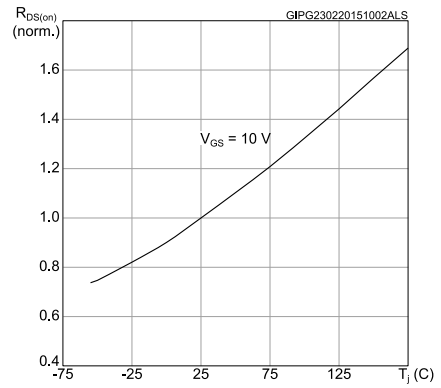


Figure 10: Gate charge vs gate-source voltage

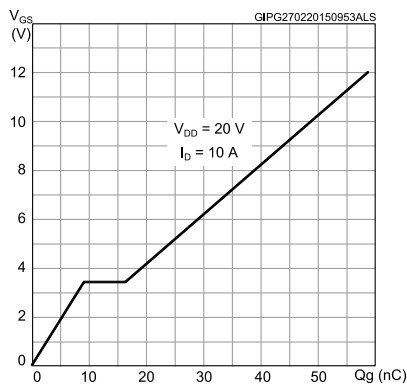


Figure 11: Capacitance variations voltage

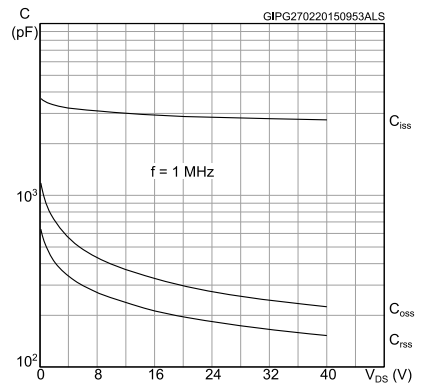
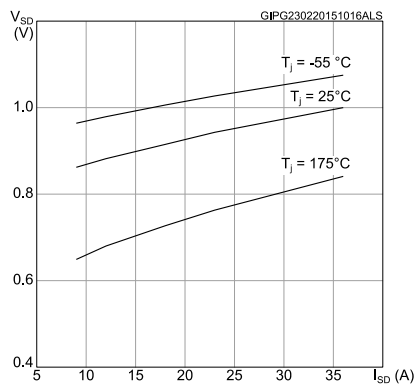


Figure 12: Source-drain diode forward characteristics



### 3 Test circuits

Figure 13: Switching times test circuit for resistive load

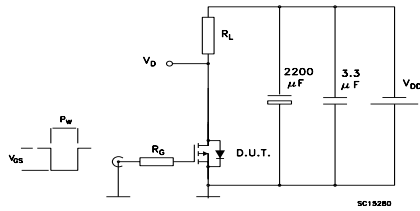


Figure 14: Gate charge test circuit

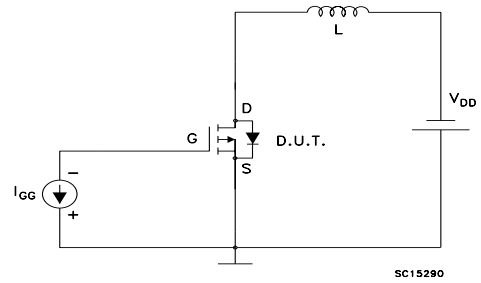
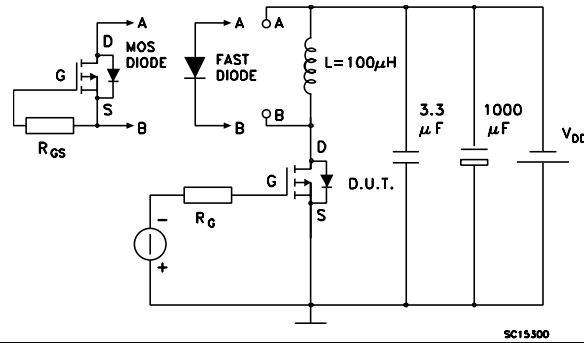


Figure 15: Test circuit for inductive load switching and diode recovery times



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 type R package information

Figure 16: PowerFLAT™ 5x6 type R package outline

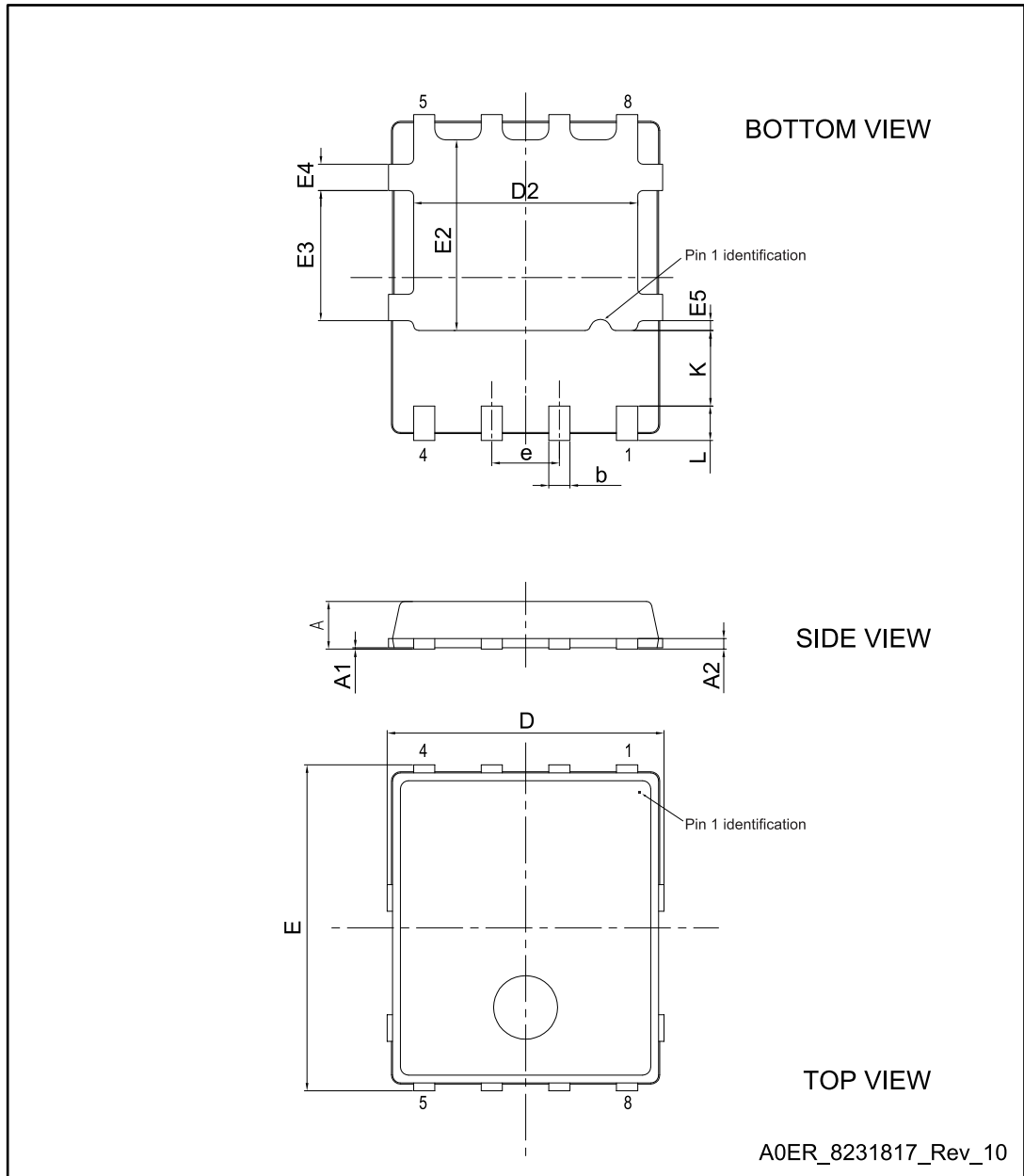
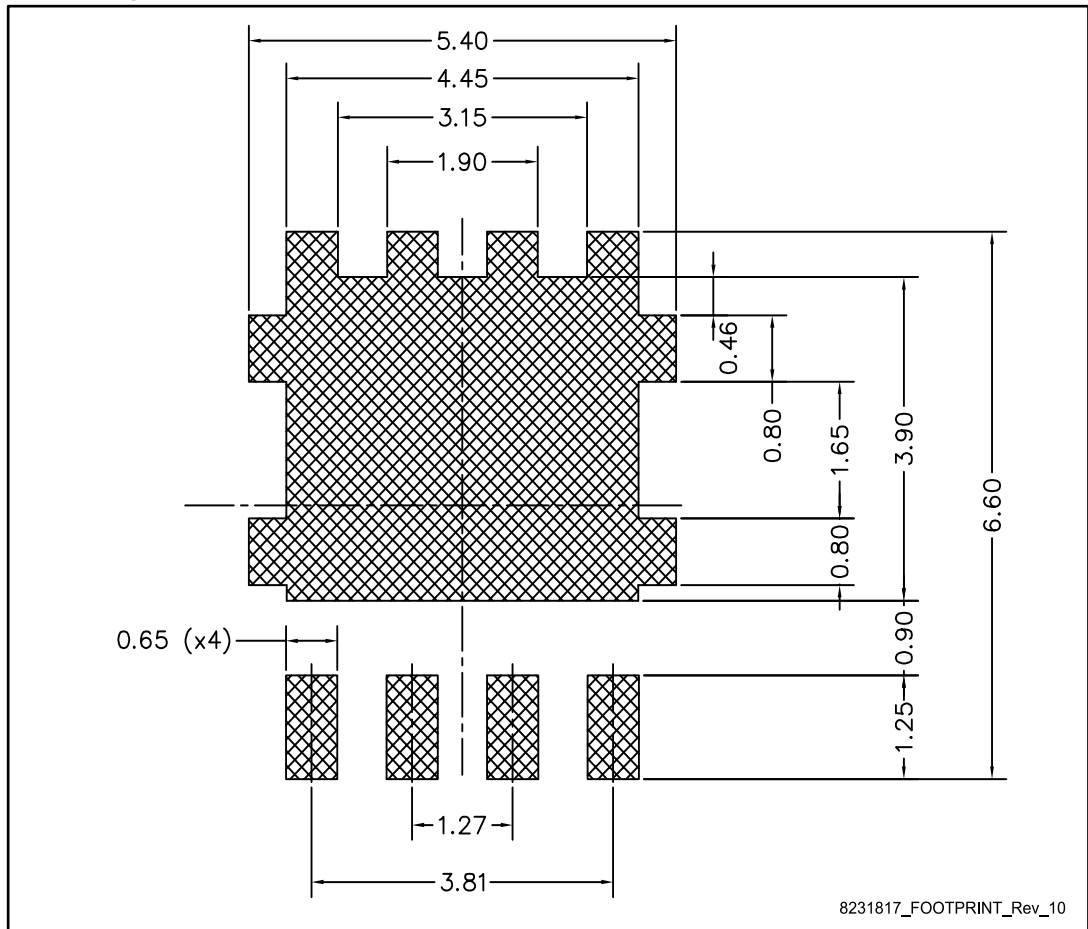


Table 8: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
e		1.27	
L	0.60		0.80
K	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)

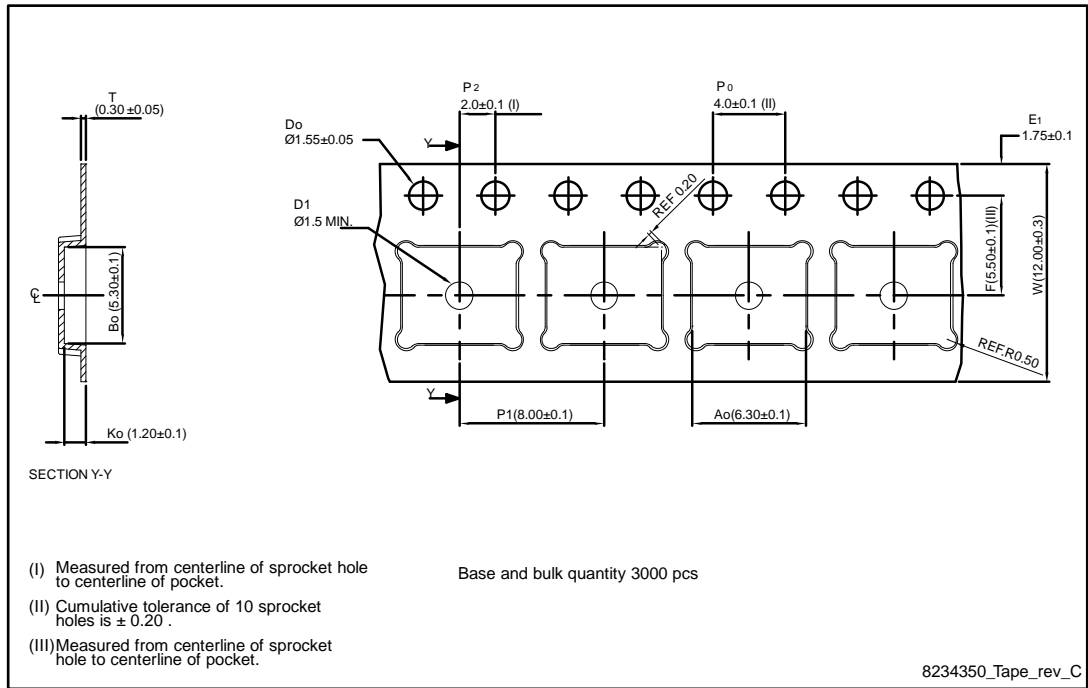


Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape

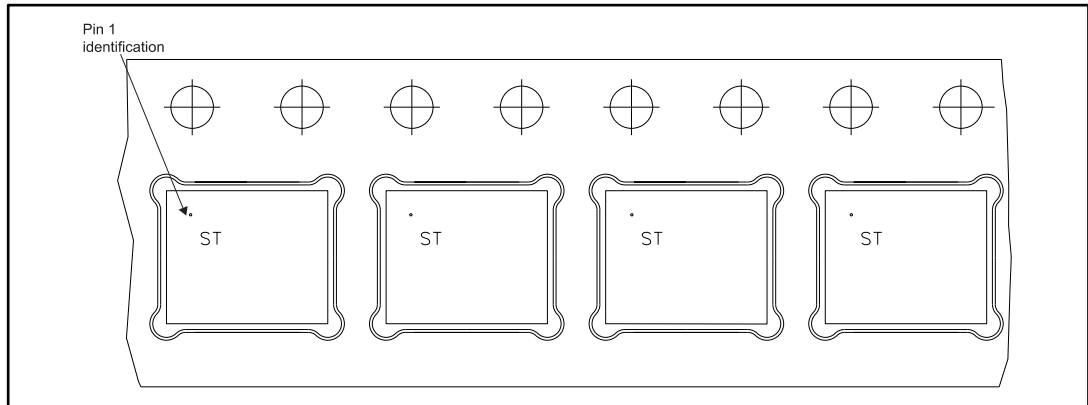
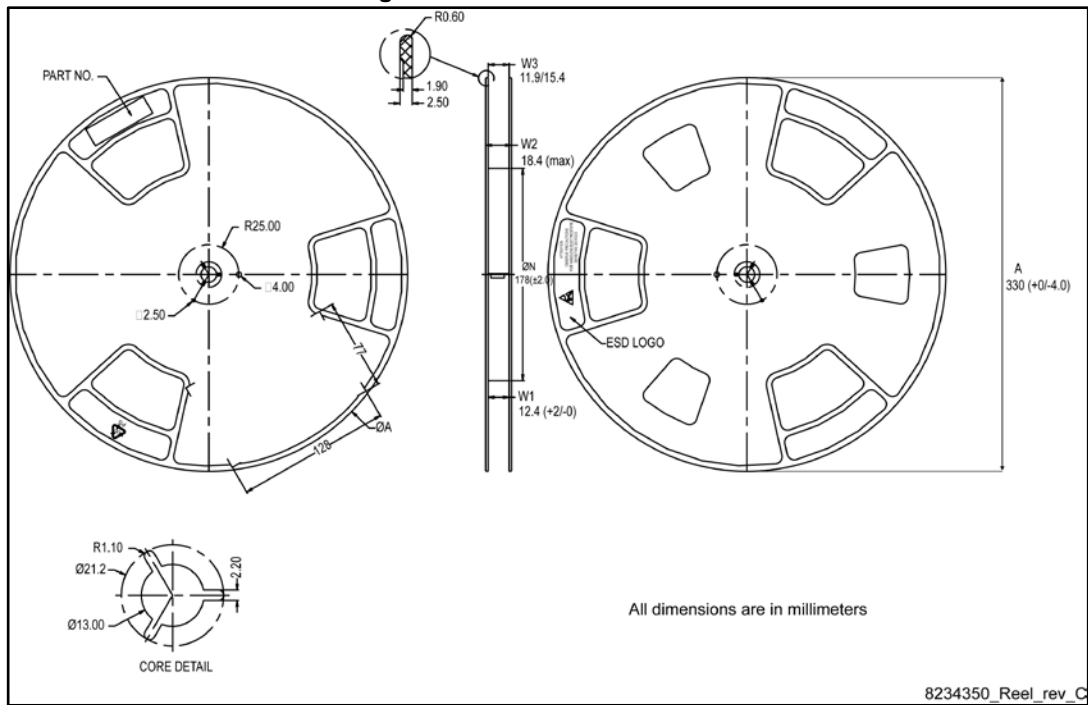


Figure 20: PowerFLAT™ 5x6 reel



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
28-Jan-2014	1	Initial release.
24-Mar-2015	2	Text edits throughout document On cover page, updated title, description and features table Renamed and updated Table 4: Static Updated Table 5: Dynamic Updated Table 6: Switching times Updated Table 7: Source-drain diode Added Section 2.1: Electrical characteristics (curves) Renamed and updated Section 4.1 PowerFLAT™ 5x6 type R package information Renamed and updated Section 5 Packing information

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.



ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View STL42P4LLF6 on WIN SOURCE](#)
-  [STMicroelectronics Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management