

FDD8426H

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 40 V, 12 A, 12 mΩ P-Channel: -40 V, -10 A, 17 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 12 mΩ at $V_{GS} = 10$ V, $I_D = 12$ A
- Max $r_{DS(on)}$ = 15 mΩ at $V_{GS} = 4.5$ V, $I_D = 11$ A

Q2: P-Channel

- Max $r_{DS(on)}$ = 17 mΩ at $V_{GS} = -10$ V, $I_D = -10$ A
- Max $r_{DS(on)}$ = 27 mΩ at $V_{GS} = -4.5$ V, $I_D = -8.3$ A
- 100% UIL Tested
- RoHS Compliant

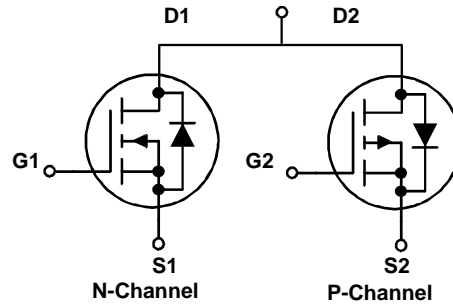
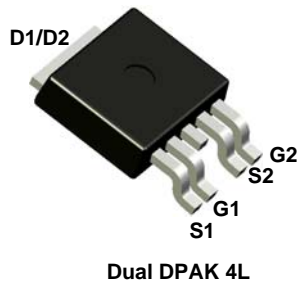


General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Applications

- Inverter
- H-Bridge



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	40	-40	V
V_{GS}	Gate to Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Package Limited)	17	-17	A
	- Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	56	-48	
	- Continuous $T_A = 25^\circ\text{C}$	12	-10	
	- Pulsed	40	-40	
P_D	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$ (Note 1)	56	65	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.1		
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3		
E_{AS}	Single Pulse Avalanche Energy (Note 3)	112	162	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1)	1.4	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1)	1.4	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8426H	FDD8426H	TO-252-4L	13"	12mm	2500units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ $I_D = -250 \mu\text{A}, V_{GS} = 0 \text{ V}$	Q1 Q2	40 -40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C $I_D = -250 \mu\text{A}$, referenced to 25°C	Q1 Q2		35 -32		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -32 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			± 100 ± 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	Q1 Q2	1.5 -1.5	2 2	3.0 -3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C $I_D = -250 \mu\text{A}$, referenced to 25°C	Q1 Q2		-6 6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 11 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}, T_J = 125^\circ\text{C}$	Q1		9.3 11 14	12 15 22	m Ω
		$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -8.3 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}, T_J = 125^\circ\text{C}$	Q2		13 19 19	17 27 30	
g_{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 12 \text{ A}$ $V_{DD} = -5 \text{ V}, I_D = -10 \text{ A}$	Q1 Q2		53 31		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1\text{MHz}$	Q1 Q2		2055 1900	2735 2650	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		255 330	335 440	pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1\text{MHz}$	Q1 Q2		165 200	245 300	pF
R_g	Gate Resistance		Q1 Q2		1.1 3.3		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 20 \text{ V}, I_D = 12 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		9.7 9.7	20 20	ns
t_r	Rise Time		Q1 Q2		4.9 6.9	10 14	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -20 \text{ V}, I_D = -10 \text{ A},$ $V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		27 32	43 51	ns
t_f	Fall Time		Q1 Q2		3.7 7.5	10 15	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{GS} = 0 \text{ V to } -10 \text{ V}$	Q1 Q2	$V_{DD} = 20 \text{ V},$ $I_D = 12 \text{ A}$	38 37	53 52	nC
					20 20	28 28	
Q_{gs}	Gate to Source Charge		Q1 Q2	$V_{DD} = -20 \text{ V},$ $I_D = -10 \text{ A}$	6.3 6.6		nC
					7.1 8		
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2				nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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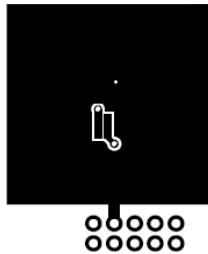
Drain-Source Diode Characteristics

V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -10\text{ A}$ (Note 2)	Q1 Q2		0.8 -0.8	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		22 25	35 40	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		11 14	20 22	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Q1

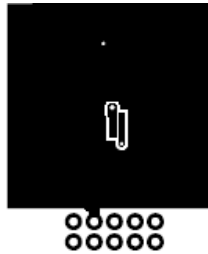


a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 96°C/W when mounted on a minimum pad of 2 oz copper

Q2



a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 96°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty cycle $< 2.0\%$.

- Starting $T_J = 25^\circ\text{C}$, N-ch: $L = 1\text{ mH}$, $I_{AS} = 15\text{ A}$, $V_{DD} = 36\text{ V}$, $V_{GS} = 10\text{ V}$; P-ch: $L = 1\text{ mH}$, $I_{AS} = -18\text{ A}$, $V_{DD} = -36\text{ V}$, $V_{GS} = -10\text{ V}$.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

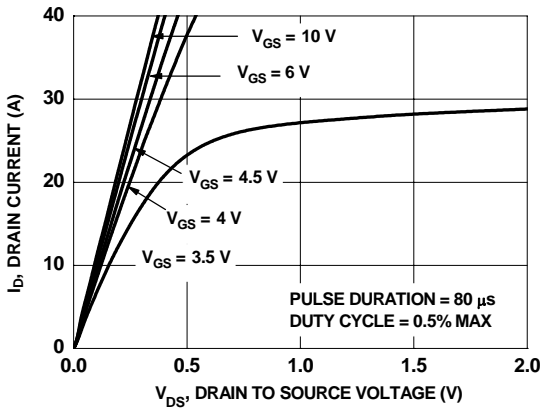


Figure 1. On Region Characteristics

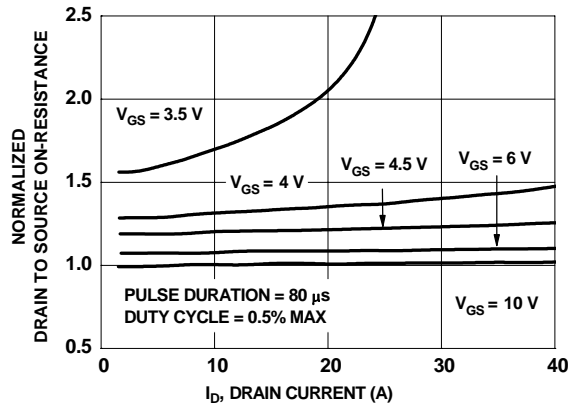


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

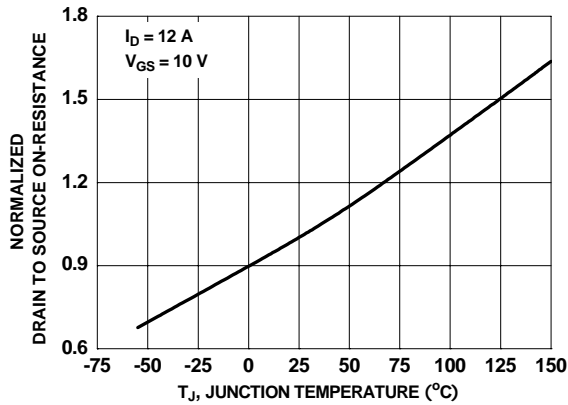


Figure 3. Normalized On Resistance vs Junction Temperature

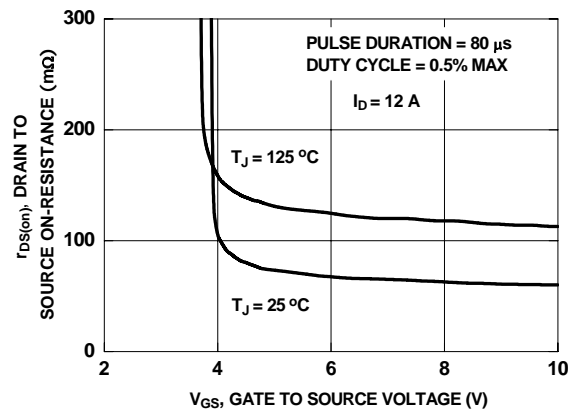


Figure 4. On-Resistance vs Gate to Source Voltage

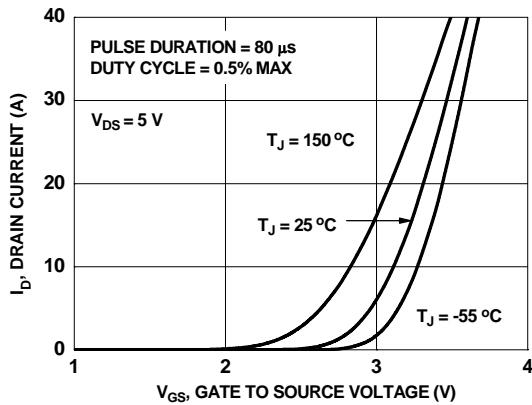


Figure 5. Transfer Characteristics

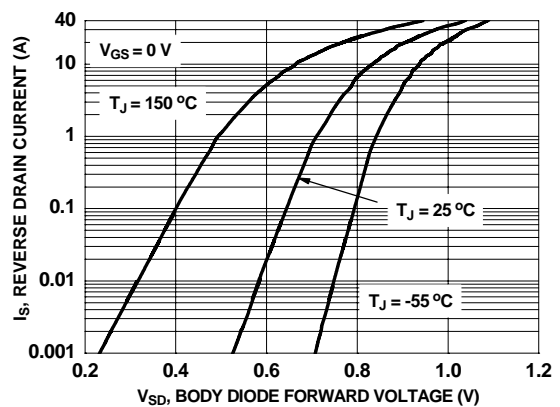


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

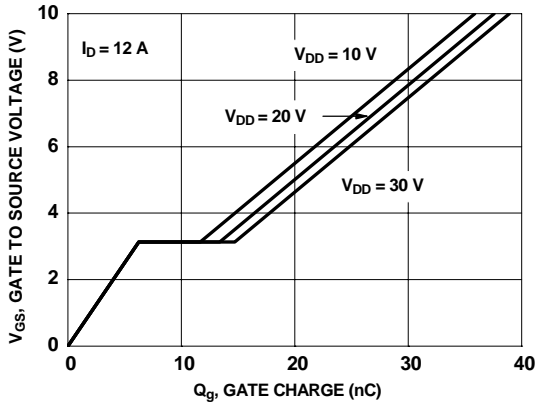


Figure 7. Gate Charge Characteristics

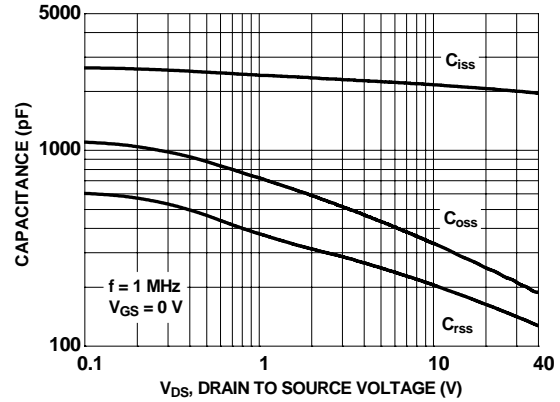


Figure 8. Capacitance vs Drain to Source Voltage

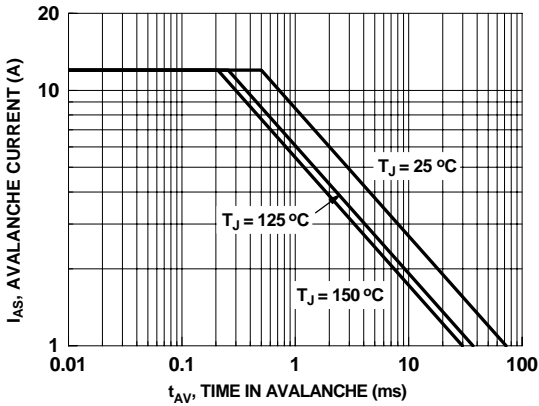


Figure 9. Unclamped Inductive Switching Capability

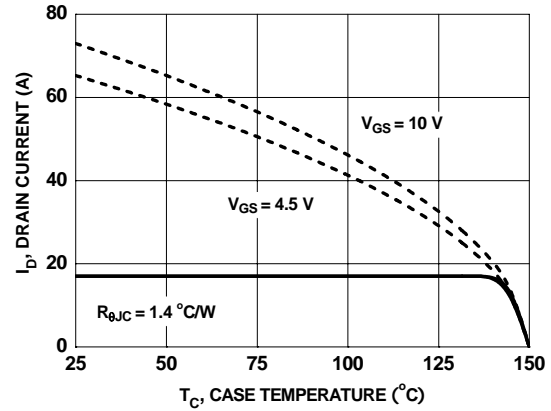


Figure 10. Maximum Continuous Drain Current vs Case Temperature

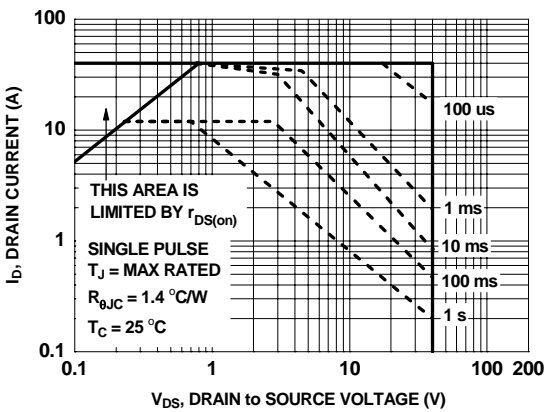


Figure 11. Forward Bias Safe Operating Area

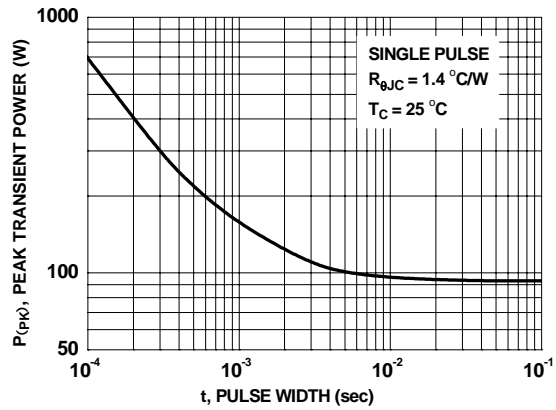


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

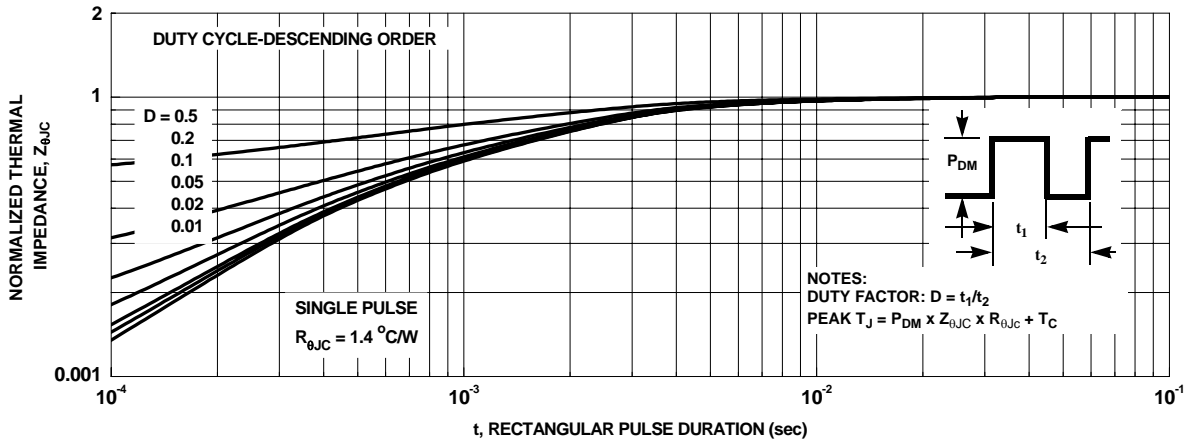


Figure 13. Junction-to-Case Transient Thermal Response Curve

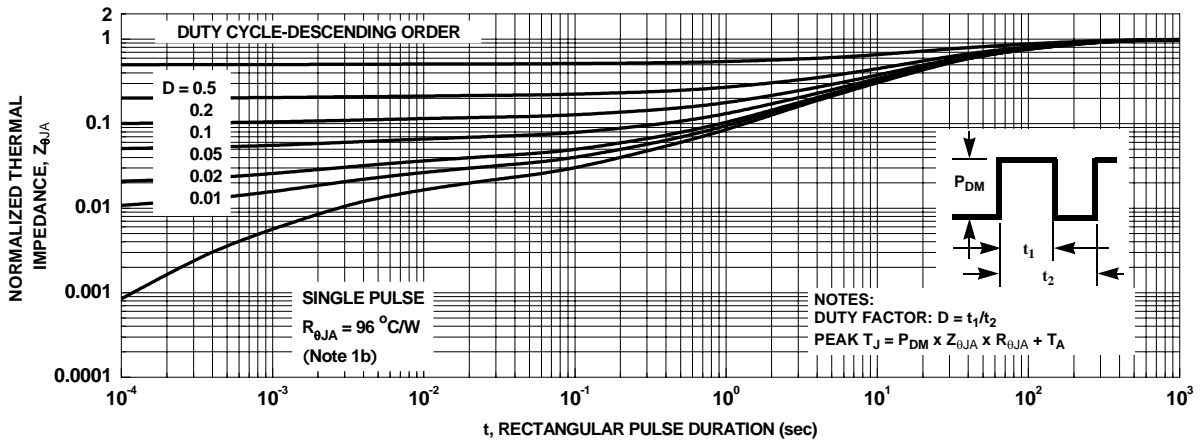


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

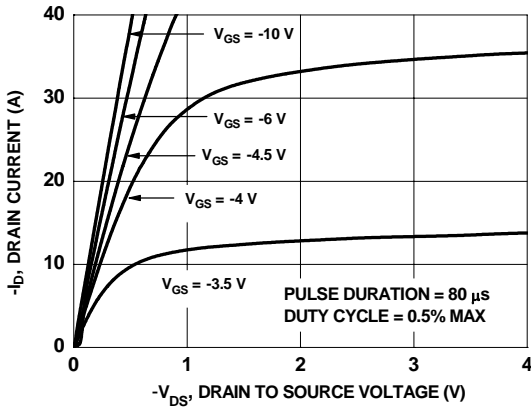


Figure 15. On-Region Characteristics

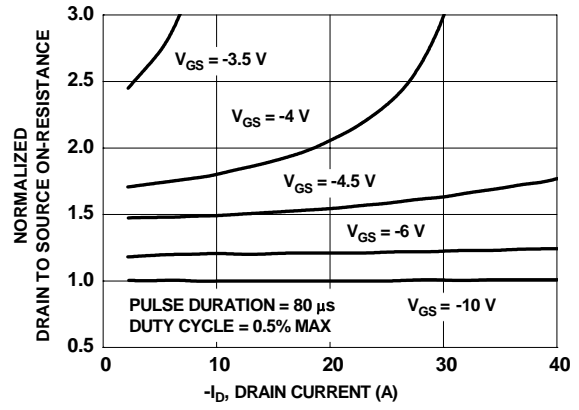


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

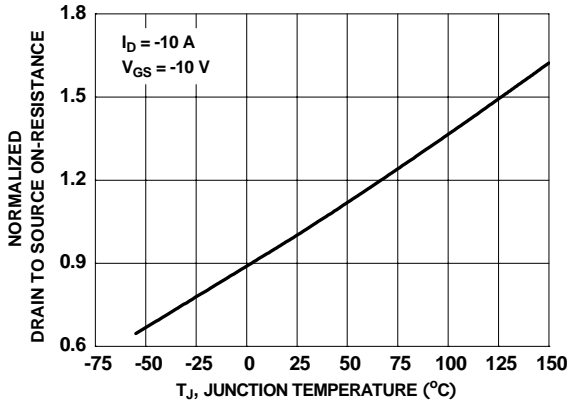


Figure 17. Normalized On-Resistance vs Junction Temperature

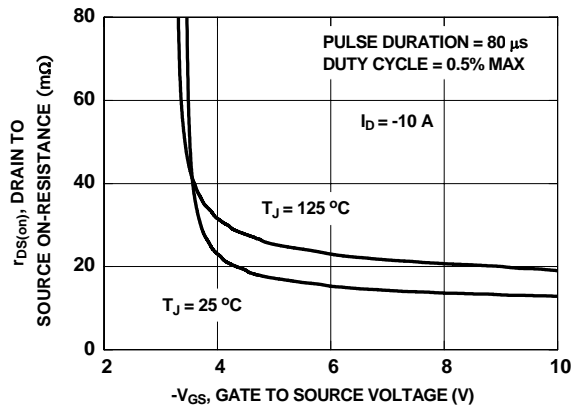


Figure 18. On-Resistance vs Gate to Source Voltage

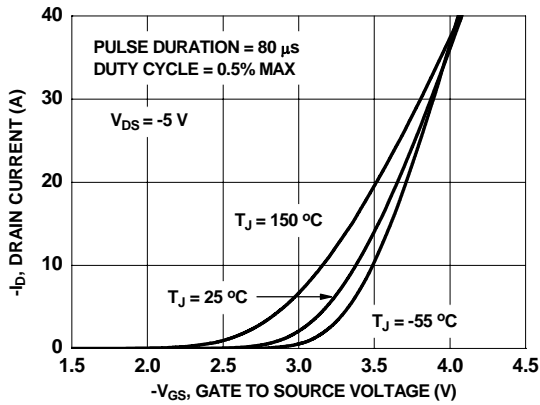


Figure 19. Transfer Characteristics

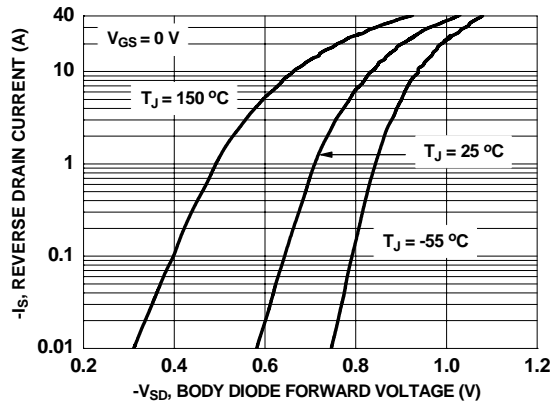


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

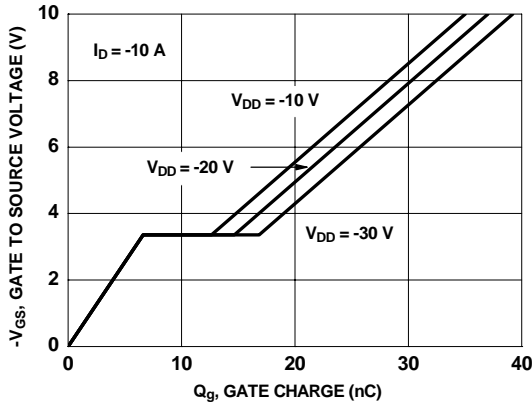


Figure 21. Gate Charge Characteristics

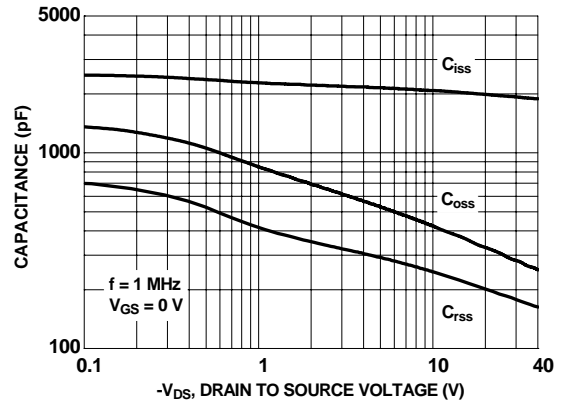


Figure 22. Capacitance vs Drain to Source Voltage

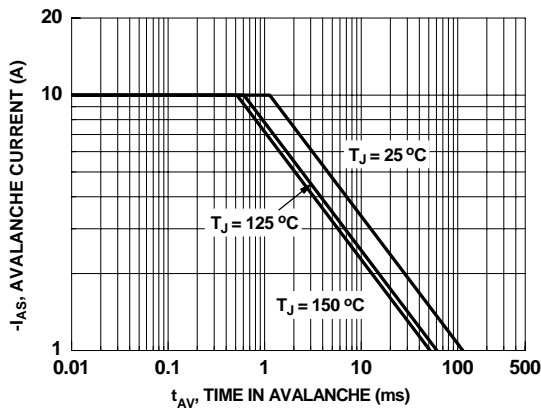


Figure 23. Unclamped Inductive Switching Capability

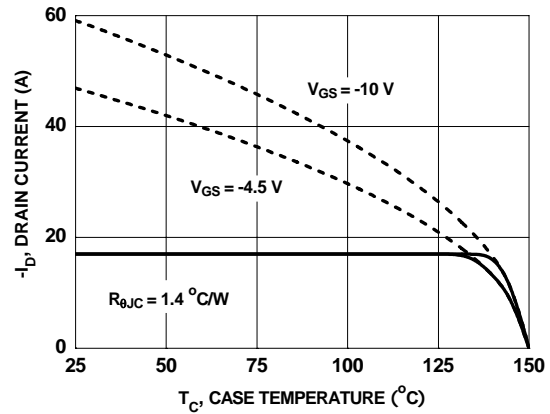


Figure 24. Maximum Continuous Drain Current vs Case Temperature

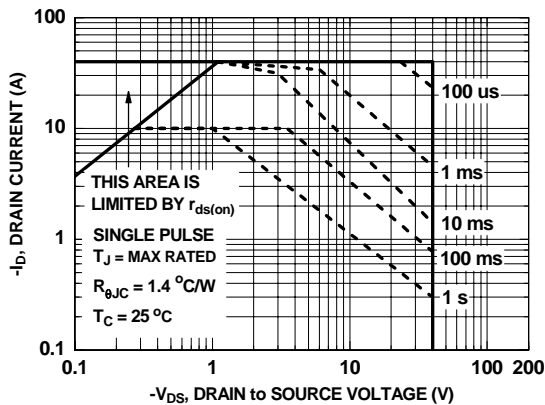


Figure 25. Forward Bias Safe Operating Area

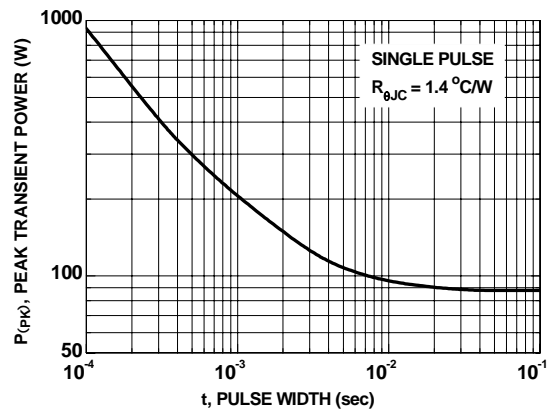


Figure 26. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

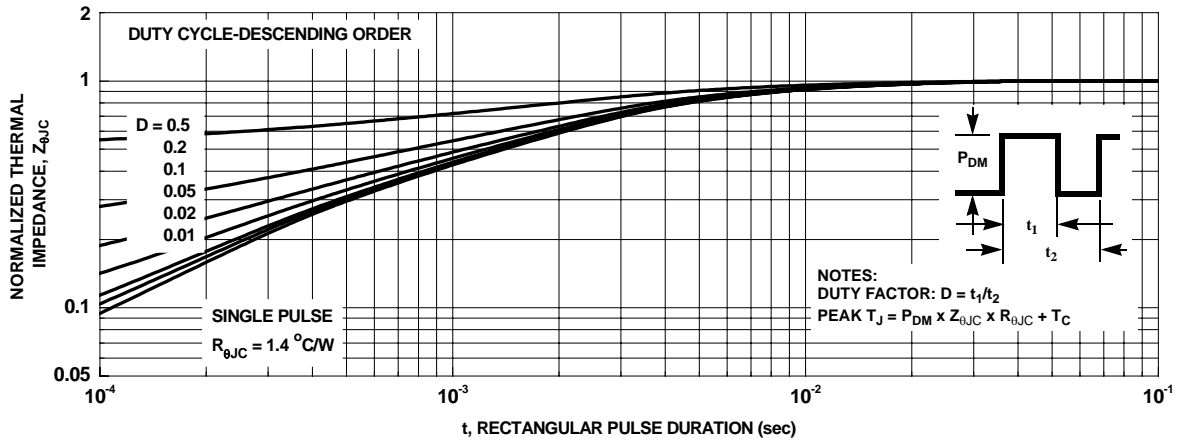


Figure 27. Junction-to-Case Transient Thermal Response Curve

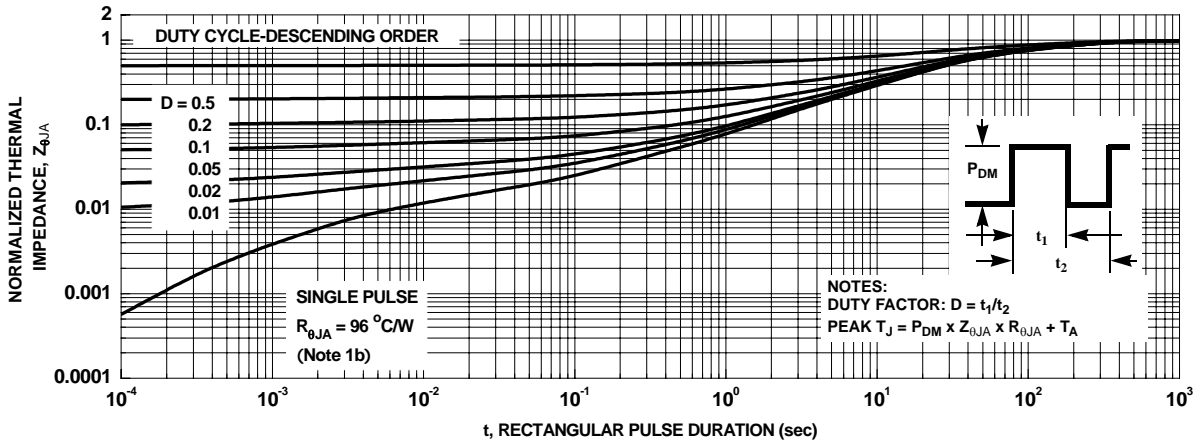
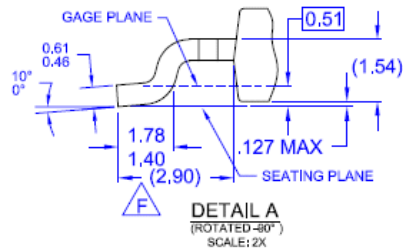
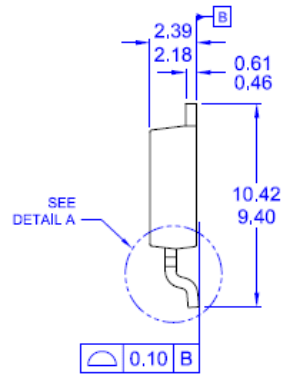
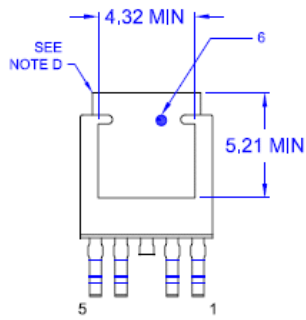
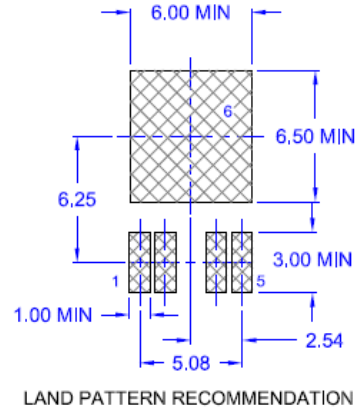
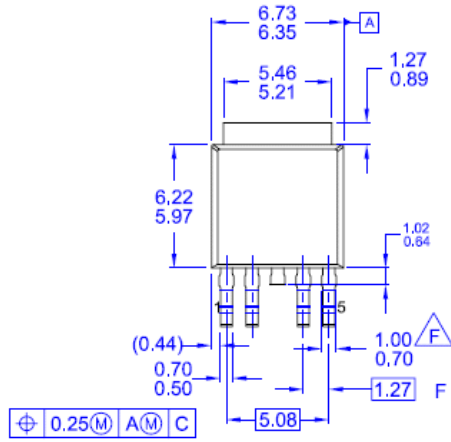


Figure 28. Junction-to-Ambient Transient Thermal Response Curve






Dimensional Outline and Pad Layout





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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT STATUS DEFINITIONS



Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I41

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