



**THE DATASHEET OF
CSD17483F4T**



CSD17483F4 30-V N-Channel FemtoFET™ MOSFET

1 Features

- Low On-Resistance
- Low Q_g and Q_{gd}
- Low-Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
 - 1.0 mm × 0.6 mm
- Ultra-Low Profile
 - 0.35-mm Height
- Integrated ESD Protection Diode
 - Rated > 4-kV HBM
 - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

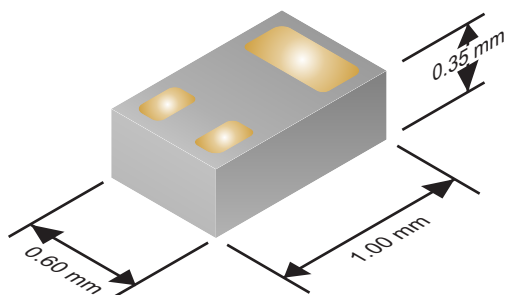
2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Single-Cell Battery Applications
- Handheld and Mobile Applications

3 Description

This 200-m Ω , 30-V N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Typical Part Dimensions



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
Q_g	Gate Charge Total (4.5 V)	1010	pC
Q_{gd}	Gate Charge Gate-to-Drain	130	pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 1.8\text{ V}$	370
		$V_{GS} = 2.5\text{ V}$	240
		$V_{GS} = 4.5\text{ V}$	200
$V_{GS(th)}$	Threshold Voltage	0.85	V

Device Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17483F4	3000	7-Inch Reel	Femto(0402)	Tape and Reel
CSD17483F4T	250		1.00 mm × 0.60 mm SMD Lead Less	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	12	V
I_D	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	1.5	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	5	A
I_G	Continuous Gate Clamp Current	35	mA
	Pulsed Gate Clamp Current ⁽²⁾	350	
P_D	Power Dissipation ⁽¹⁾	500	mW
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
T_J , T_{stg}	Operating Junction, Storage Temperature	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 7.4\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	2.7	mJ

(1) Typical $R_{\theta JA} = 90^\circ\text{C/W}$ on 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Top View

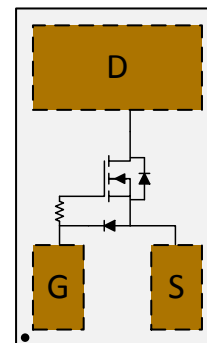


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4 Revision History

Changes from Revision D (December 2016) to Revision E	Page
• Raised I_{DSS} Test Condition Voltage	3
• Raised I_{GSS} Test Condition Voltage	3

Changes from Revision C (September 2014) to Revision D	Page
• Added <i>Receiving Notification of Documentation Updates</i> in the <i>Device and Documentation Support</i> section	7
• Added <i>Community Resources</i> in the <i>Device and Documentation Support</i> section	7
• Updated all mechanical drawings, increased the size of the pads in the <i>Recommended Stencil Pattern</i> section.	8

Changes from Revision B (January 2014) to Revision C	Page
• Corrected timing V_{DS} to read 15 V	3

Changes from Revision A (November 2013) to Revision B	Page
• Added I_G parameter	1
• Lowered I_{DSS} limit.....	3
• Lowered I_{GSS} limit	3

Changes from Original (July 2013) to Revision A	Page
• Removed jumbo reel info and included small reel info.....	1

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	30			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			100	nA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 10\text{ V}$			50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.65	0.85	1.10	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 1.8\text{ V}, I_{DS} = 0.5\text{ A}$		370	550	m Ω
		$V_{GS} = 2.5\text{ V}, I_{DS} = 0.5\text{ A}$		240	310	
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.5\text{ A}$		200	260	
		$V_{GS} = 8\text{ V}, I_{DS} = 0.5\text{ A}$		185	240	
g_{fs}	Transconductance	$V_{DS} = 15\text{ V}, I_{DS} = 0.5\text{ A}$		2.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V},$ $f = 1\text{ MHz}$		145	190	pF
C_{oss}	Output capacitance			42	55	pF
C_{rss}	Reverse transfer capacitance			2	3	pF
R_G	Series gate resistance			23		Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 15\text{ V}, I_{DS} = 0.5\text{ A}$		1010	1300	pC
Q_{gd}	Gate charge gate-to-drain			130		pC
Q_{gs}	Gate charge gate-to-source			220		pC
$Q_{g(th)}$	Gate charge at V_{th}			145		pC
Q_{oss}	Output charge		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		1095	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 0.5\text{ A}, R_G = 2\ \Omega$		3.3		ns
t_r	Rise time			1.3		ns
$t_{d(off)}$	Turnoff delay time			10.6		ns
t_f	Fall time			3.4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 0.5\text{ A}, V_{GS} = 0\text{ V}$		0.73	0.9	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 15\text{ V}, I_F = 0.5\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		1475		pC
t_{rr}	Reverse recovery time			5.5		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	90	$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance ⁽²⁾	250	

(1) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

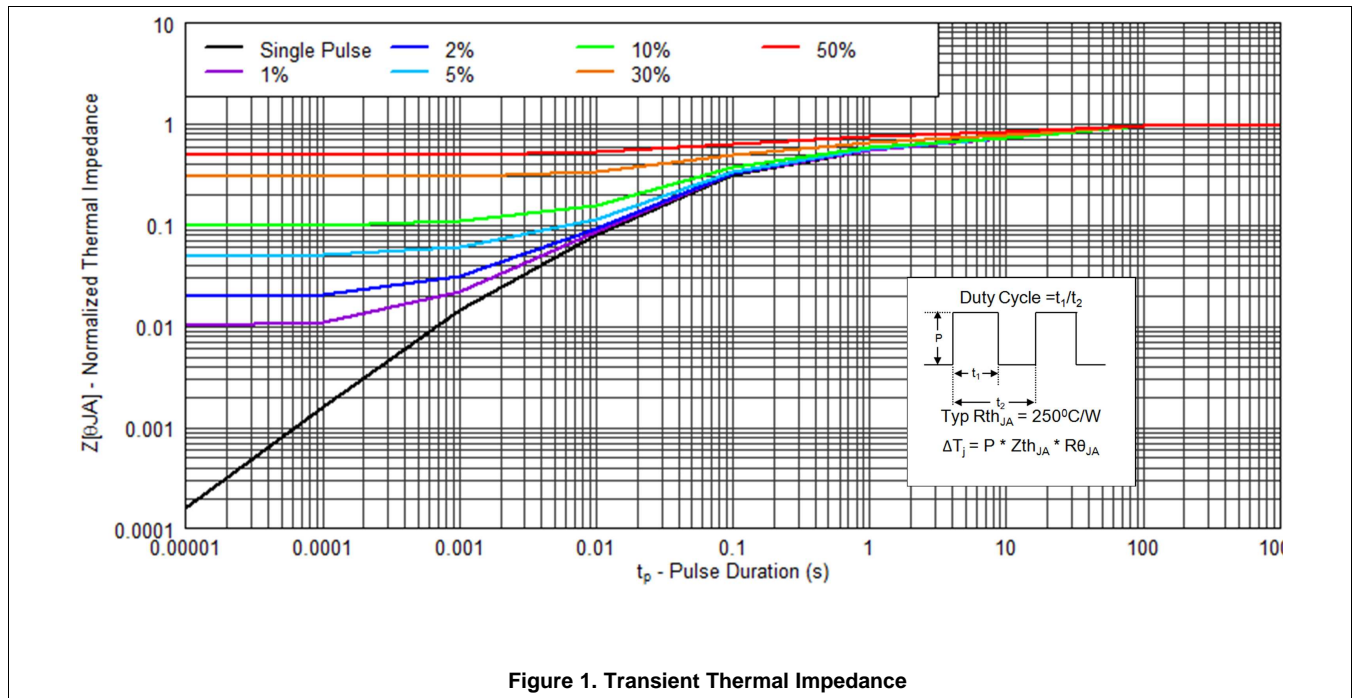


Figure 1. Transient Thermal Impedance

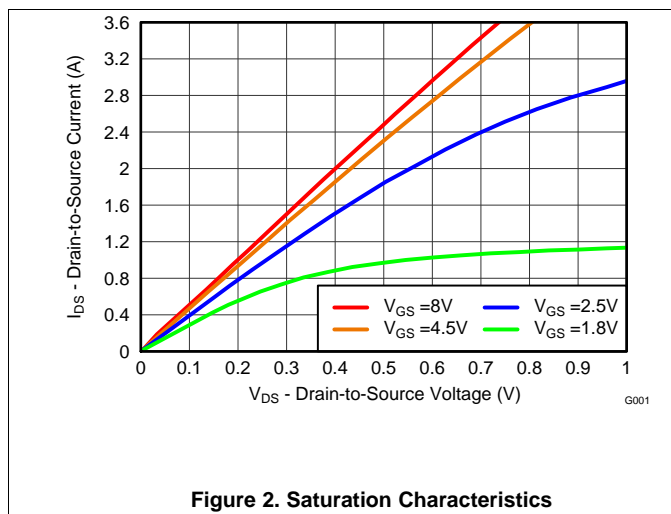


Figure 2. Saturation Characteristics

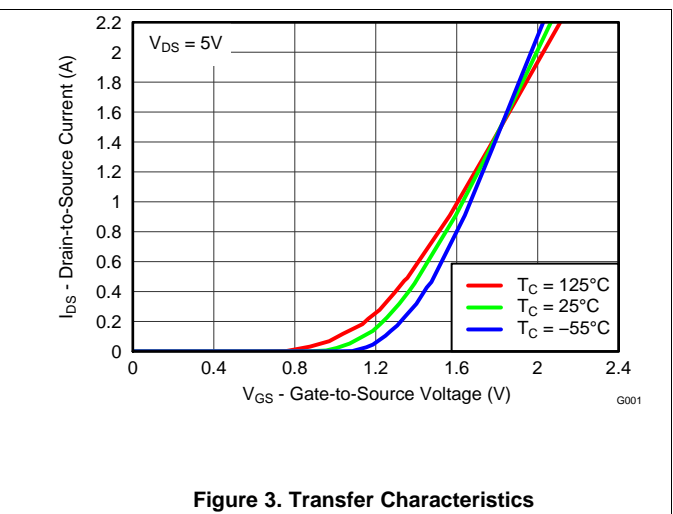
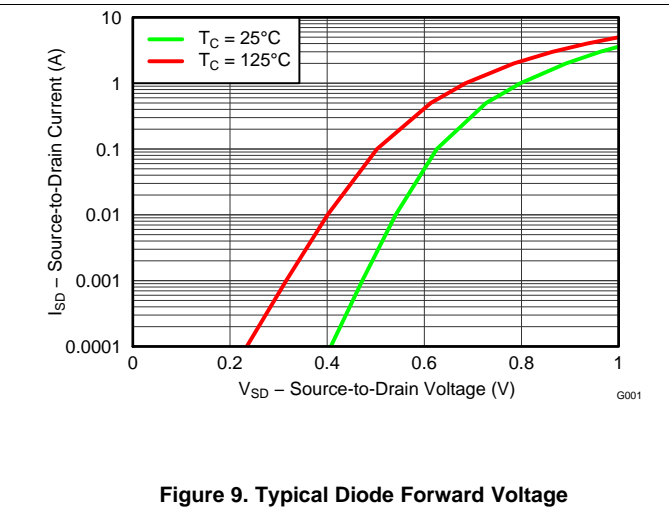
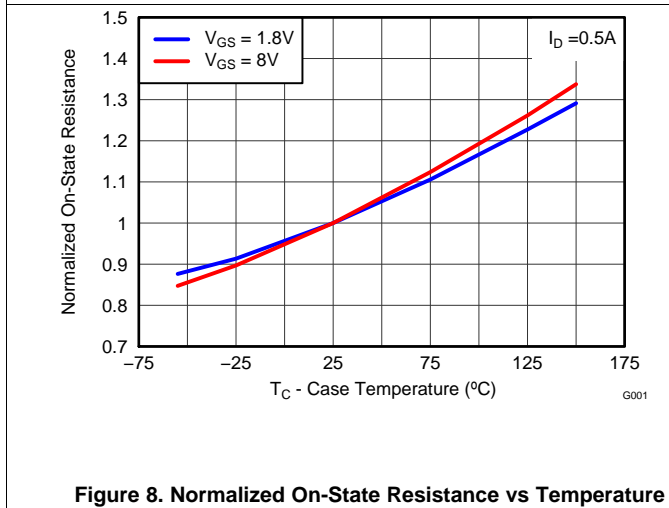
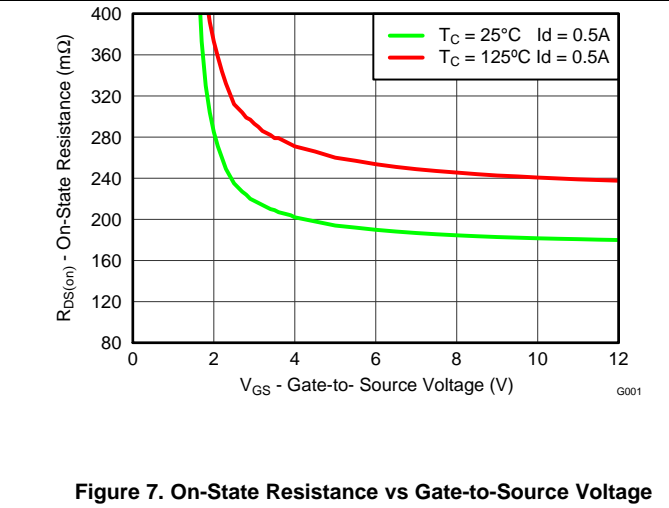
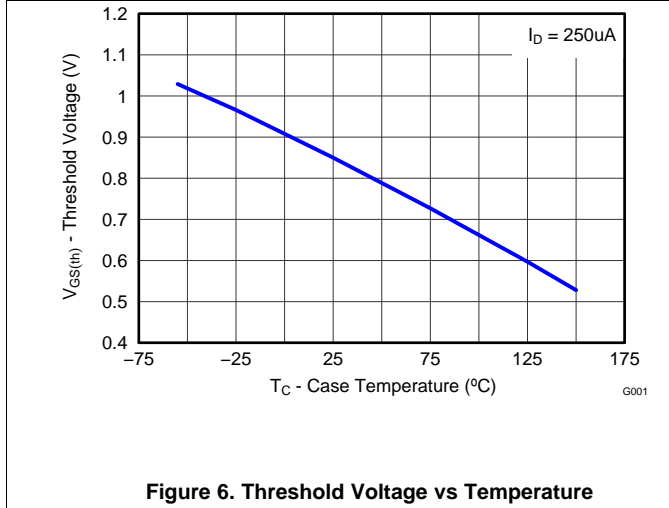
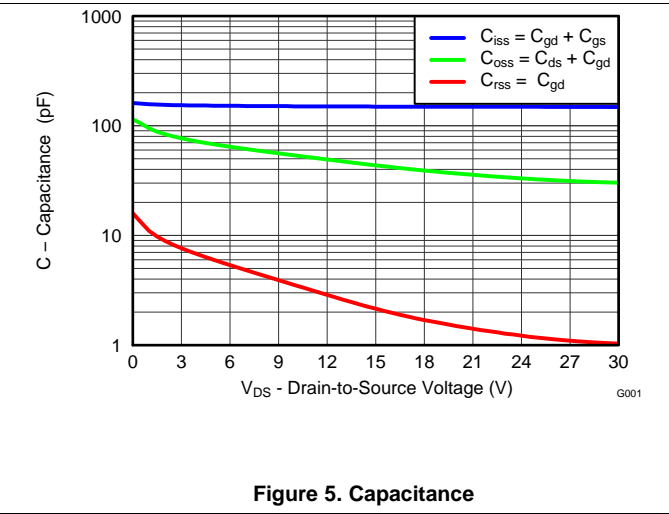
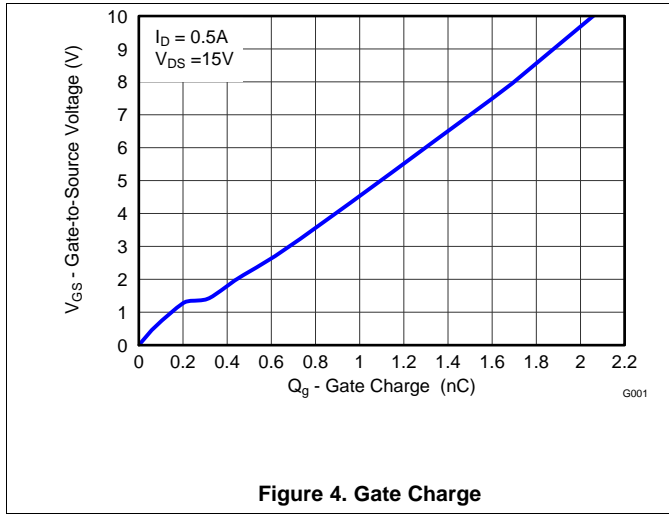


Figure 3. Transfer Characteristics

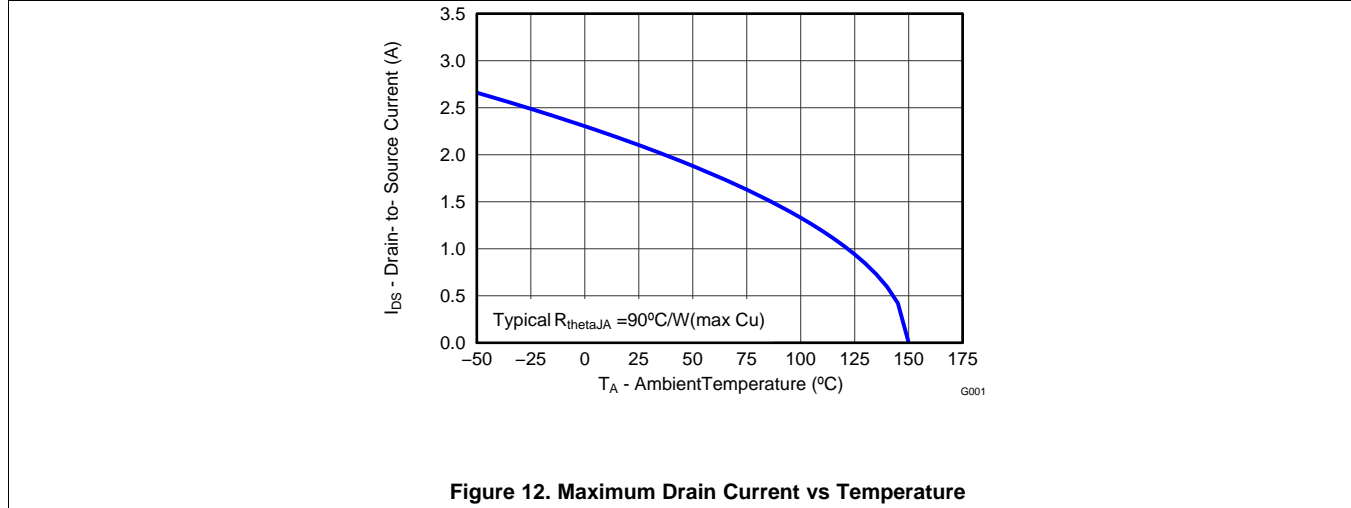
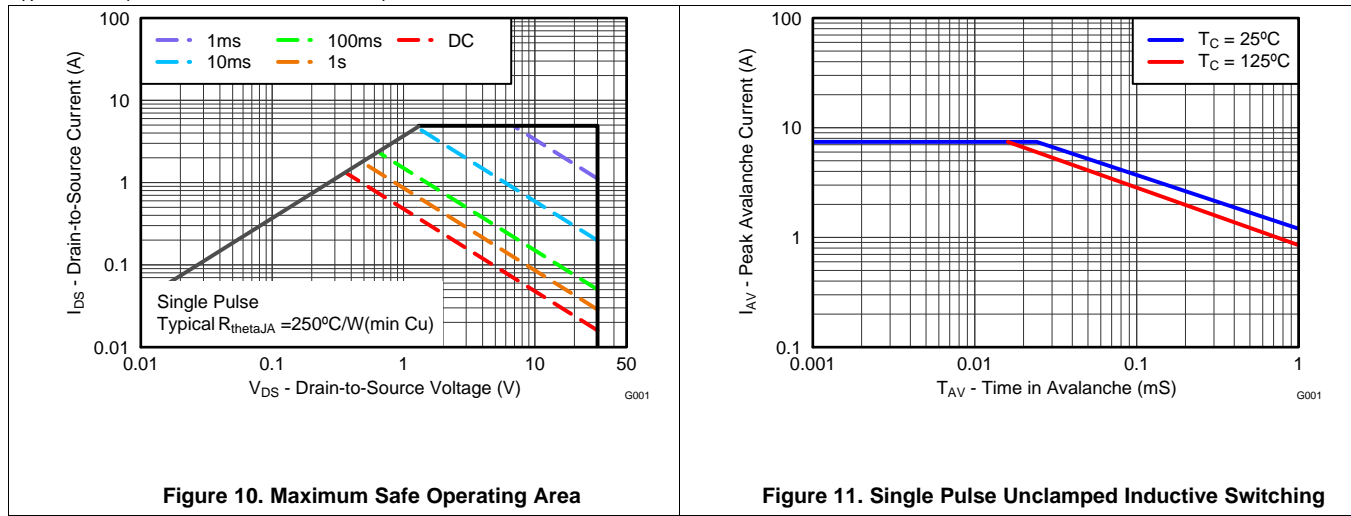
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

FemtoFET, E2E are trademarks of Texas Instruments.
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6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

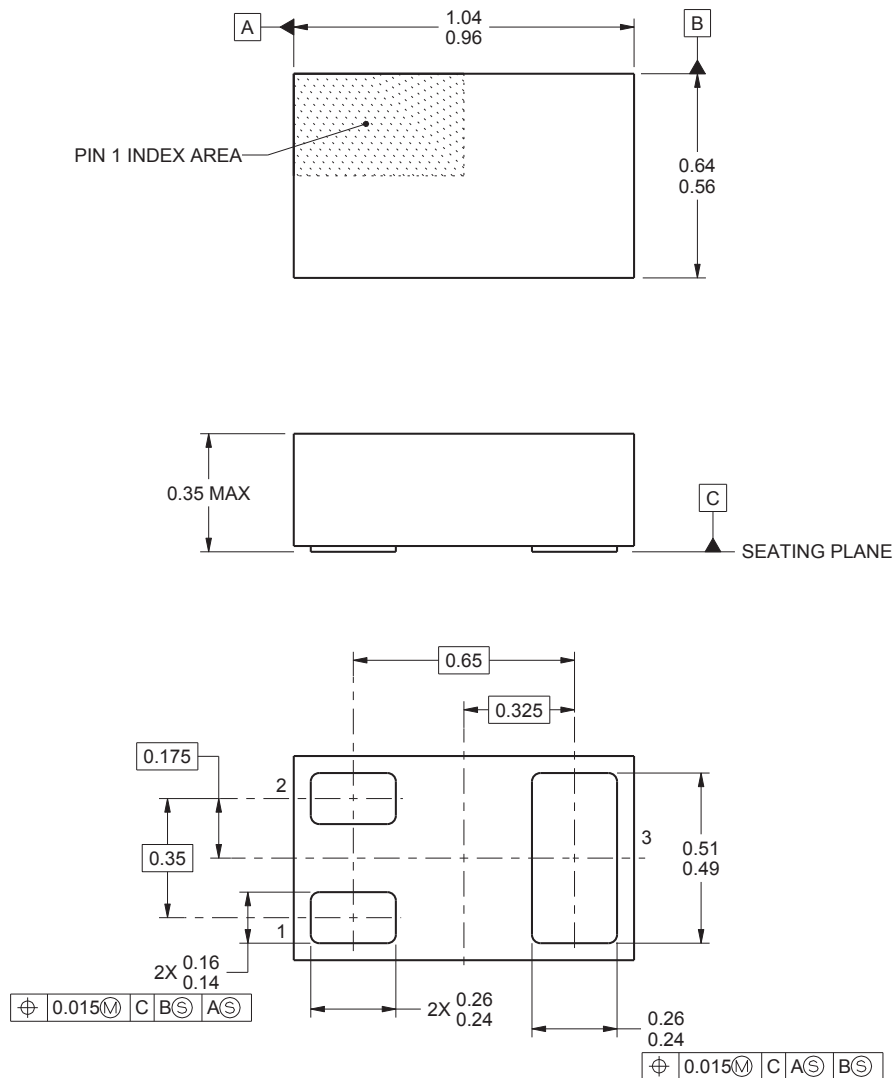
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

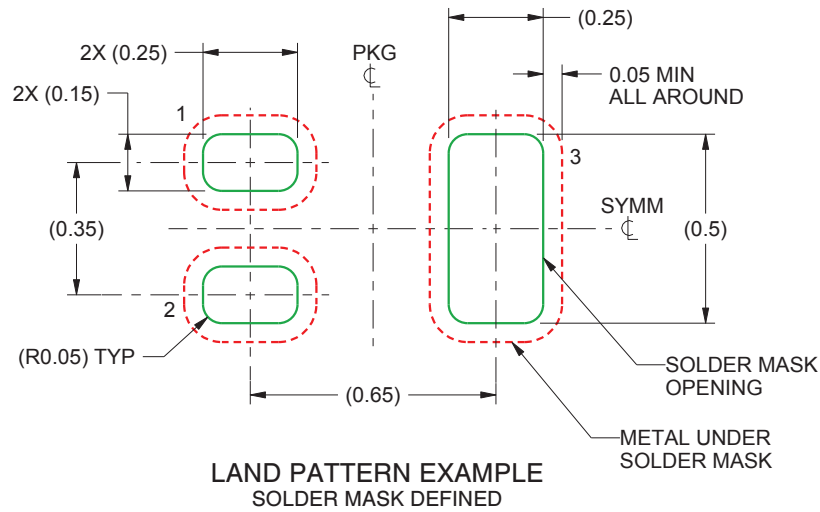
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



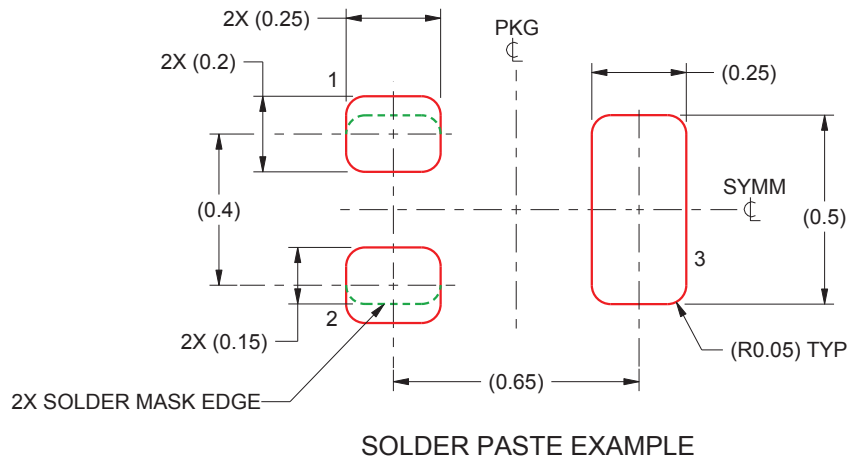
- (1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- (2) This drawing is subject to change without notice.
- (3) This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

7.2 Recommended Minimum PCB Layout





- (1) All dimensions are in millimeters.
- (2) For more information, see [QFN/SON PCB Attachment](#) (SLUA271).

7.3 Recommended Stencil Pattern



- (1) All dimensions are in millimeters.
- (2) Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17483F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	DP	
CSD17483F4T	ACTIVE	PICOSTAR	YJC	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	DP	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17483F4	PICOST AR	YJC	3	3000	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4	PICOST AR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4T	PICOST AR	YJC	3	250	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4T	PICOST AR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17483F4	PICOSTAR	YJC	3	3000	220.0	220.0	35.0
CSD17483F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD17483F4T	PICOSTAR	YJC	3	250	220.0	220.0	35.0
CSD17483F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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